

# FDW2521C

## Complementary PowerTrench® MOSFET

### General Description

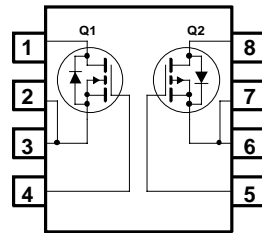
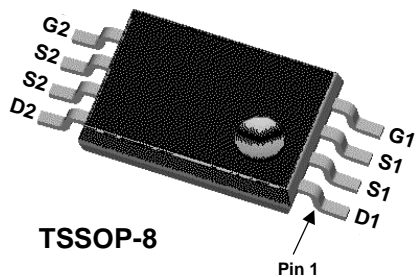
This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

### Applications

- DC/DC conversion
- Power management
- Load switch

### Features

- **Q1: N-Channel**  
5.5 A, 20 V.  $R_{DS(ON)} = 21\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$   
 $R_{DS(ON)} = 35\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- **Q2: P-Channel**  
-3.8 A, 20 V.  $R_{DS(ON)} = 43\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$   
 $R_{DS(ON)} = 70\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Low profile TSSOP-8 package



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DSS}$	Drain-Source Voltage	20	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	$\pm 12$	V
$I_D$	Drain Current - Continuous (Note 1a)	5.5	-3.8	A
	- Pulsed	30	-30	
$P_D$	Power Dissipation (Note 1a) (Note 1b)	1.0		W
		0.6		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	125	$^\circ\text{C/W}$
		208	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2521C	FDW2521C	13"	12mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Off Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	Q1 Q2	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		14 -16		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA
<b>On Characteristics (Note 2)</b>							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	Q1 Q2	0.6 -0.6	0.8 -1.0	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		-3.2 3.0		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 4.2\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}, I_D = -3.8\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -3.0\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.8\text{ A}, T_J = 125^\circ\text{C}$	Q1 Q2		17 24 23 36 56 49	21 35 34 43 70 69	$\text{m}\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	Q1 Q2	30 -15			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 5.5\text{ A}$ $V_{DS} = -5\text{ V}, I_D = -3.5\text{ A}$	Q1 Q2		26 13.2		S
<b>Dynamic Characteristics</b>							
$C_{iss}$	Input Capacitance	Q1: $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	Q1 Q2		1082 1030		pF
$C_{oss}$	Output Capacitance	Q2: $f = 1.0\text{ MHz}$	Q1 Q2		277 280		pF
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	Q1 Q2		130 120		pF
<b>Switching Characteristics</b>							
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 10\text{ V}, I_D = 1\text{ A}$ , $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		8 11	20 20	ns
$t_r$	Turn-On Rise Time	Q2: $V_{DD} = -5\text{ V}, I_D = -1\text{ A}$ , $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		8 18	27 32	ns
$t_{d(off)}$	Turn-Off Delay Time	Q1: $V_{DD} = -5\text{ V}, I_D = -1\text{ A}$ , $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		24 34	38 55	ns
$t_f$	Turn-Off Fall Time	Q2: $V_{DD} = -5\text{ V}, I_D = -1\text{ A}$ , $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		8 34	16 55	ns
$Q_g$	Total Gate Charge	Q1: $V_{DS} = 10\text{ V}, I_D = 5.5\text{ A}, V_{GS} = 4.5\text{ V}$	Q1 Q2		12 9.7	17 16	nC
$Q_{gs}$	Gate-Source Charge	Q2: $V_{DS} = -5\text{ V}, I_D = -3.8\text{ A}, V_{GS} = -4.5\text{ V}$	Q1 Q2		2 2.2		nC
$Q_{gd}$	Gate-Drain Charge	Q1: $V_{DS} = -5\text{ V}, I_D = -3.8\text{ A}, V_{GS} = -4.5\text{ V}$	Q1 Q2		3 2.4		nC

**Electrical Characteristics** (continued) $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			0.83 -0.83	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.83\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -0.83\text{ A}$ (Note 2)	Q1 Q2		0.7 -0.7	1.2 -1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

- a)  $R_{\theta JA}$  is  $125^\circ\text{C/W}$  (steady state) when mounted on a 1 inch<sup>2</sup> copper pad on FR-4.
- b)  $R_{\theta JA}$  is  $208^\circ\text{C/W}$  (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

Typical Characteristics: Q1

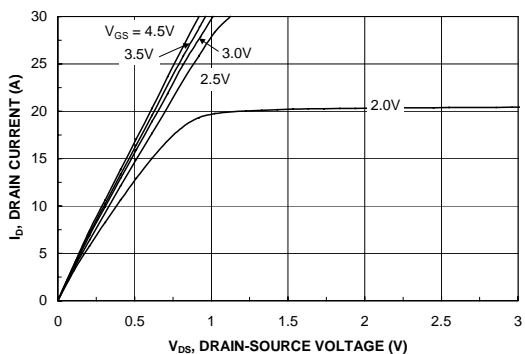


Figure 1. On-Region Characteristics.

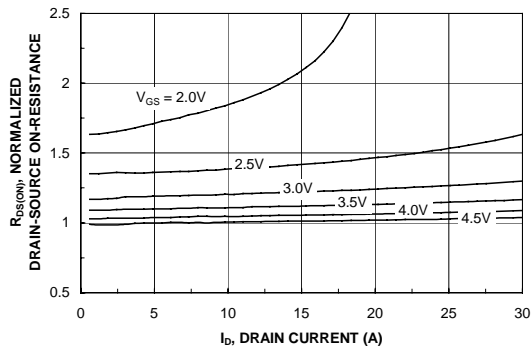


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

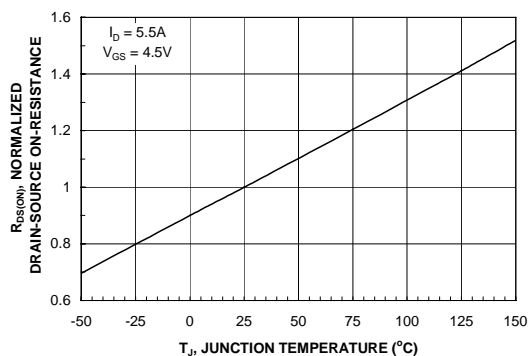


Figure 3. On-Resistance Variation with Temperature.

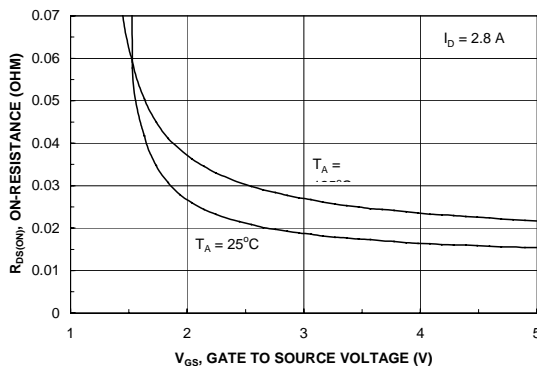


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

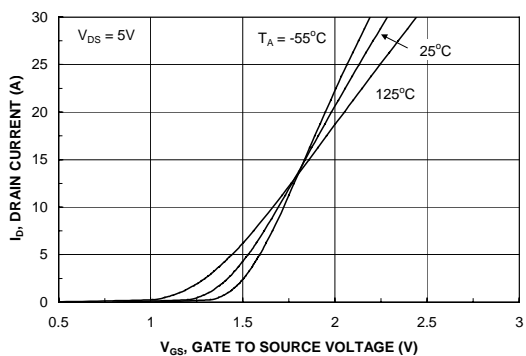


Figure 5. Transfer Characteristics.

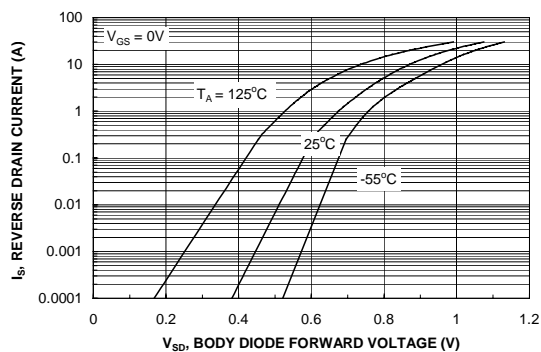


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

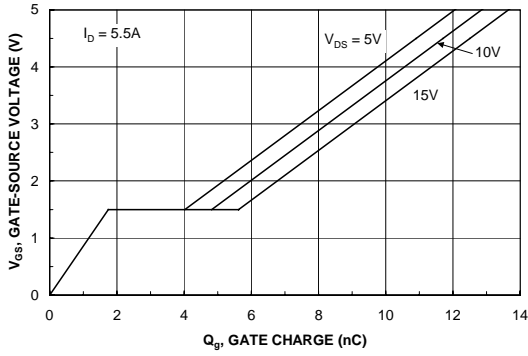


Figure 7. Gate Charge Characteristics.

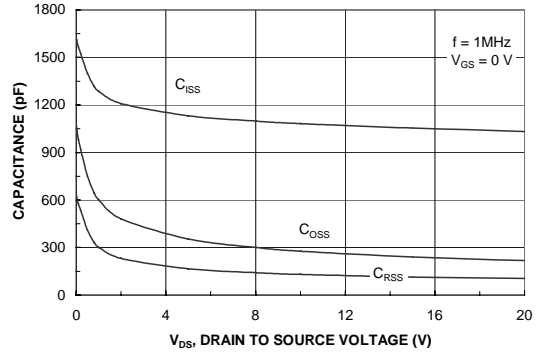


Figure 8. Capacitance Characteristics.

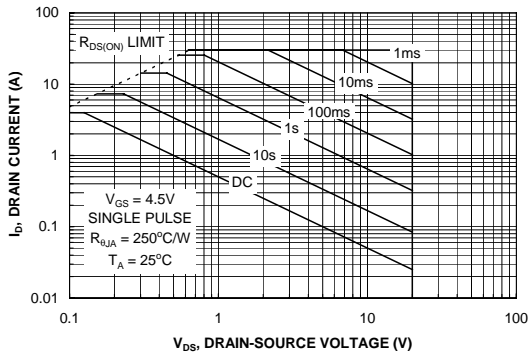


Figure 9. Maximum Safe Operating Area.

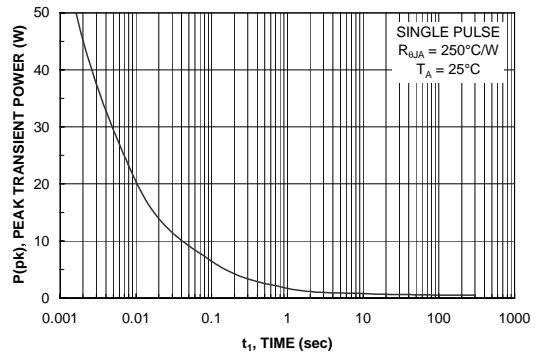


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q2

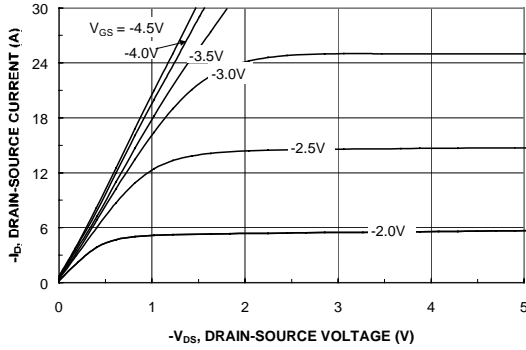


Figure 11. On-Region Characteristics.

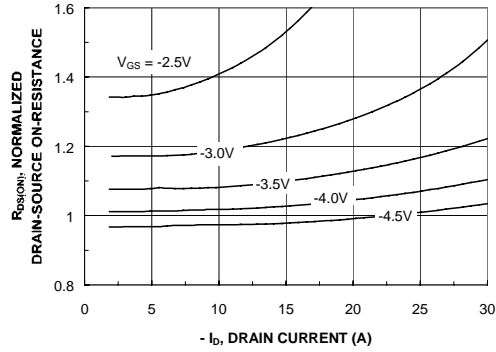


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

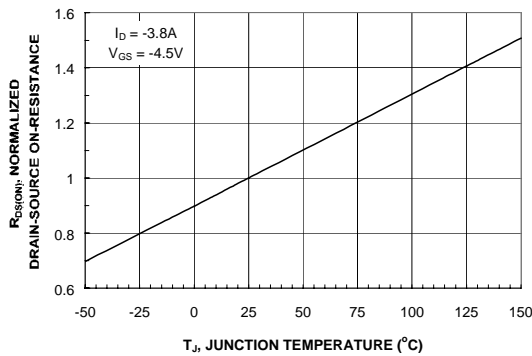


Figure 13. On-Resistance Variation with Temperature.

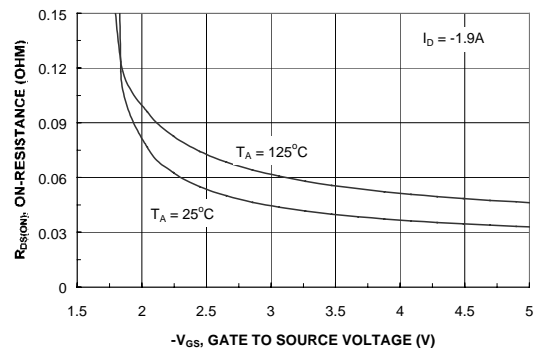


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

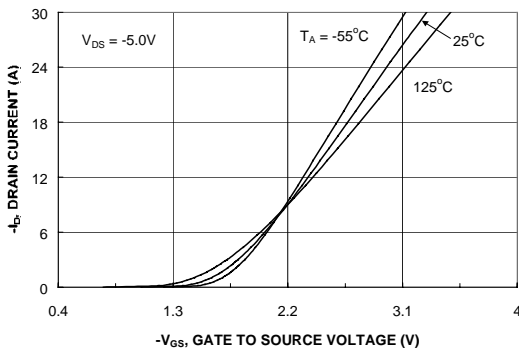


Figure 15. Transfer Characteristics.

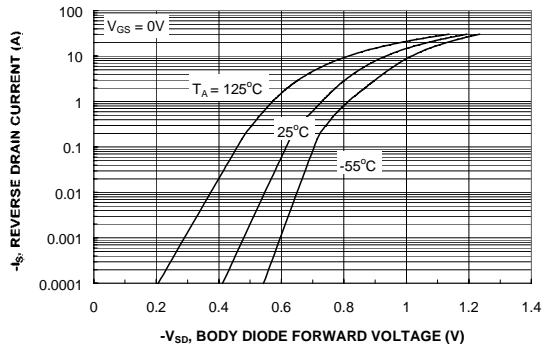


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

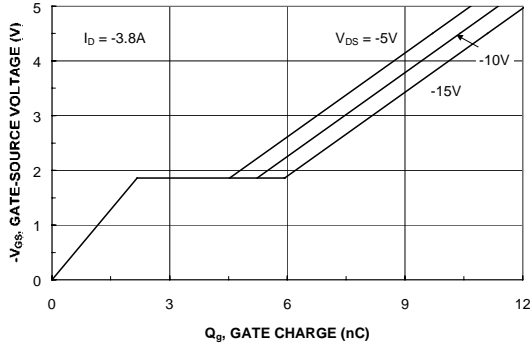


Figure 17. Gate Charge Characteristics.

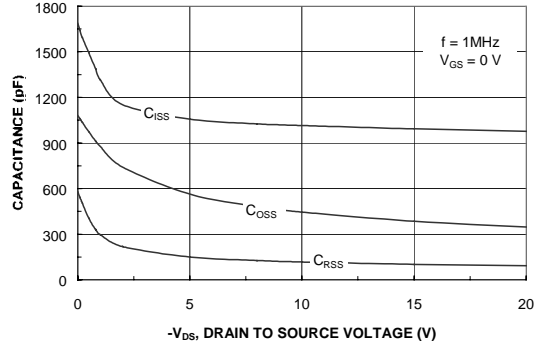


Figure 18. Capacitance Characteristics.

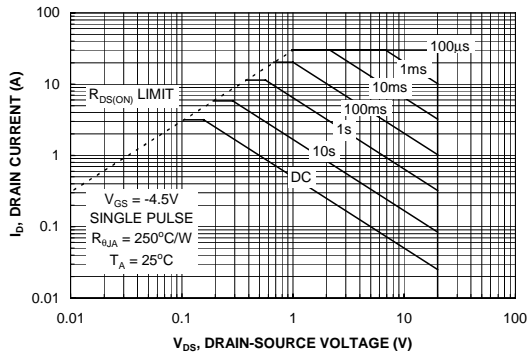


Figure 19. Maximum Safe Operating Area.

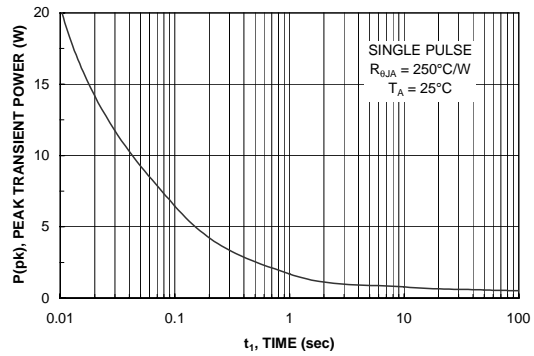


Figure 20. Single Pulse Maximum Power Dissipation.

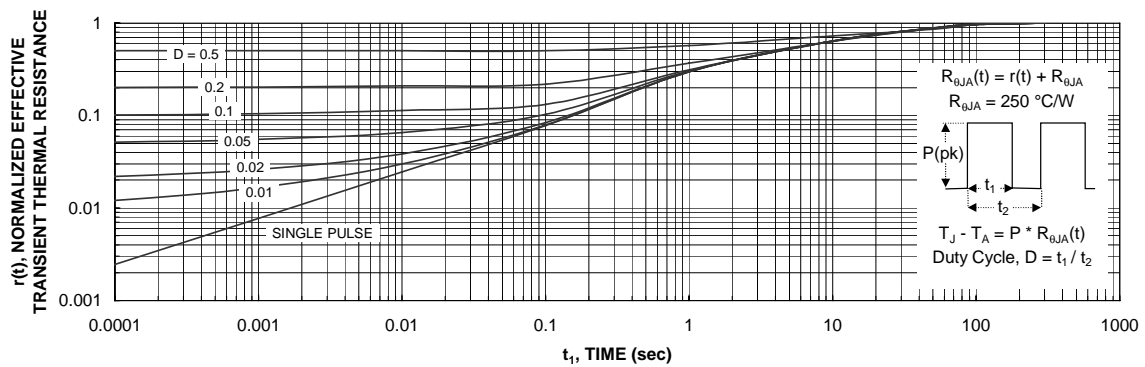


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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