

MOSFET - N-Channel, POWERTRENCH®

80 V, 80 A, 4.5 m Ω

FDWS86368-F085

Features

- Typical $R_{DS(on)} = 3.7 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- Typical $Q_{g(tot)} = 57 \text{ nC}$ at $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- UIS Capability
- Wettable Flanks for Automatic Optical Inspection (AOI)
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS (T_J = 25°C, Unless otherwise noted)

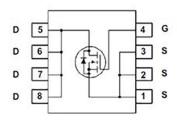
Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-to-Source Voltage	80	V
V _{GS}	Gate-to-Source Voltage	±20	V
I _D	Drain Current (T _C = 25°C) Continuous (V _{GS} = 10 V) (Note 1) Pulsed	80 (See Figure 4)	Α
E _{AS}	Single Pulse Avalanche Energy (Note 2)	82	mJ
P _D	Power Dissipation	214	W
	Derate Above 25°C	1.43	W/°C
TJ, T _{STG}	Operating and Storage Temperature	-55 to +175	°C
Rejc	Thermal Resistance, Junction to Case	0.7	°C/W
ReJA Maximum Thermal Resistance, Junction to Ambient (Note 3)		50	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Current is limited by bondwire configuration.
- 2. Starting $T_J = 25^{\circ}$ C, $\dot{L} = 40 \,\mu$ H, $I_{AS} = 64 \,$ A, $V_{DD} = 80 \,$ V during inductor charging and $V_{DD} = 0 \,$ V during time in avalanche.
- 3. ReJA is the sum of the junction–to–case and case–to–ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. ReJC is guaranteed by design, while ReJA is determined by the board design. The maximum rating presented here is based on mounting on a 1 in pad of 2 oz copper.

V _{DSS}	R _{DS(ON)} MAX	I _D MAX
80 V	4.5 mΩ @ 10 V	80 A

ELECTRICAL CONNECTION



N-Channel MOSFET



MARKING DIAGRAM



A = Assembly Location Y = Year

WW = Work Week
WL = Assembly Lot
FDWS = Device Code
86368 = Device Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
FDWS86368-F085	DFNW8 (Power56) (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications,

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

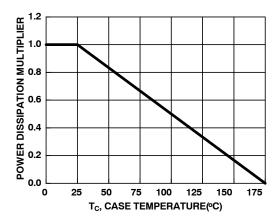
Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Units
OFF CHAF	ACTERISTICS				•	•	•
B _{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		80			٧
I _{DSS} Drain-to-Source Leakage Current		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 25°C				1	μΑ
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 175°C (Note 4)				1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V				±100	nA
ON CHAR	ACTERISTICS					•	
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$		2.0	3.0	4.0	V
R _{DS(on)}	Drain to Source On Resistance	e I _D = 80 A, V _{GS} = 10 V, T _J = 25°C			3.7	4.5	mΩ
		I _D = 80 A, V _{GS} = 10 V, T _J = 175°C (Note 4)			7.4	9.0	1
OYNAMIC	CHARACTERISTICS				•	•	
C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz			4350		pF
C _{oss}	Output Capacitance				636		pF
C _{rss}	Reverse Transfer Capacitance				20		pF
R _g	Gate Resistance	f = 1 MHz			2.5		Ω
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V	V _{DD} = 64 V, I _D = 80 A		57	75	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V			8		nC
Q_{gs}	Gate-to-Source Gate Charge				23		nC
Q _{gd}	Gate-to-Drain "Miller" Charge				11		nC
WITCHIN	G CHARACTERISTICS						
t _{on}	Turn-On Time	$V_{DD} = 40 \text{ V}, I_D = 80 \text{ A},$	V_{GS} = 10V, R_{GEN} = 6 Ω			60	ns
t _{d(on)}	Turn-On Delay				23		ns
t _r	Rise Time				22		ns
t _{d(off)}	Turn-Off Delay				32		ns
t _f	Fall Time				13		ns
t _{off}	Turn-Off Time					59	ns
PRAIN-SC	OURCE DIODE CHARACTERISTI	cs					
V _{SD}	Source-to-Drain Diode Voltage	V _{GS} = 0 V, I _{SD} = 80 A V _{GS} = 0 V, I _{SD} = 40 A				1.25 1.2	V
t	Reverse-Recovery Time	$I_F = 80 \text{ A}, \ \Delta I_{SD}/\Delta t = 100 \text{ A/}\mu\text{s}, \ V_{DD} = 64 \text{ V}$			58	75	ns
Q _{rr}	Reverse-Recovery Charge				49	67	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product

performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. The maximum value is specified by design at $T_J = 175^{\circ}$ C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

200



V_{GS} = 10V 175 BY PACKAGE ₹ 150 CURRENT LIMITED ID, DRAIN CURRENT 125 100 75 50 25 75 100 125 150 175 T_C, CASE TEMPERATURE(°C) 200 25

CURRENT LIMITED

Figure 1. Normalized Power Dissipation vs. **Case Temperature**

Figure 2. Maximum Continuous Drain Current vs. Case Temperature

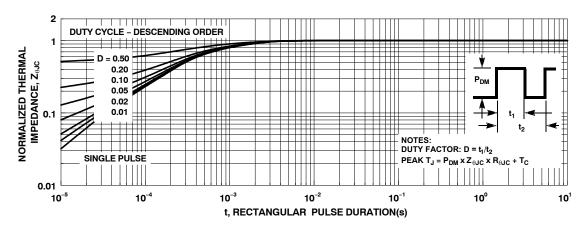


Figure 3. Normalized Maximum Transient Thermal Impedance

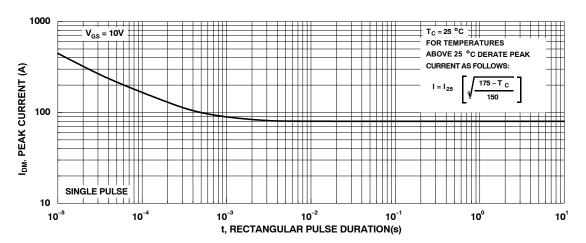


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

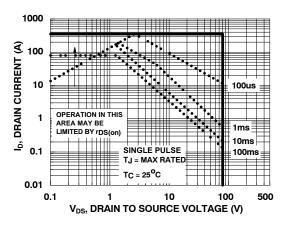


Figure 5. Forward Bias Safe Operating Area

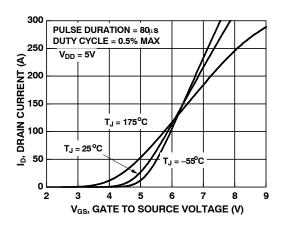


Figure 7. Transfer Characteristics

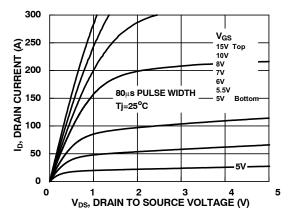
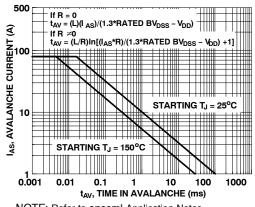


Figure 9. Saturation Characteristics



NOTE: Refer to **onsemi** Application Notes <u>AN7514</u> and <u>AN7515</u>

Figure 6. Unclamped Inductive Switching Capability

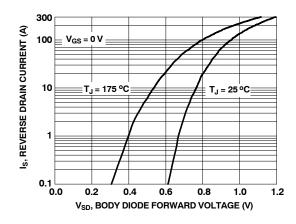


Figure 8. Forward Diode Characteristics

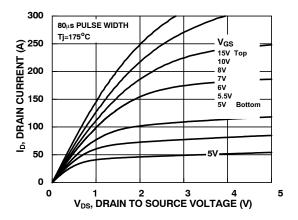


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

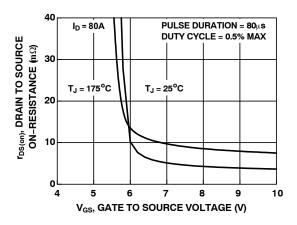


Figure 11. R_{DSON} vs. Gate Voltage

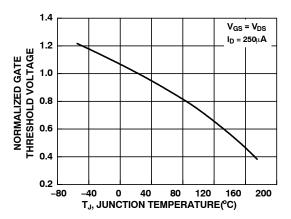


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

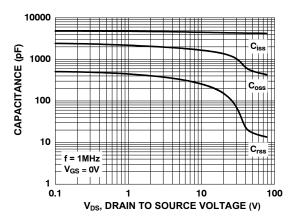


Figure 15. Capacitance vs. Drain to Source Voltage

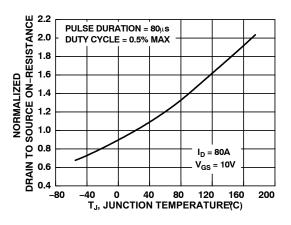


Figure 12. Normalized R_{DSON} vs. Junction Temperature

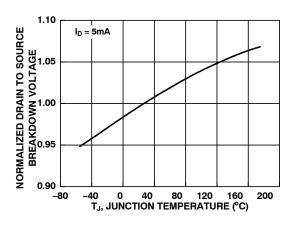


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

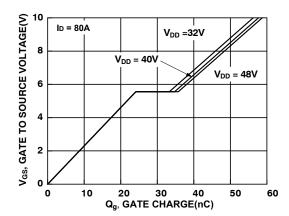
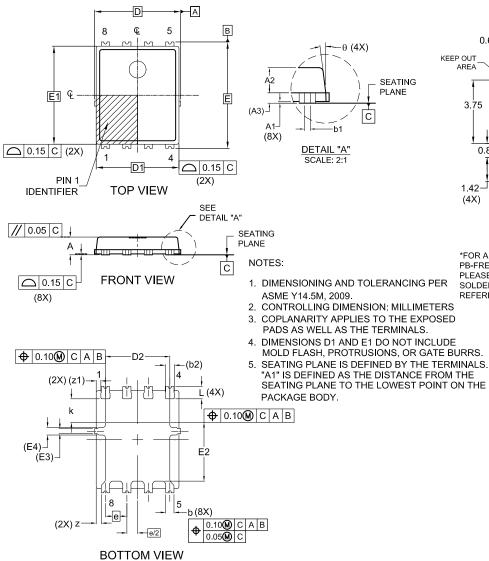
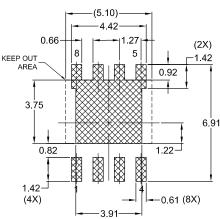


Figure 16. Single Pulse Maximum Power Dissipation

PACKAGE DIMENSIONS

DFNW8 5.2x6.3, 1.27PCASE 507AU ISSUE A





LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRIMD.

DIM	MILLIMETERS			
Diwi	MIN.	NOM.	MAX.	
Α	0.90	1.00	1.10	
A1	-	•	0.05	
A2	0.65	0.75	0.85	
A3	0.30 REF			
b	0.47	0.52	0.57	
b1	0.13	0.18	0.23	
b2	(0.54)			
D	5.00	5.10	5.20	
D1	4.80	4.90	5.00	
D2	3.72	3.82	3.92	
Е	6.20	6.30	6.40	
E1	5.70	5.80	5.90	
E2	3.38	3.48	3.58	
E3	-	0.30 REF	-	
E4	0.45 REF			
е	1.27 BSC			
e/2	0.635BSC			
k	1.30	1.40	1.50	
L	0.64	0.74	0.84	
z	0.24	0.29	0.34	
z1	(0.28)			
θ	0°		12°	

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