FAIRCHILD SEMICONDUCTOR®

July 2009

FDZ371PZ

P-Channel 1.5 V Specified PowerTrench® Thin WL-CSP MOSFET
-20 V, -3.7 A, 75 mΩ

Features

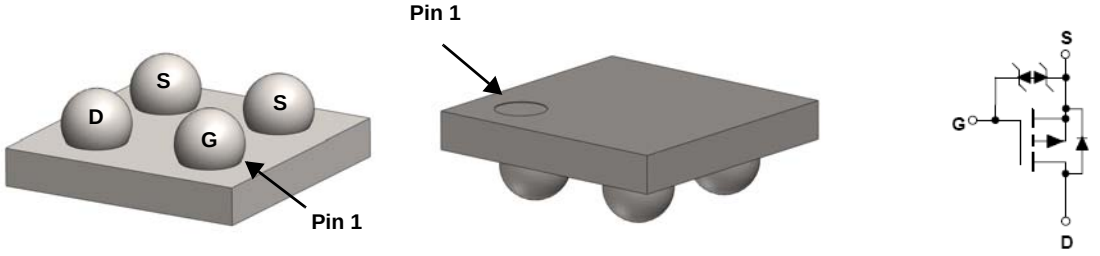
- Max $r_{DS(on)}$ = 75 mΩ at V_{GS} = -4.5 V, I_D = -2.0 A
- Max $r_{DS(on)}$ = 90 mΩ at V_{GS} = -2.5 V, I_D = -1.5 A
- Max $r_{DS(on)}$ = 110 mΩ at V_{GS} = -1.8 V, I_D = -1.0 A
- Max $r_{DS(on)}$ = 150 mΩ at V_{GS} = -1.5 V, I_D = -1.0 A
- Occupies only 1.0 mm^2 of PCB area.Less than 30% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.4 mm height when mounted to PCB
- HBM ESD protection level >4.4kV typical (Note 3)
- RoHS Compliant

General Description

Designed on Fairchild's advanced 1.5 V PowerTrench® process with state of the art "fine pitch" Thin WLCSP packaging process, the FDZ371PZ minimizes both PCB space and $r_{DS(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{DS(on)}$.

Applications

- Battery management
- Load switch
- Battery protection



BOTTOM **TOP**

WL-CSP 1.0X1.0 Thin

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-20	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	-Continuous	T_A = 25°C	(Note 1a)	-3.7	A
	-Pulsed			-12	
P_D	Power Dissipation	T_A = 25°C	(Note 1a)	1.7	W
	Power Dissipation	T_A = 25°C	(Note 1b)	0.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	260	

Package Marking and Ordering Information

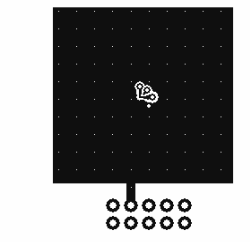
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
K	FDZ371PZ	WL-CSP 1.0X1.0 **Thin**	7 ”	8 mm	5000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

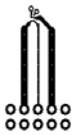
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.35	-0.6	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -2.0 A		55	75	mΩ
		V_{GS} = -2.5 V, I_D = -1.5A		65	90	
		V_{GS} = -1.8 V, I_D = -1.0 A		80	110	
		V_{GS} = -1.5 V, I_D = -1.0 A		100	150	
		V_{GS} = -4.5 V, I_D = -2.0 A, T_J =125°C		80	124	
g_{FS}	Forward Transconductance	V_{DD} = -5 V, I_D = -3.3 A		14		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz		750	1000	pF
C_{oss}	Output Capacitance			110	145	pF
C_{rss}	Reverse Transfer Capacitance			100	150	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10 V, I_D = -3.3 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		5.9	12	ns
t_r	Rise Time			9.1	18	ns
$t_{d(off)}$	Turn-Off Delay Time			124	198	ns
t_f	Fall Time			88	140	ns
Q_g	Total Gate Charge	V_{GS} = -4.5 V, V_{DD} = -10 V, I_D = -3.3 A		12	17	nC
Q_{gs}	Gate to Source Charge			1.1		nC
Q_{gd}	Gate to Drain “Miller” Charge			3.4		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.1	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.3 A (Note 2)		-0.7	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -3.3 A, di/dt = 100 A/μs		61	98	ns
Q_{rr}	Reverse Recovery Charge			29	47	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 75 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 260 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

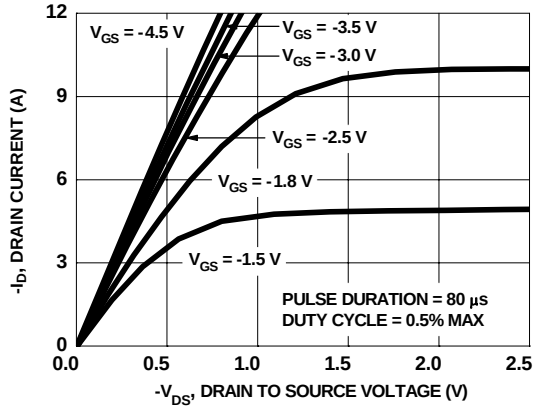


Figure 1. On-Region Characteristics

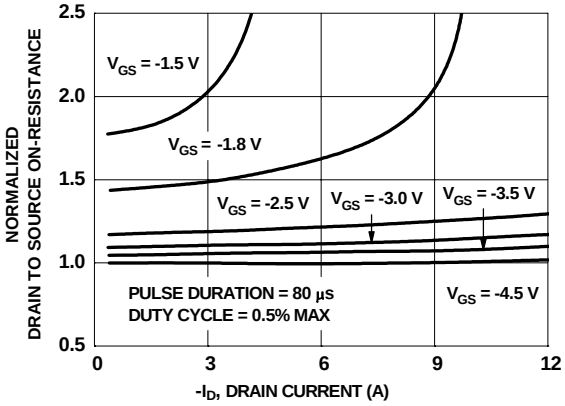


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

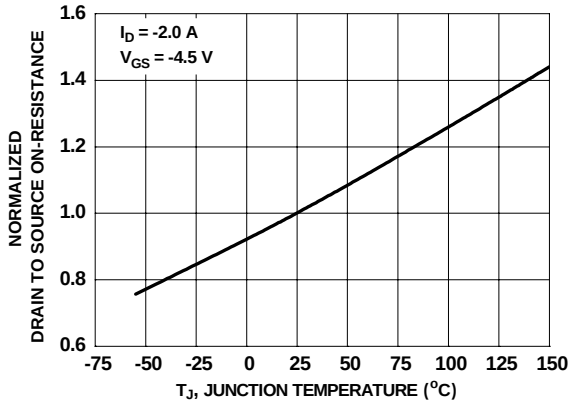


Figure 3. Normalized On-Resistance vs Junction Temperature

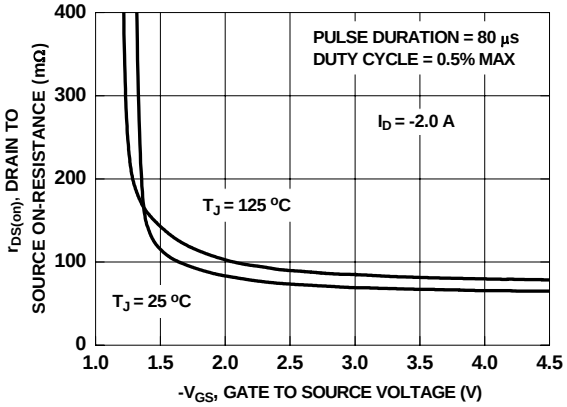


Figure 4. On-Resistance vs Gate to Source Voltage

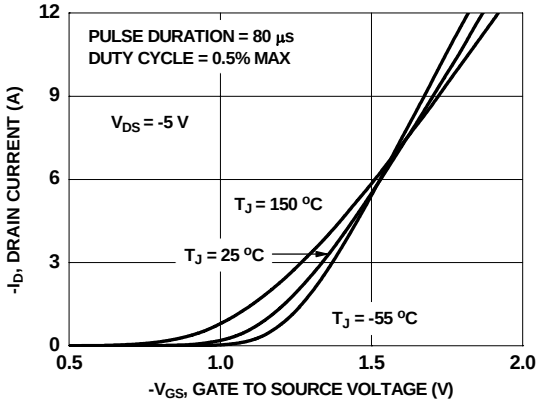


Figure 5. Transfer Characteristics

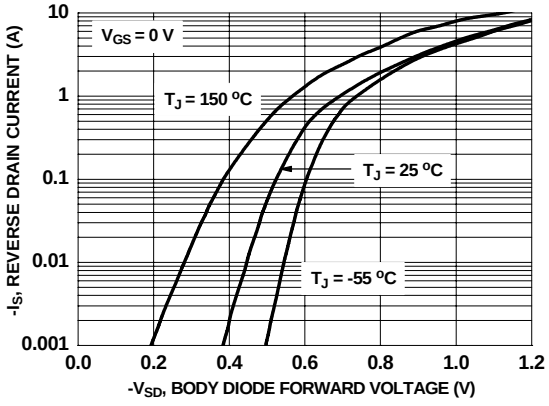


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

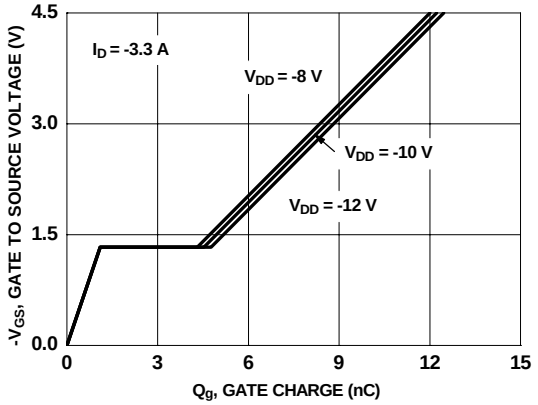


Figure 7. Gate Charge Characteristics

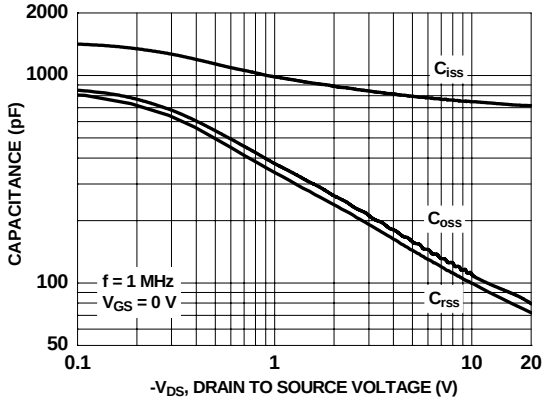


Figure8. Capacitance vs Drain to Source Voltage

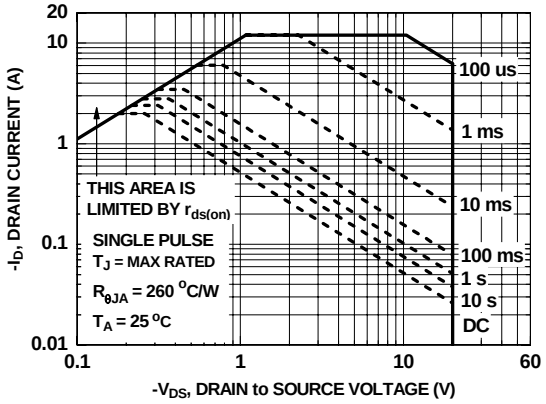


Figure 9. Forward Bias Safe Operating Area

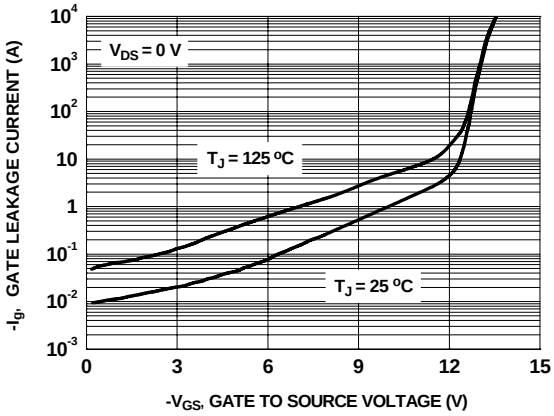


Figure 10. Gate Leakage Current vs Gate to Source Voltage

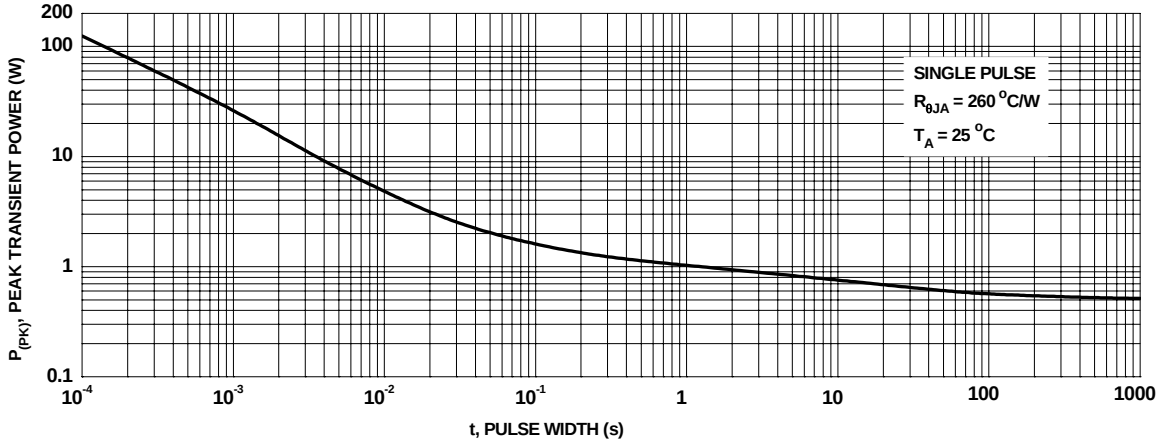


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

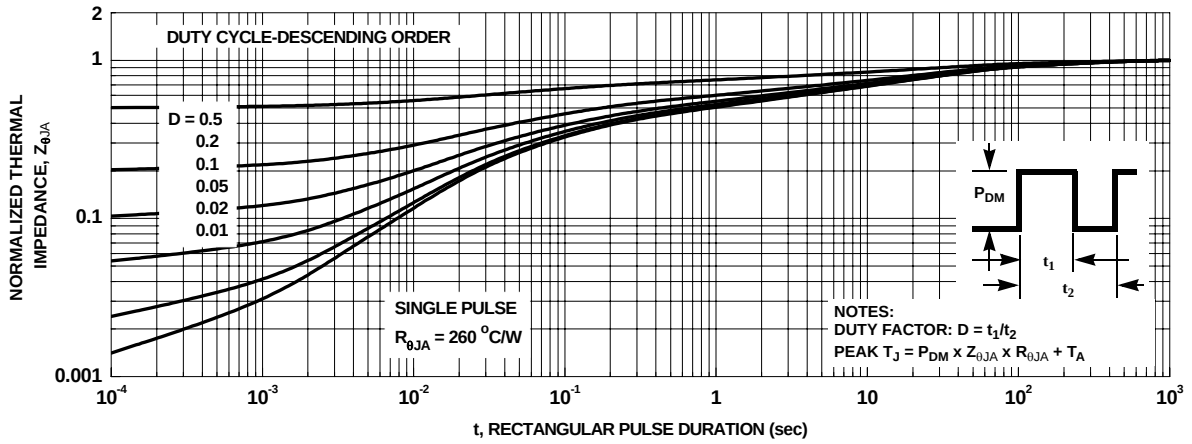
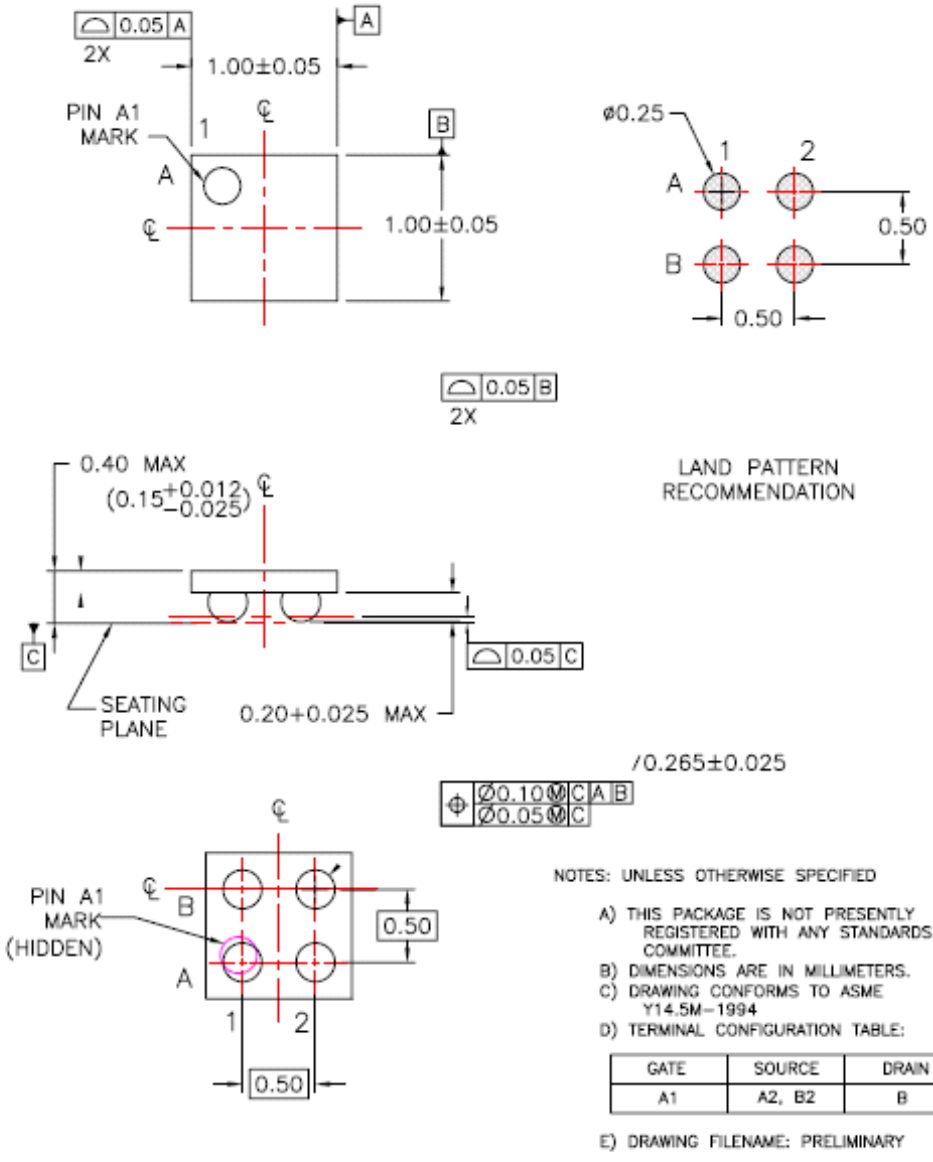


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

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C) DRAWING CONFORMS TO ASME Y14.5M–1994
D) TERMINAL CONFIGURATION TABLE:

GATE	SOURCE	DRAIN
A1	A2, B2	B

E) DRAWING FILENAME: PRELIMINARY

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