8CH 24-Bit ΣΔADC, 4x20 LCM and 8-bit Microcontroller

- 2.4V to 3.6V operation voltage range
- Single 24-bit High-precision Sigma-Delta ADC
- 8-bit CISC architecture microcontroller
  - 8051 compatible instruction set
  - 1T execution core
  - 3x32-bit timer/counter, 2CH/counter
  - 4 Instruction sources
- 4Kx16 Bytes MTP with 32-word Information data
- Advanced multi-mode power management
- Support multi-clock sources
  - Internal 12MHz HSRC
  - Internal 32KHz LSRC
  - External crystal oscillator
- System manager controller
- External vector interrupts for interrupt controller
- Real-time clock with programmable alarm control
- 4X20 LCD Module driver
  - 1/4 duty, 1/3 bias or 1/2bias
- On-chip peripherals
  - 8CH Fully differential ADC I/O Channels
  - Integrated temperature sensor
  - Power supply monitoring
  - Internal power-on reset
  - Auxiliary hardware reset
  - Dual IDAC current sources
  - UART/SPI/I2C communication interface
- Analog peripheral function
  - Excitation current DAC
  - Rail-to-rail comparator
  - Hysteresis comparator
  - LVD and LVR functions
  - Rail-to-rail operational amplifier
- 32 GPIOs with multi-Configurable modes
  - Digital input mode
  - Push-pull output mode
  - Open-drain mode
  - Internal pull-up mode
  - Analog input mode
  - High-impedance mode
- Multi-function ALU (MFA)
- -40 ~ 85℃ operation temperature
- Package Type
  - LQFP48-7x7 package
  - TSSOP-24L
  - TSSOP-28L

Applications

- Instrumentation signal measurements
- Temperature measurements
- Gas detectors and Smoke detectors
- Weigh scale facilities
- Pressure measurements
- Industrial system controller
- Smart Home sensor analog front-end controller
- Home appliance sensor signal processor

Description

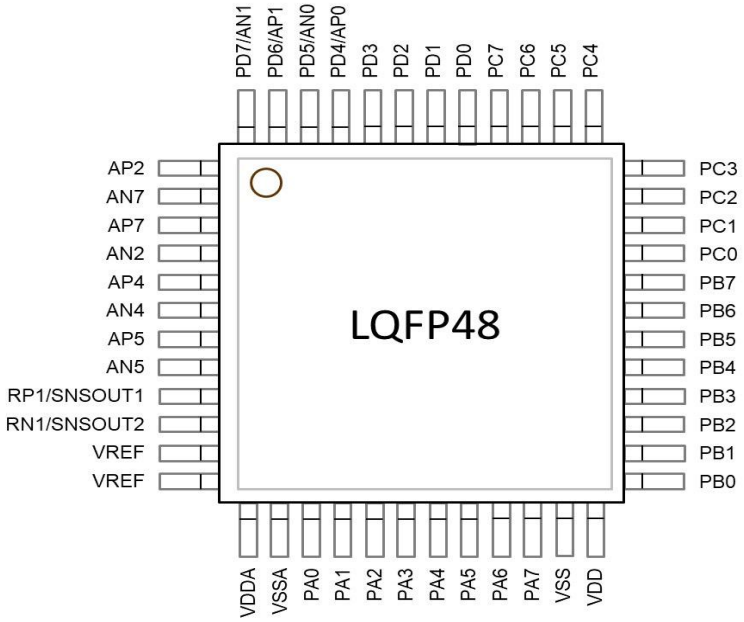
ESMT FE8116x series is a general purpose 8051 platform that targets on various consumer applications. The MCU platform is integrated with an 8051 core running up to 12MHz, up to 4K-word MTP program memory, 32-word data memory and up to 1K-byte data SRAM (x-ram) with 256-byte internal-SRAM (i-ram). The MCU platform is also integrated with rich peripherals support, including real-time clock (RTC), watchdog timer controller (WDT), timer controller (TMR), UART interface controller (UART), I2C serial interface controller (I2C), serial peripheral interface controller (SPI), 24-bit high resolution delta-sigma ADC (SDM), analog controller (ANAC), STN LCD driver (LCM), and multi-function ALU (MFA).

Pin Function Description

Pin Name	Pin No.	I/O	DESCRIPTION
PD4	45	I/O	LCM COM3/CH0+ signal terminal input/GPIO Port D.4
PD5	46	I/O	LCM COM2/CH0- signal terminal input/GPIO Port D.5
PD6	47	I/O	LCM COM1/CH1+ signal terminal input/GPIO Port D.6
PD7	48	I/O	LCM COM0/CH1- signal terminal input/GPIO Port D.7
AP2, AN2	1,2	I	Differential CH2+/CH2- signal input
AP7,AN7	3,4	I	Differential CH7+/CH7- signal input
AP4,AN4	5,6	I	Differential CH4+/CH4- signal input
AP5,AN5	7,8	I	Differential CH5+/CH5- signal input
RP1/SNSOUT1	9	I/O	CH6+ terminal input/CH1+ reference input/IDACx output
RN1/SNSOUT2	10	I/O	CH6- terminal input/CH1- reference input/IDACx output
RP0,RN0	11,12	I	Differential CH0+/CH0- reference signal input
VDDA	13	P	Internal LDO output connection
VSSA	14	G	Internal LDO ground connection
PA0	15	I/O	GPIO Port A.0/SPI MISO
PA1	16	I/O	GPIO Port A.1/SPI MOSI
PA2	17	I/O	GPIO Port A.2/SPI clock/Interrupt 3
PA3	18	I/O	GPIO Port A.3/SPI SS/Interrupt 2
PA4	19	I/O	GPIO Port A.4/I2C data
PA5	20	I/O	GPIO Port A.5/I2C clock/Interrupt 1
PA6	21	I/O	GPIO Port A.6/UART RX
PA7	22	I/O	GPIO Port A.7/UART TX
VSS	23	G	Ground terminal
VDD	24	P	Power terminal
PB0	25	I/O	GPIO Port B.0/LCD SEG19/Hardware Reset
PB1	26	I/O	GPIO Port B.1/LCD SEG18/External Crystal oscillator output
PB2	27	I/O	GPIO Port B.2/LCD SEG17/External Crystal oscillator input
PB3	28	I/O	GPIO Port B.3/LCD SEG16/Interrupt 0
PB4	29	I/O	GPIO Port B.4/LCD SEG15/PWM0
PB5	30	I/O	GPIO Port B.5/LCD SEG14/PWM1
PB6	31	I/O	GPIO Port B.6/LCD SEG13/PWM2
PB7	32	I/O	GPIO Port B.7/LCD SEG12/PWM3
PC0	33	I/O	GPIO Port C.0/LCD SEG11/PWM4
PC1	34	I/O	GPIO Port C.1/LCD SEG10/PWM5
PC2	35	I/O	GPIO Port C.2/LCD SEG9/OCD Data/nCTS
PC3	36	I/O	GPIO Port C.3/LCD SEG8/OCD Clock/nRTS

Pin Name	Pin No.	I/O	DESCRIPTION
PC4	37	I/O	GPIO Port C.4/LCD SEG7/ISP Data
PC5	38	I/O	GPIO Port C.5/LCD SEG6/ISP Clock
PC6	39	I/O	GPIO Port C.6/LCD SEG5/COMP+ input terminal
PC7	40	I/O	GPIO Port C.7/LCD SEG4/COMP- input terminal
PD0	41	I/O	GPIO Port D.0/LCD SEG3/Capture0
PD1	42	I/O	GPIO Port D.1/LCD SEG2/Capture1/OPAMP- input terminal
PD2	43	I/O	GPIO Port D.2/LCD SEG1/Capture 2/OPAMP+ input terminal
PD3	44	I/O	GPIO Port D.3/LCD SEG0/Capture3/OPAMP Output terminal

Package Outline and Pin Configuration

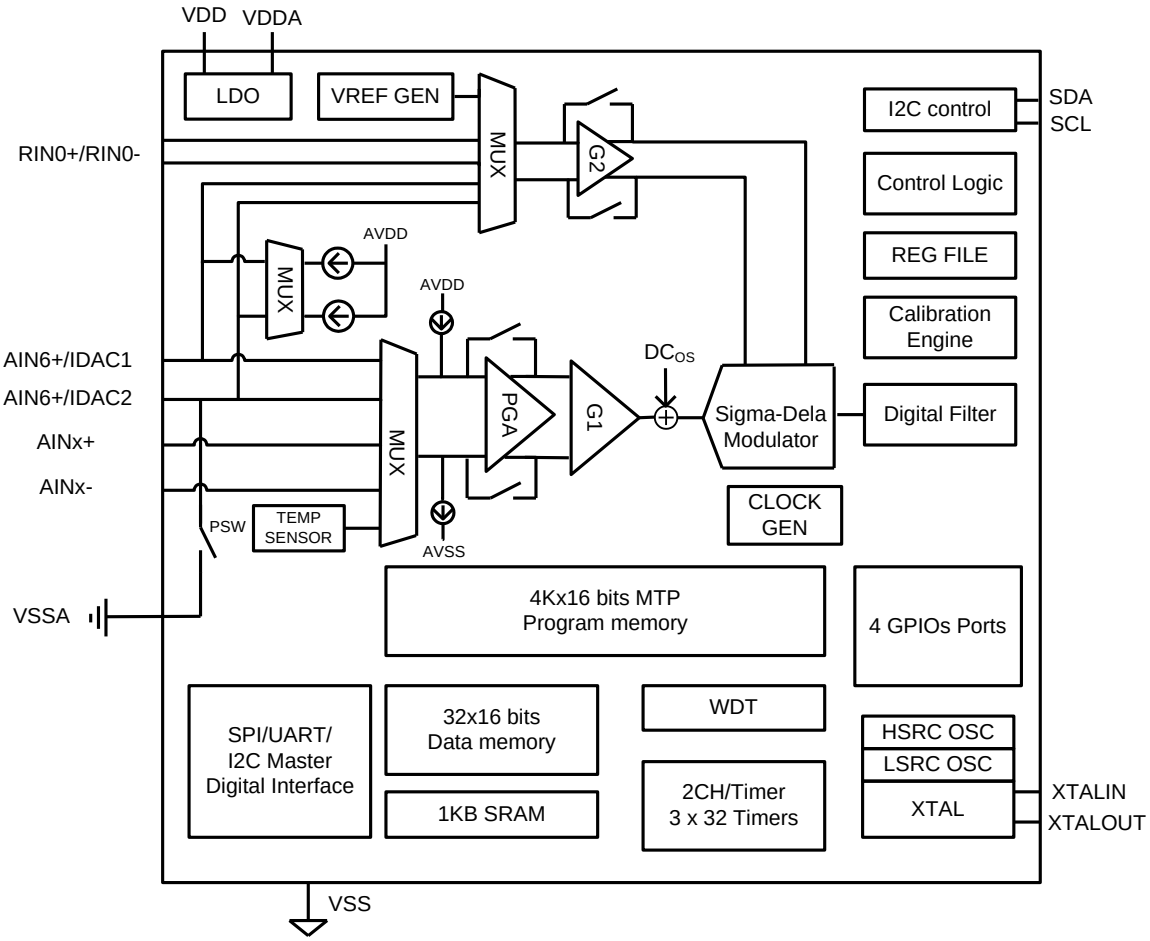


Topside view of FE81160

Ordering Information

Product ID	Package Type	Packing	Comments
FE81160	LQFP48	3000 Units/Reel	Green
FE81161	TSSOP24	3000 Units/Reel	Green
FE81162	TSSOP28	3000 Units/Reel	Green

Functional Block Diagram



Absolute Maximum Rating

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage	VDD to VSS	-0.3	4.0	V
VDDA	Regulator voltage	VDDA to VSSA	-0.3	4.0	V
V_{AIN}	Analog Input voltage	AIPx*1, AINx*1	-0.3	VDD+0.3	V
V_{RIN}	Reference Input voltage	RIP0, RIN0, VCM		VDD+0.3	
V_{IO}	Digital I/O ports	PAy*2, PBy*2, PCy*2, PDy*2	-0.3	VDD+0.3	V
T_A	Operating ambient temperature range		-40	85	°C
T_J	Maximum junction temperature		–	150	°C
T_{stg}	Storage temperature range		-55	150	°C
ESD	Human Body Model		±2k		V
	Charged Device Model		±500		

*1 x stands for 0~6

*2 y stands for 0~7

Recommended Operating Conditions

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage	VDD to VSS	2.4	3.6	V
V_{AIN}	Analog Input voltage	AIPx[*1], AINx[*1], RIPx, RINx,VCM	2.4	3.6	V
V_{IO}	Digital I/O ports	PAy[*2], PBy[*2], PCy[*2], PDy[*2]	2.4	3.6	V
RC_{OSC}	Internal RC clock oscillator		8	12	MHz
$XTAL_{OSC}$	External XTAL oscillator		4	12	MHz

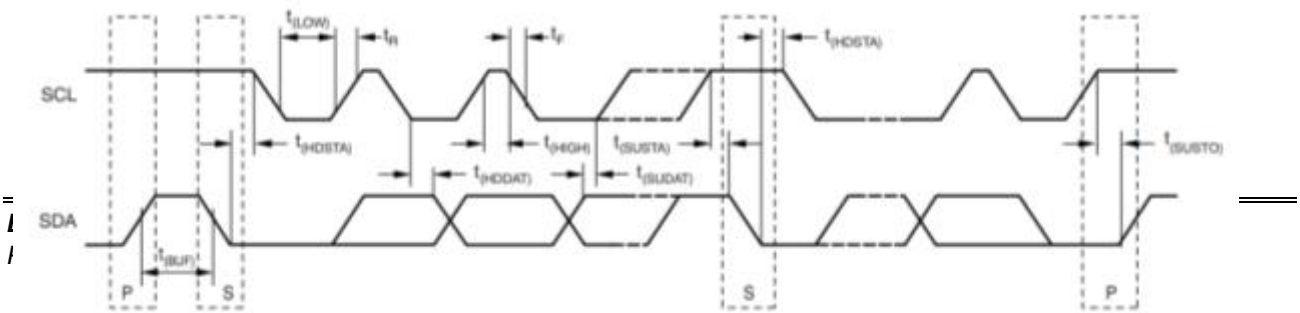
I2C Digital Communication Timing Diagrams

SYMBOL	CONDITION	MIN	MAX	UNIT
f_{SCL}	SCL operating frequency	2.5	—	us
f_{BUF}	Bus free time between STOP and START	1.3	—	us
t_{HDSTA}	Hold time after repeated START condition.	600	—	ns
t_{SUSTA}	Repeated START condition setup time	600	—	ns
t_{SUSTO}	STOP condition setup time	600	—	ns
t_{HDDAT}	Data hold time (*2)	0	—	ns
t_{HSUDAT}	Data setup time	100	—	ns
t_{LOW}	SCL clock low period	1300	—	ns
t_{HIGH}	SCL clock high period	600	—	ns
t_{VDAT}	Data valid time (*3)	—	900	ns
t_{FDA}	Data fall time	—	300	ns
t_R	Clock rise time	—	300	ns
t_F	Clock fall time	—	300	ns
Time out	Clock fall time	100	—	ms
$t_{RCClock/data}$	rise time for SCL=100KHz	—	1	us

(*1) The host and device have the same VDD voltage. The voltages are based on statisctical analysis of samples tested during initial release.

(*2) The maximum t_{HDDAT} can be 0.9us for fast mode, and is less than the maximum t_{VDAT} by a transition time.

(*3) t_{VDAT}=time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worst). = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).



Electrical Characteristics

- VDD=3.3V, at T_A=-40 ~ 85°C, unless otherwise noted

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
VDD	Supply voltage	Normal operation		2.2	–	3.6	V
$I_{Q,NORMAL}$	Quiescent supply	Normal mode	12MHz	–	5.3	200	mA
			8MHz	–	3.9	–	
$I_{Q,SLOW}$		Slow mode		–	1.2	150	mA
$I_{Q,WAIT}$		Wait mode		–	2.2	–	mA
$I_{Q,SWAIT}$		Slow wait mode		–	616	–	uA
$I_{Q,HALT}$		Halt mode		–	29	–	uA
$I_{Q,SD}$		Shutdown mode		–	–	10	uA
General Purpose I/O ports							
V_{IH}	Logic input Hi threshold	VDD = 3.3V		0.7VDD	–	–	V
V_{IL}	Logic input Lo threshold	VDD = 3.3V		–	–	0.3VDD	V
R_{PU}	Internal pull up resistor	VDD = 3.3V		5.0	8.5	12	KΩ
I_{LEAK}	Leakage current			–	–	1	uA
V_{OH}	Hi-level logic output	I_{OUT} = -6mA		VDD-0.3	–	–	V
V_{OL}	Lo-level logic output	I_{OUT} = +6mA		–	–	0.3	V
F_{OUT}	Port output frequency	C_L = 20pF, R_L = 1KΩ		–	3	–	MHz
F_{IN}	Port input frequency			–	12	–	MHz
I_{SOURCE}	I/O ports sourcing current	VDD=3.3V, V_{OH}=0.9VDD		–	18	–	mA
I_{SINK}	I/O port sinking current			–	25	–	mA
Power-on Reset							
V_{POR}	POR threshold voltage	$dV_{DD}/dt \leqq 3.3V/s$		1.2	1.45	1.7	V
T_{POR}	POR trigger delay time	$dV_{DD}/dt > 3.3V/s$		30	50	100	us
Supply Voltage Supervisor							
V_{LVD}	LVD threshold voltage	LVD[2:0]=000		V_{LVD}-5%	3.0	V_{LVD}+5%	V
		LVD[2:0]=001			2.8		V
		LVD[2:0]=010			2.6		V
		LVD[2:0]=011			2.4		V
		LVD[2:0]=100			2.2		V
		LVD[2:0]=101			1.0		V
		LVD[2:0]=110			1.8		V
V_{LVR}	LVR threshold voltage	LVR[1:0]=00		V_{LVR}-5%	2.6	V_{LVR}+5%	V
		LVR[1:0]=01			2.4		V
		LVR[1:0]=10			2.2		V
		LVR[1:0]=11			2.0		V
T_{LVD}	LVD trigger delay time	VDD=3.3V → V_{LVD} threshold voltage		70	105	140	us
T_{LVR}	LVR trigger delay time	VDD=3.3V → V_{LVR} threshold voltage		150	210	270	us

I_{LVD}	LVD quiescent current	VDD=3.3V		6	9.5	13	uA
I_{LVR}	LVR quiescent current	VDD=3.3V		6	9.5	13	uA
Clock System							
I_{LSRC}	LSRC quiescent current	VDD=3.3V		—	1	2.5	uA
F_{HSRC}	HSRC clock oscillator	FSET=0	V_{DD}=3.3V, 25℃	-1%	12	+1%	MHz
			V_{DD}=3.3V, -40~85℃	-2%		+2%	
		FSET=1	V_{DD}=3.3V, 25℃	-1%	8	+1%	MHz
			V_{DD}=3.3V, -40~85℃	-2%		+2%	
TC_{HSRC}	HSRC Temperature coef.			—	400	—	KHz
F_{LSRC}	LSRC clock oscillator			24	32	40	KHz
T_{WAKEUP}	HSRC stable time				1024		clocks
SD24, Sigma-Delta Modulator							
VDDA	Analog power supply			2.2	—	3.6	V
I_{ADC}	SD24 quiescent current	V_{DD}=3.3V, ENADC=1		150	200	350	uA
f_{SAMP}	SD24 sampling clock	f_{MCLK}=8MHz		31.25	250	1000	KHz
V_{FSR}	Diff. input voltage range			$-V_{REF}/G_{PGA}$	—	V_{REF}/G_{PGA}	V
Z_{IN}	Input Impedance	f_{SAMP}=250KHz			—	2	MΩ
V_{ICM}	Input Common-mode voltage			V_{SS}	—	V_{LDO}-0.9	V
G_{ADC}	Digital gain	ADCGN[3:0]		1,2,4,8,16			V/V
G_{TOTAL}	Total signal gain			1 ~ 2048			V/V
GV_{REF}	Reference voltage ratio	VRGN[1:0]		1, 1/2,3/4,1/4			V/V
V_{DCOS}	Input offset	DCSET[2:0]		1/16~7/16V_{REF}			V
PSRR	Power supply reject ratio						
CMRR	Common mode reject ratio						
E_{GAIN}	Gain error						
NRES	Resolution			—	—	24	bits
ENOB	Effective number of bits	V_{REF}=1.2V, PGA=1,ODR=2Hz		—	20	—	bits
NFB	Noise free bits	V_{REF}=1.2V, PGA=1,ODR=2Hz		—	18	—	bits
ODR	SD24 Output data rate			—	—	1000	Hz
$VREF_{ADC}$	SD24 reference input voltage	V_{REFP}-V_{REFN}		0	—	V_{LDO}	V
PGA Amplifier							
V_{CM_PGA}	PGA input common-mode voltage			0.4	—	V_{LDO}-0.8	V
G_{PGA}	PGA gain	PGAGN[2:0]		1,2,4,8,16,32,64,128			V/V
Supply Voltage Monitoring							
$V_{MONITOR}$	VDD monitor supply voltage			2.2	—	3.6	V
$I_{MONITOR}$	VDD monitor quiescent current	VDD=3.3V		3	5	7	uA
$R_{MONITOR}$	VDD monitor ratio			—	1/4	—	V/V
Analog Linear Regulator							
V_{LDO}	LDO supply voltage	VDD=3.3V, No load		2.65	2.85	3.05	V

LD_{LDO}	LDO load regulation	VDD=3.3V, IOUT=10mA	–	0.15	–	%/mA
LN_{LDO}	LDO line regulation		–	0.3	–	%/V
TC_{LDO}	LDO TEMP Coeff.	VDD=3.3V, -40~85℃	–	–	±200	ppm/℃
Temperature Sensor						
VDD_{TS}	TEMP Sensor operation voltage		2.2	–	3.6	V
I_{TS}	TEMP Sensor quiescent current	VDD=3.3V	–	33	45	uA
TEMP	Temperature range		-40	–	125	℃
TC_{TS}	Temperature coefficient	T_A = -40~85℃	–	334	–	uV/℃
TS_{AC}	Temperature accuracy	VDD=2.2~3.6V, T_A = 0~50℃	–	1	–	℃
		VDD=2.2~3.6V, T_A = -40~85℃	–	2.5	–	℃
Rail-Rail Operational Amplifier						
VDD_{OPA}	Comparator operation voltage		2.2	–	3.6	V
I_{OPA}	OPA quiescent current	VDD = 3.3V, T_A=25℃	–	150	250	uA
V_{OS}	Input offset voltage	V_{IN}=0.4~2.0V	-5	1.5	5	mV
V_{CM_RROP}	OPA common mode voltage	VDD = 3.3V, T_A=25℃	VSS	–	VDD	V
SR+	Slew rate in rising	VDD=3.3V, C=100pF,ΔV_{IN}=+500mV	–	0.3	–	V/us
SR-	Slew rate in falling	VDD=3.3V, C=100pF,ΔV_{IN}=-500mV	–	0.3	–	V/us
I_{OH_OPA}	OPA source current	VDD=3.3V, ΔV_{VCM}= -2%	10	–	–	mA
I_{OL_OPA}	OPA sink current	VDD=3.3V, ΔV_{VCM}=+2%	10	–	–	mA
VOUT	OPA output range	VDD=3.3V	0.3	–	VDD-0.3	V
Comparator						
VDD_{CMP}	Comparator Operation voltage		2.2	–	3.6	V
I_{CMPR}	R2R CMP quiescent current	VDD=3.3V	–	95	–	uA
I_{CMPH}	HYS CMP quiescent current	VDD=3.3V	–	9	–	uA
$VREF_{CMPH}$	Internal reference in HYS COMP	VDD=3.3V	-1%	1.2	1%	V
VTH_{CMPR}	Internal reference in R2R COMP	CMPTH[1:0]=00	–	180	–	mV
		CMPTH[1:0]=01	–	260	–	
		CMPTH[1:0]=10	–	350	–	
		CMPTH[1:0]=11	–	430	–	
VCM_{CMPR}	R2R CMP common-mode voltage		0	–	VDD	V
VOS_{CMPR}	R2R CMP offset voltage		–	20	–	mV
VOS_{CMPH}	HYS CMP offset voltage	HYS[2:0]=000	–	1	–	mV
		HYS[2:0]=001	–	5	–	
		HYS[2:0]=010	–	15	–	
		HYS[2:0]=011	–	20	–	
		HYS[2:0]=100	–	25	–	
		HYS[2:0]=101	–	30	–	
		HYS[2:0]=110	–	35	–	
		HYS[2:0]=111	–	40	–	

LCD Controller						
VDD_{LCD}	LCM Operation voltage		2.2	–	3.6	V
I_{LCD}	LCD controller quiescent current	VDD=3.3V	–	1.5	–	uA
I_{LCDBUF}	LCD driver quiescent current	VDD=3.3V	–	10.5	–	uA
CTR_{V2}	V2 Contrast level	VCTR[3:0]=0000~1111	2.2	–	2.64	V
CTR_{V1}	V1 Contrast level	VCTR[3:0]=0000~1111	1.1	–	1.98	V

General Description

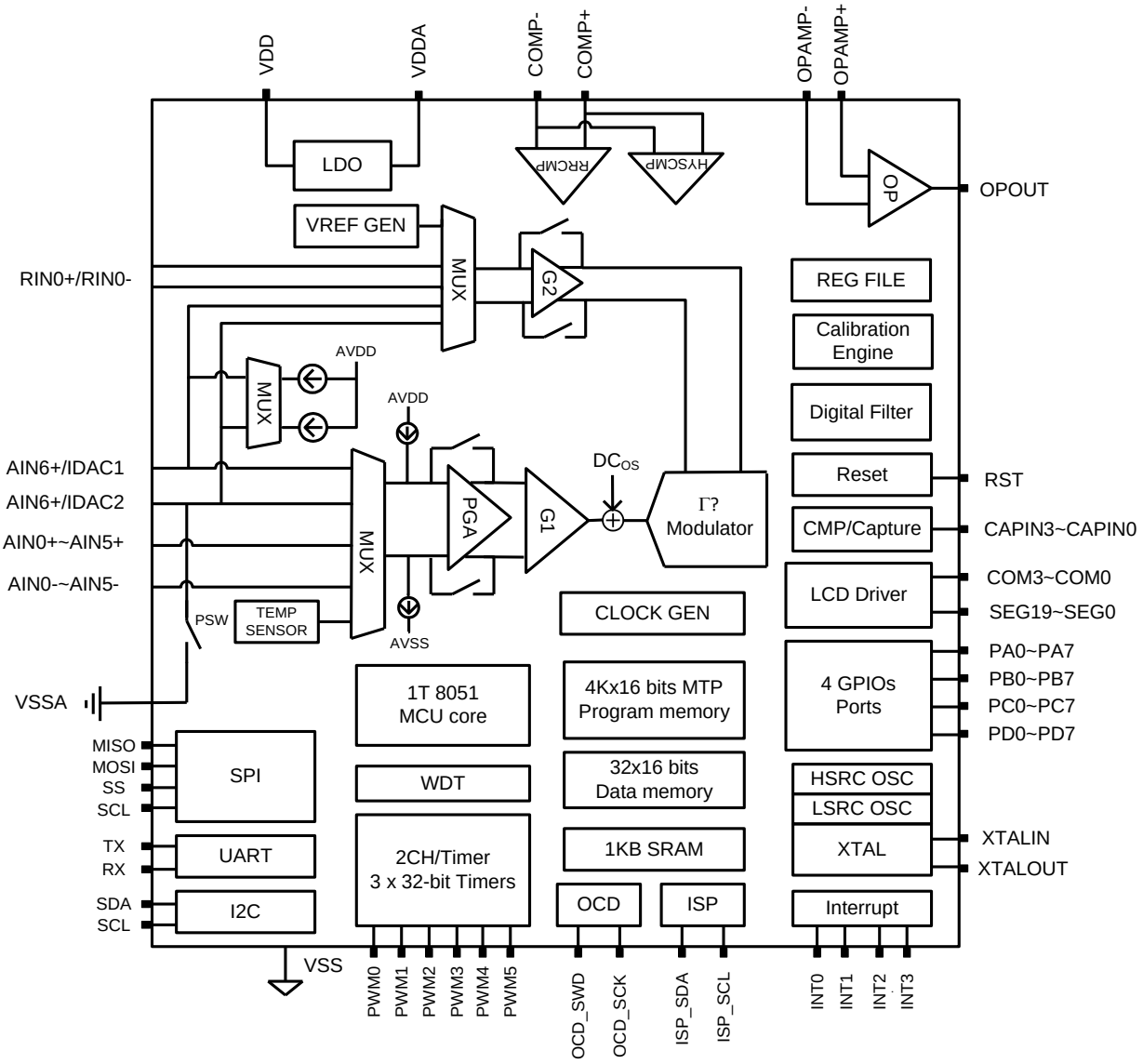
The FE8116x is a 1T execution cycle and 8051 core-based microcontroller. The processor could operate up to 12MHz system clock. It integrates 4Kx16 bit program memory, 32-word data memory and 1KB SRAM on a single chip.

The FE8116x integrated high precision sigma-delta ADC with up to 8 channels and input multiplexer which is flexible adopt low-level analog sensor input signals.

The FE8116x includes single 24-bit sigma-delta ADC with internal reference buffering and PGA amplifier. The ADC incorporates dynamic input differential multiplexing with up to 7 external input channels and 2 internal channels for power supply monitoring and internal on-chip temperature measurement. The ADC includes digital decimation filtering and programmable output data rates which is intended for measurement applications with wide dynamic range and low-frequency signals.

The chip embedded a multi-oscillator system includes 8MHz/12MHz HSRC, 32KHz LSRC and external crystal oscillator. The oscillator clock signals feeds into programmable divider circuits from which the MCU core clock and peripheral clocks are generated. The 8-bit CISC microcontroller is an optimized 1T execution which is compatible with 8051 instruction set. The device embeds a 4Kx16-bit MTP program memory and 32-word data memory. The 1KB SRAM is also provide on chip.

FE8116x incorporates a serial On-Chip Debugging (OCD) and In-System Programming (ISP) interfaces. On-chip factory firmware supports in-circuit serial download and UART debug modes by program development emulator.


VDD
VDDA
COMP-
COMP+
OPAMP-
OPAMP+
LDO
RRCMP
HYSCMP
OP
OPOUT
VREF GEN
MUX
G2
RIN0+/RIN0-
REG FILE
Calibration Engine
Digital Filter
AVDD
MUX
AVDD
AIN6+/IDAC1
AIN6+/IDAC2
AIN0+~AIN5+
AIN0-~AIN5-
DCOS
PGA
G1
Γ? Modulator
Reset
RST
CMP/Capture
CAPIN3~CAPIN0
LCD Driver
COM3~COM0
SEG19~SEG0
MUX
PSW
TEMP SENSOR
AVSS
CLOCK GEN
4 GPIOs Ports
PA0~PA7
PB0~PB7
PC0~PC7
PD0~PD7
VSSA
1T 8051 MCU core
4Kx16 bits MTP Program memory
MISO
MOSI
SS
SCL
SPI
WDT
32x16 bits Data memory
HSRC OSC
LSRC OSC
TX
RX
UART
2CH/Timer 3 x 32-bit Timers
1KB SRAM
XTAL
XTALIN
XTALOUT
SDA
SCL
I2C
OCD
ISP
Interrupt
VSS
PWM0
PWM1
PWM2
PWM3
PWM4
PWM5
OCD_SWD
OCD_SCK
ISP_SDA
ISP_SCL
INT0
INT1
INT2
INT3

Register Map

FMC Control										
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
D000	FMCCTL	FMCEN	INFOEN	ISAVB	—	—	—	—	WDTOF	0x20
D001	FMCCMD	FMCMD								0x00
D002	FMCAD0	FMADDR0								0x00
D003	FMCAD1	FMADDR1								0x00
D004	FMCDA0	FMDATA0								0x00
D005	FMCDA1	FMDATA1								0x00
D006	FMCSTA	BUSY	ECC	—	—	—	—	—	—	0x00
D007	FMCCS0	CKSUM0								0x00
D008	FMCCS1	CKSUM1								0x00

System Management Unit Control (0xE000 ~ 0xE1FF)										
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
E000	DEVID0	DeviceID0								0x00
E001	DEVID1	DeviceID1								0x00
E002	DEVID2	DeviceID2								0x00
E003	DEVID3	DeviceID3								0x00
E004	RSTSRC		LVR		WDT	CPU	CHIP	EXT	POR	0x01
E005	SYSRST					EXTR	CPURH	CPUR	CHIPR	0x00
E006	PRST0	UARTR	I2CR		RTCR		LCMR	ANAR	SDMR	0x00
E007	PRST1			CAPR	MFAR	SPIR	TMR2R	TMR1R	TMR0R	0x00
E008	PACTL0	PA7CTL0	PA6CTL0	PA5CTL0	PA4CTL0	PA3CTL0	PA2CTL0	PA1CTL0	PA0CTL0	0x0F
E009	PACTL1	PA7CTL1	PA6CTL1	PA5CTL1	PA4CTL1	PA3CTL1	PA2CTL1	PA1CTL1	PA0CTL1	0x0F
E00C	PAMS0	PA7MS0	PA6MS0	PA5MS0	PA4MS0	PA3MS0	PA2MS0	PA1MS0	PA0MS0	0x00
E00D	PAMS1	PA7MS1	PA6MS1	PA5MS1	PA4MS1	PA3MS1	PA2MS1	PA1MS1	PA0MS1	0x00
E00E	PAMS2	PA7MS2	PA6MS2	PA5MS2	PA4MS2	PA3MS2	PA2MS2	PA1MS2	PA0MS2	0x00
E017	PAMSK	PA7MSK	PA6MSK	PA5MSK	PA4MSK	PA3MSK	PA2MSK	PA1MSK	PA0MSK	0X00
E018	PAOUT	PA7OUT	PA6OUT	PA5OUT	PA4OUT	PA3OUT	PA2OUT	PA1OUT	PA0OUT	0X00
E019	PAIN	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0	0X00
E01A	PBCTL0	PB7CTL0	PB6CTL0	PB5CTL0	PB4CTL0	PB3CTL0	PB2CTL0	PB1CTL0	PB0CTL0	0x07
E01B	PBCTL1	PB7CTL1	PB6CTL1	PB5CTL1	PB4CTL1	PB3CTL1	PB2CTL1	PB1CTL1	PB0CTL1	0x00
E01E	PBMS0	PB7MS0	PB6MS0	PB5MS0	PB4MS0	PB3MS0	PB2MS0	PB1MS0	PB0MS0	0x00

E01F	PBMS1	PB7MS1	PB6MS1	PB5MS1	PB4MS1	PB3MS1	PB2MS1	PB1MS1	PB0MS1	0x00
E020	PBMS2	PB7MS2	PB6MS2	PB5MS2	PB4MS2	PB3MS2	PB2MS2	PB1MS2	PB0MS2	0x00
E029	PBMSK	PB7MSK	PB6MSK	PB5MSK	PB4MSK	PB3MSK	PB2MSK	PB1MSK	PB0MSK	0X00
E02A	PBOUT	PB7OUT	PB6OUT	PB5OUT	PB4OUT	PB3OUT	PB2OUT	PB1OUT	PB0OUT	0X00
E02B	PBIN	PBIN7	PBIN6	PBIN5	PBIN4	PBIN3	PBIN2	PBIN1	PBIN0	0X00
E02C	PCCTL0	PC7CTL0	PC6CTL0	PC5CTL0	PC4CTL0	PC3CTL0	PC2CTL0	PC1CTL0	PC0CTL0	0x0F
E02D	PCCTL1	PC7CTL1	PC6CTL1	PC5CTL1	PC4CTL1	PC3CTL1	PC2CTL1	PC1CTL1	PC0CTL1	0x0F
E030	PCMS0	PC7MS0	PC6MS0	PC5MS0	PC4MS0	PC3MS0	PC2MS0	PC1MS0	PC0MS0	0x00
E031	PCMS1	PC7MS1	PC6MS1	PC5MS1	PC4MS1	PC3MS1	PC2MS1	PC1MS1	PC0MS1	0x00
E032	PCMS2	PC7MS2	PC6MS2	PC5MS2	PC4MS2	PC3MS2	PC2MS2	PC1MS2	PC0MS2	0x00
E03B	PCMSK	PC7MSK	PC6MSK	PC5MSK	PC4MSK	PC3MSK	PC2MSK	PC1MSK	PC0MSK	0X00
E03C	PCOUT	PC7OUT	PC6OUT	PC5OUT	PC4OUT	PC3OUT	PC2OUT	PC1OUT	PC0OUT	0X00
E03D	PCIN	PCIN7	PCIN6	PCIN5	PCIN4	PCIN3	PCIN2	PCIN1	PCIN0	0X00
E03E	PCCTL0	PC7CTL0	PC6CTL0	PC5CTL0	PC4CTL0	PC3CTL0	PC2CTL0	PC1CTL0	PC0CTL0	0x0F
E03F	PCCTL1	PC7CTL1	PC6CTL1	PC5CTL1	PC4CTL1	PC3CTL1	PC2CTL1	PC1CTL1	PC0CTL1	0x0F
E042	PCMS0	PC7MS0	PC6MS0	PC5MS0	PC4MS0	PC3MS0	PC2MS0	PC1MS0	PC0MS0	0x00
E043	PCMS1	PC7MS1	PC6MS1	PC5MS1	PC4MS1	PC3MS1	PC2MS1	PC1MS1	PC0MS1	0x00
E044	PCMS2	PC7MS2	PC6MS2	PC5MS2	PC4MS2	PC3MS2	PC2MS2	PC1MS2	PC0MS2	0x00
E04D	PCMSK	PC7MSK	PC6MSK	PC5MSK	PC4MSK	PC3MSK	PC2MSK	PC1MSK	PC0MSK	0X00
E04E	PCOUT	PC7OUT	PC6OUT	PC5OUT	PC4OUT	PC3OUT	PC2OUT	PC1OUT	PC0OUT	0X00
E04F	PCIN	PCIN7	PCIN6	PCIN5	PCIN4	PCIN3	PCIN2	PCIN1	PCIN0	0X00
E050	TMRSTL	—	—	—	—	—	TMR2ST	TMR1ST	TMR0ST	0X00
E051	RAMCFG	MS[3:0]				—	MSE	DVS[1:0]		0X02

Clock Controller (0xE200 ~ 0xE3FF)										
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
E200	CKEN				XTALSEL		ENLSRC	ENHSRC	ENXTAL	0x01
E201	CKSTA						LSRCOK	HSRCOK	XTALOK	0x00
E202	CKSEL	TMR2CK	TMR1CK	TMR0CK	INTCK	RTCCK	PMUCK	SYSCK		0x00
E203	HPCKCTL	—	—	—	—	ENFMC	ENPFB	ENHPB	ENMCU	0x07
E204	PFCKCTL0	ENUART	ENI2C	ENWDT	ENRTC	—	ENLCM	ENANA	ENSDM	0x00
E205	PFCKCTL1	ENPD	ENPC	ENPB	ENPA	ENSPI	ENTMR2	ENTMR1	ENTMR0	0x00
E206	PFCKCTL2	—	—	—	—	—	ENCAP	ENMFA	ENINT	0x00
E207	SYSCKD	PFB_N[3:0]				MCU_N[3:0]				0x00

E208	PFCKD0	TMR0_N[1:0]		—	—	—	SDM_N[2:0]		0x01
E209	PFCKD1	—	—	—	—	TMR2_N[1:0]		TMR1_N[1:0]	0X00
E20A	PWMOD	—	—	—	—	—	—	PWMOD[1:0]	0X00

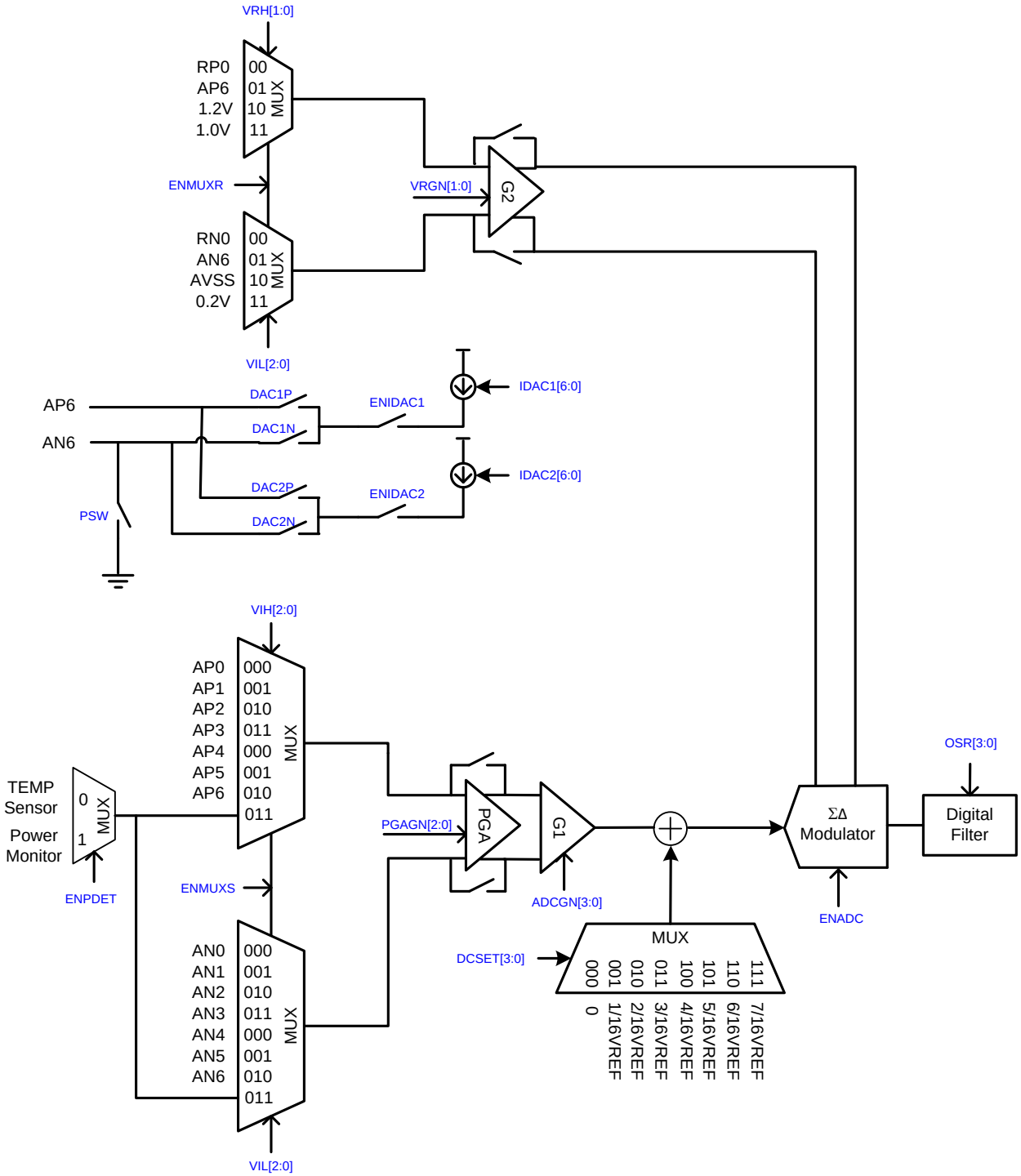
Interrupt Controller (0xE400 ~ 0xE5FF)										
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
E400	GINTMSK	—	—	—	—	—	—	—	ENGINT	0x01
E401	INTCTL	INT3CTL[1:0]		INT2CTL[1:0]		INT1CTL[1:0]		INT0CTL[1:0]		0x00
E402	ENTEN	—	—	—	—	ENINT3	ENINT2	ENINT1	ENINT0	0x00
E403	INTDCTL	—	—	—	—	DBSAMPC[3:0]				0x00
E404	INTSTA	—	—	—	—	INT3F	INT2F	INT1F	INT0F	0x0F
E405	PINTSTA0	WDTINTF	RTCINTF	SDMINTF	—	INT3F	INT2F	INT1F	INT0F	0x0F
E406	PINTSTA1	—	SPIINTF	UARTINTF	I2CINTF	—	TMR2INTF	TMR1INTF	TMR0INTF	0x00
E407	IRQNUM	—	—	—	IRQNUM[4:0]					0x00
E408	IRQCLR	—	—	—	—	—	—	—	IRQCLR	0x00

SDADC REGISTER (0xE600 ~ 0xE7FF)										
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
E600	RDATL	RAW_DATAL[7:0]								0x00
E601	RDATM	RAW_DATAM[7:0]								0x00
E602	RDATH	RAW_DATAH[7:0]								0x00
E603	CDATL	CAL_DATAL[7:0]								0x00
E604	CDATM	CAL_DATAM[7:0]								0x00
E605	CDATH	CAL_DATAH[[7:0]								0x00
E606	SNSGNL	SNS_GAINL[7:0]								0x00
E607	SNSGNM	SNS_GAINM[7:0]								0x00
E608	SNSGNH	SNS_GAINH[7:0]								0x00
E609	SNSOSL	SNS_OSL[7:0]								0x00
E60A	SNSOSM	SNS_OSM[7:0]								0x00
E60B	SNSOSH	SNS_OSH[7:0]								0x00
E60C	SNSINIL	SNS_INIL[7:0]								0x00
E60D	SNSINIM	SNS_INIM[7:0]								0x00
E60E	SNSINIH	SNS_INIH[7:0]								0x00

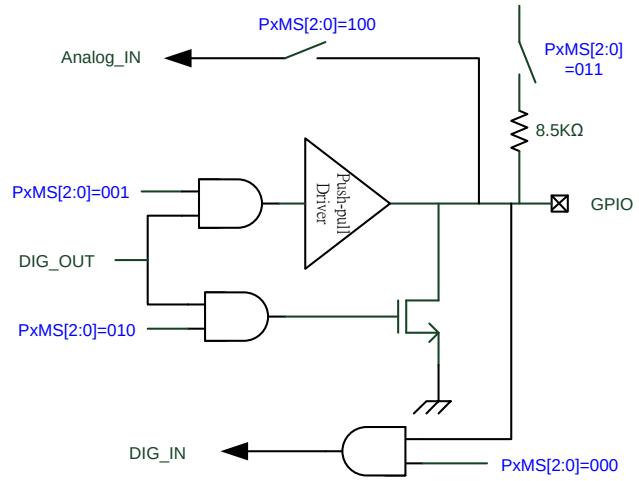
E60F	TMPGNL	TMP_GAINL[7:0]								0x00
E610	TMPGNM	TMP_GAINM[7:0]								0x00
E611	TMPGNH	TMP_GAINH[7:0]								0x00
E612	TMPOSL	TMP_OSL[7:0]								0x00
E613	TMPOSM	TMP_OSM[7:0]								0x00
E614	TMPOSH	TMP_OSH[7:0]								0x00
E615	TMPINIL	TMP_INIL[7:0]								0x00
E616	TMPINIM	TMP_INIM[7:0]								0x00
E617	TMPINIH	TMP_INIH[7:0]								0x00
E618	OSR	—	—	—	—	OSR[3:0]				
E619	MUXSIG	ENMUXS	—	INL[2:0]			INH[2:0]			0x00
E61A	MUXREF	ENMUXR	—	—	—	VRL[1:0]		VRH[1:0]		0x00
E61B	PGASET	—	ENBUF	ENPGACH	ENPGA	—	PGAGN[2:0]			0x00
E61C	GNSET0	ENADC[1:0]		VRGN[1:0]		ADCGN[3:0]				0x00
E61D	GNSET1	—	—	—	—	—	DCSET[2:0]			0x00
E61E	REFCTL	—	—	—	—	—	ENDEM	ENTSCH	ENVREF	0x00
E61F	INTSTA	INTFG	—	—	—	—	—	—	ENINT	0x00
E680	INCH	—	—	—	—	—	INCH[1:0]		—	0X00

Analog Controller REGISTER (0xE800 ~ 0xE9FF)										
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
E800	CMPCFG	HYS[2:0]			CMPTH[1:0]		ENINT	ENCMPH	ENCMPR	
E801	CMPOUT	—	—	—	—	—	—	—	CMPOUT	
E802	LVCFG	LVDFG	LVD[2:0]			LVR[1:0]		ENLVD	ENLVR	
E803	LVDINT	—	—	—	—	—	—	—	LVDINT	
E804	PWRCFG	—	ENOPA	ENBODN	ENBODP	ENPDET	ENVCM	ENLDO	EBCHIP	
E805	IDACCFG	—	—	—	PSW	DAC2N	DAC1N	DAC2P	DAC1P	
E806	IDAC1CTL	ENIDAC1	IDAC1[6:0]							
E807	IDAC2CTL	ENIDAC2	IDAC2[6:0]							

Sigma-Delta Modulator Network



GPIO Connection Network



GPIO Configuration Table

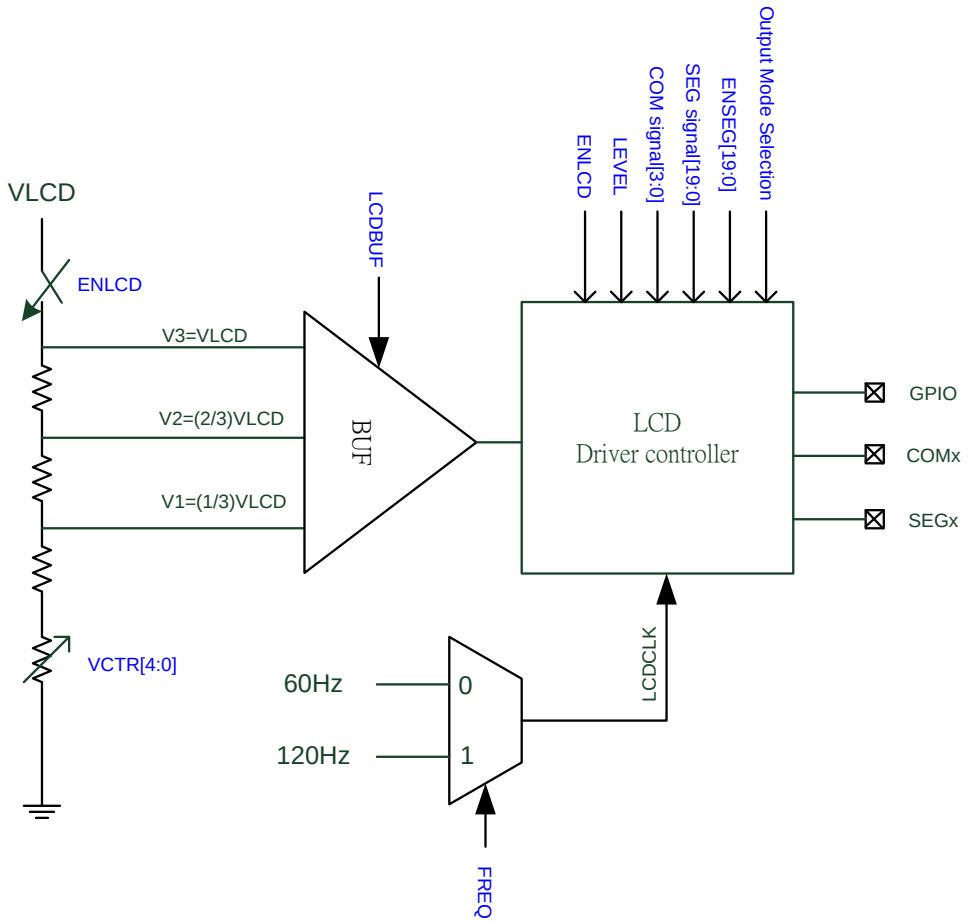
PORT	CONFIG	FUNCTION
PA.0	00	GPIO
	01	MISO
	10	
	11	
PA.1	00	GPIO
	01	MOSI
	10	
	11	
PA.2	00	GPIO
	01	SCLK
	10	INT3
	11	
PA.3	00	GPIO
	01	SS
	10	INT2
	11	
PA.4	00	GPIO
	01	SDA
	10	
	11	
PA.5	00	GPIO
	01	SCL
	10	INT1
	11	
PA.6	00	GPIO
	01	RX
	10	
	11	
PA.7	00	GPIO
	01	TX
	10	
	11	

PORT	CONFIG	FUNCTION
PB.0	00	GPIO
	01	RST
	10	
	11	SEG19
PB1	00	GPIO
	01	XTALOUT
	10	
	11	SEG18
PB.2	00	GPIO
	01	XTALIN
	10	
	11	SEG17
PB.3	00	GPIO
	01	
	10	INT0
	11	SEG16
PB.4	00	GPIO
	01	PWM0
	10	
	11	SEG15
PB.5	00	GPIO
	01	PWM1
	10	
	11	SEG14
PB.6	00	GPIO
	01	PWM2
	10	
	11	SEG13
PB.7	00	GPIO
	01	PWM3
	10	
	11	SEG12

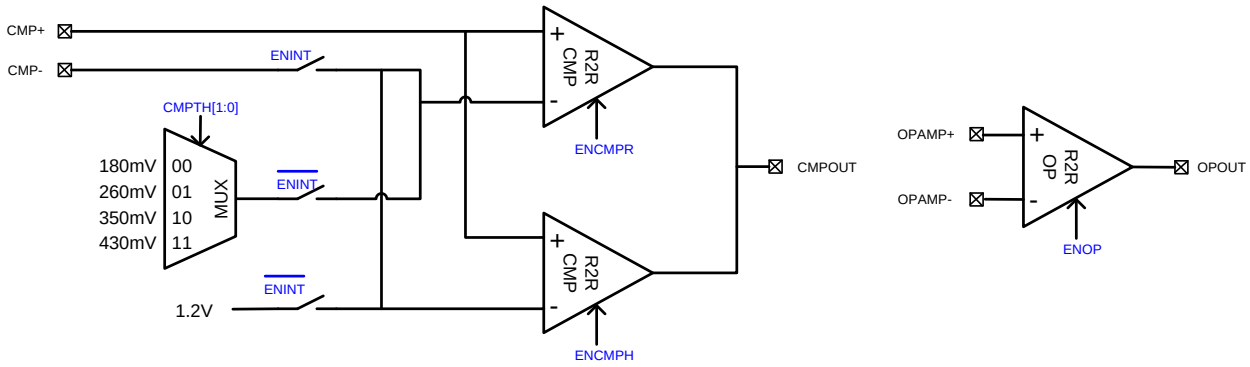
PORT	CONFIG	FUNCTION
PC.0	00	GPIO
	01	PWM4
	10	
	11	SEG11
PC.1	00	GPIO
	01	PWM5
	10	
	11	SEG10
PC.2	00	GPIO
	01	nCTS
	10	OCD_SDA
	11	SEG9
PC.3	00	GPIO
	01	nRTS
	10	OCD_SCK
	11	SEG8
PC.4	00	GPIO
	01	
	10	ISP_SDA
	11	SEG7
PC.5	00	GPIO
	01	
	10	ISP_SCL
	11	SEG6
PC.6	00	GPIO
	01	
	10	CMPP
	11	SEG5
PC.7	00	GPIO
	01	
	10	CMPN
	11	SEG4

PORT	CONFIG	FUNCTION
PD.0	00	GPIO
	01	CAPIN0
	10	
	11	SEG3
PD.1	00	GPIO
	01	CAPIN1
	10	OPAOUT
	11	SEG2
PD.2	00	GPIO
	01	CAPIN2
	10	OPAP
	11	SEG1
PD.3	00	GPIO
	01	CAPIN3
	10	OPAN
	11	SEG0
PD.4	00	GPIO
	01	
	10	AP0
	11	COM3
PD.5	00	GPIO
	01	
	10	AN0
	11	COM2
PD.6	00	GPIO
	01	
	10	AP1
	11	COM1
PD.7	00	GPIO
	01	
	10	AN1
	11	COM0

LCM Driver Network



OPAMP and Comparator Network



Overview

The FE8116x is a 8-bit RISC processor with low-noise, low-power and multi-function configurable sigma-delta data converter and LCD driver. The device incorporates buffers, reference voltages, programmable gain stages, internal digital filtering, sensor diagnostics and on-chip temperature sensors which is intended to applicable into wide dynamic range, low-frequency input signals, scales, pressure and temperature measurements.

Register File

The FE8116x build-in register files which can be configured to control the functions of analog front end. After power up, the internal power on reset circuit will clear the register data into default value.

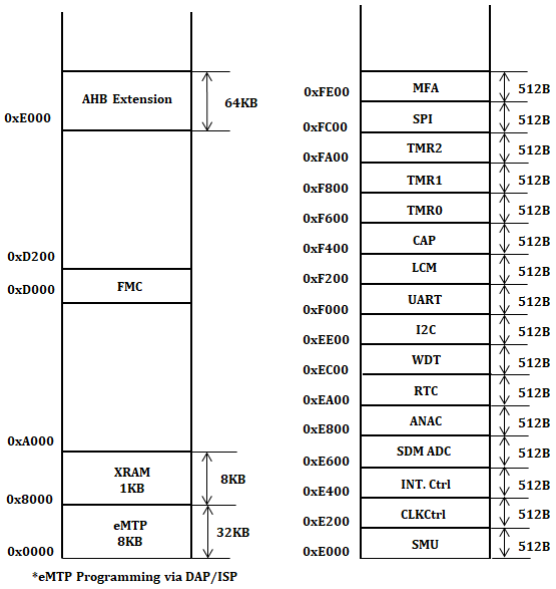
Memory Organization

The FE8116x contains 4 memory blocks

- 4K words MTP program memory
- 32 words on-chip MTP data memory
- 1K bytes general purpose SRAM
- 256 bytes internal XRAM (iRAM)

MTP program memory

The device allocates 4K words of MTP program memory for code running. After power-on reset or hardware reset, the FE8116x will execute program code from address 0x0000 of internal 4K words program memory. The MTP reserved extra 32 words for data memory. The brief calibration or manufacturing parameters could be saved in the space. The memory arragenment map is in Fig.



LCD Driver

The FE8116x includes a maximum 4 COMs and 20 SEGs to drive external LCD panel which used as a user interface in most of the appliances. The LCD panel could display the measurement data to users' reading. The COMs and SEGs signals vary continuously both in time and amplitude to generate an AC-like signals to drive LCD panel. The LCD driver could drive signals directly to versatile customized LCD panels.

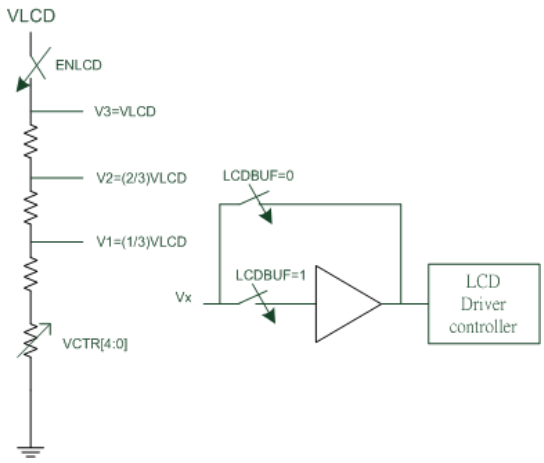
The FE8116x incorporates COMs and SEGs signals, as well as 1/2 and 1/3 bias voltage setting in 1/4 duty operation. The bias voltage designs in resistive-type. There are VCTR[3:0] 4 bits in contrast adjustment register, which is used to fine tune the panel crystal twisting level. User could discriminate the display panel transparancy by configuring the contrast register.

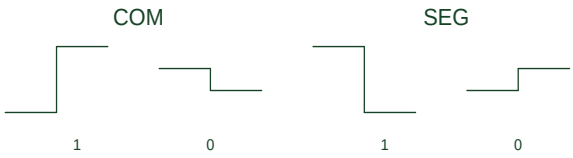
LCD Driver Output

The LCD driver output could up to 4 COMs and 20 SEGs. The LCD driver bias type is resistive-type only. The fundamental driver power supplies from external regulator with resistive divider. Internal bias supply voltage drivers are allocated for higher loading LCD panels. The internal buffer could be disabled with capacitive loading panel for low power consumption.

LCD Waveform Timing Diagrams

The LCD driver output signal should be emulate an AC-like signal to stimulate pixels of LCD panel. Each COM and SEG signals will map to a specific waveform, each pixel will be driven by the (COM-SEG). User could select the bias voltage level in 1/3 bias or 1/2 bias by LEVEL bit configuration register, it is a 1/3 bias driving signals waveform below for reference.





Comparators

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on a comparison of two analog inputs.

There are 2 independent comparators within the device. One is a rail-to-rail differential input comparator, another is an input hysteresis comparator. The comparators offer flexible system inquiry in different applications. Because of the comparators use the same I/O pins, only one of the comparators could be active at a certain time.

The comparators optimized for normal voltage operation. Internal hysteresis makes it easy to use even with slow moving input signals. The rail-to-rail input topology maximizes the input wide dynamic range available. The enable control allows for reduced power consumption and release the multi-function I/O pins to other usage.

Operational Amplifier

The FE8116x incorporates a rail-to-rail differential operational amplifier which can be used to amplify low-level sensor signal to fit the dynamic range of following data processing stage. The operational amplifier can be enabled and disabled by ENOPA bit in PWRCFG register by digital communication interface in the device. System designer could use the operational amplifier to implement an analog filter in noisy and tough operation environment or unity gain buffer for impedance matching.

Power Supply Monitors

Regard to monitor the supply voltage quality, the FE8116x build-in supply voltage monitoring function. The VDDA voltage will be attenuated internally divider circuit by one-fourth and applies to data converter. The power supply monitoring is useful because of voltage variation from power supply could be measured continuously. The power supply monitoring is a combo functions in CH7 of multiplexer. User could be active the function by configuring the input multiplexing in CH7 and ENPDET=1.

Linear Regulator (LDO)

The FE8116x has 2 independent power supply pins, VDD and VDDA. VDD is the supply voltage of the device which power the digital section the FE8116x including clock generator and digital processing circuits. After the supply voltage is stable, nternal power on sequence will reset all the circuits into an initial condition and register map will return to default value. The VDD supply voltage is reference to VSS and the maximum voltage rating is 4.0V.

There is a build-in on-chip linear regulator for analog section to enhance the capability of supply voltage noise rejection which powers from supply voltage VDD of the device. The

regulator could be enabled by register configuration ENLDO before data converter active. There are external decoupling capacitors on VDDA pin to filter high-frequency noise. In power saving mode, designer could turn off the LDO to reduce power consumption. During LDO disabled, off-chip microcontroller could access the register data from I2C digital interface.

The LDO regulator supplies a regulated voltage to critical analog section of the device contains programmable gain amplifier, reference voltage, current DACs and delta-sigma data converters. VDDA is referenced to VSSA and the maximum voltage rating is 4.0V. VDDA should be connected to external capacitors for noise filtering. It recommends using an uF-order capacitor parallel to a few hundred pF capacitor. The VDDA could be used as the regulated sensor excitation bias for signal conditioning.

One thing needs to be noted that before enable the LDO, the ENCHIP bit should active also. The ENCHIP=1 will wake up the heart of analog section will could supply power to all the sub-circuits.

Because of the fully differential architecture of sigma-delta modulator, a common-mode voltage shall be a bias voltage for integrators. The ENVCM bit in PWRCFG register must be active and enable the ADC conversion by ENADC bit.

Channel Multiplexer Configuration

The FE8116x incorporates differential 8 channels multiplexed data acquisition system utilized in industrial process control, portable medical devices, and automated test equipment need increased channel density where the user can measure the signals from multiple sensors, monitor and scan input channels into a single sigma-delta ADC. The differential multiplexing channels could be configured independently. The benefit of multiplexing is using fewer channels for multiple signal conditioning to save print circuit board space, power consumption and cost. The sigma-delta data converter is conventionally monotonic and uses integrated modulator for oversampling and digital decimation filtering that requires an internal clock source to synchronize all the functionality circuit blocks, resulting in a nonzero cycle latency. The multiplexer input faces limited bandwidth, settling time and input range which will degrade the system performance requiring to be designed carefully.

The FE8116x can be configured as 8 fully differential analog input channels, the ADC on the device can be fully buffered internally. The analog input signals are connected to internal programmable gain amplifier when the device is operated in buffered mode. It can be configured as unbuffered mode by hardware register setting. Buffering the input channel means that the device can handle significant source impedances on the selected analog input and also the external anti-aliasing RC filter components which placed on the analog

inputs. Be careful to design the RC filtering circuit which will result in dc gain errors depending on the output impedance of the signal sources. (It is recommended that a 10nF to 100nF capacitor be placed on the input the ADC to filter the external system noise for better performance.

On-Chip Temperature Sensor

The FE8116x integrates an on-chip temperature sensor to use as junction or environment temperature measurement. The temperature sensor measurement could be initiated if the analog input signal multiplexers are selected, VINHMUX[2:0]=111, VINLMUX[2:0]=111 and ENPDET=0. The CH7 of the input signal multiplexer combos the on-chip temperature sensor and power supply monitoring functions. If ENPDET=0, the channel inputs the temperature sensor signals, else ENPDET=1, the supply voltage can be monitored by data converter.

Temperature readings follow the same process as the analog inputs, but only relevant MSB 14 bits are used to indicate the temperature measurement result. 1LSB stands for 0.025625℃ in temperature where the MSB is the sign-bit represents the positive or negative temperature. The DATA[23:10] is the output data of temperature measurement. DATA[23] stands for the sign-bit of temperature, 0 represents the junction temperature above 0℃ and 1 represents below 0℃.

Programmable Gain Amplifier (PGA)

The device integrates a programmable gain amplifier to interface the analog sensor signals, which could be used as an input analog buffer as well as gain stage, then forwarding the amplified input signal to low-noise sigma-delta modulator. The PGA function could be enabled by configuring INBUF bit in register. If the INBUF=1, the amplifier will active, and the amplifier will be disabled when INBUF=0. The PGA amplifier will be active automatically as the gain setting greater than 1. If the gain setting is equal to 1, user could configure to enable the buffer or not to adapt the input source connections. Although its wide input dynamic range of PGA and analog-to-digital converter, it is necessary to ensure that the headroom required for correct operation is tolerable in gain configuration.

When the PGA amplifier is enabled, the input channel multiplexer will apply to input of the instrumentation amplifier. The low-noise programmable gain amplifier can amplify small amplitude signals to be gained while still maintaining excellent noise performance. The input gain in buffered mode could be programmed in 1, 2, 4, 8, 16, 32, 64 and up to 128 times in the configuration register. For example, with an internal 1.2V reference voltage, the unipolar input range is from 1.2V and the bipolar range is from ±1.2V.

If the FE8116x is operated with external reference that has a value equal to VDDA, the analog input signal must be limited to 80% of VREF/PGAGN[2:0] when the programmable

gain amplifier is enabled.

By unknown or higher source impedance, the input channel should set to using buffer mode where the input channels feeds into a high impedance input stage. Therefore, the FE8116x can tolerate any signal source impedances which connect to external resistive-type sensors directly. User could enable buffered mode to set the INBUF=1. It should be noted that the input common mode range of buffer mode between AVSS+100mV to AVDD-1V.

When INBUF=0, the devices operate in unbuffered mode. User can configure the ADCGN to setup the 2nd gain stage to amplify the input signals without buffer. If the input source impedance is low enough compared to input impedance of sigma-delta modulator, it will not result in much gain error on data converter output.

Sigma-Delta Data Converter

FE8116x incorporates a low noise, low power 24-bit sigma-delta analog-to-digital data converter functioning in oversampling architecture. It incorporates a sigma-delta modulator, a programmable gain instrumentation amplifier, and a on-chip digital decimation filter intended for the measurement of low-frequency signals such as those in RTD, thermocouple, thermopile, pressure transducer and scales. The input signals are conditioned into a digital pulse train with pulse density modulation. The pulse density contains the input signal information which accompany a band-limited digital filter and decimation. A sinc3 configurable digital low pass filter is used to decimate the modulator output data train and convert into a valid high resolution data result.

The input of ADC should allocate an anti-aliasing filter for image signal filtering. The transition band of anti-aliasing filter could be greatly simplified rather than brick-wall stop band filter in Nyquist-rate data converters. In most applications, a simple single-pole RC filter is required for easy implementation.

There is a 2nd gain stage connected after programmable gain amplifier. The 2nd gain stage which feeds through the sigma-delta modulator directly and the gains setting could be configured the ADCGN[3:0] bits in register map. The gain can be configured as gain up to 1, 2, 4, 8 or 16 when it is operated either in buffered mode or unbuffered mode. The absolute input voltage in unbuffered mode is restricted between AVSS-30mV to AVDD+30mV. Because of no buffer circuits enabled during unbuffered mode, the power consumption could be minimized in data conversion.

FE8116x allocates 8 input channels that can be buffered or unbuffered. User could adapt to different application from input source impedance to configure the buffer on/off. The input buffer incorporates with programmable gain stage to amplify low-level sensor input signals. In addition to the input gain stage configuration, the reference volage of sigma-delta data

converter could be configured also. If the full-scale of input signal after PGA amplifier stage is far below the default reference voltage, user could setup the gain of reference by VRGN[1:0] bits in register in x1, x3/4, x1/2 and x1/4 times of reference voltage which referred to analog input voltage.

There is programmable input DC offset voltage setup if the analog input voltage is not equally equipped in full-scale input dynamic range. Designer could configure the DCSET[2:0] which could adjust the input DC level by 1/16VREF to 7/16VREF from analog input voltage.

Upon the input offset voltage from sensors, the input of the sigma-delta modulator has a system chopper switch to remove the system offset effect. User could average output data from toggling input chopper switch to have an offset-free output. The ADC data converter will have a better performance if the ADC chopper function is active.

The output data rate of the FE8116x is user programmable. The allowable update rates along with different settling times could be configured by oversampling ratio register. Normal mode signal bandwidth noise rejections the major function of the digital filter. If user would like to immune 50Hz/60Hz power buzz, it could be implemented by placing the frequency response of the digital filter with output notches at 50Hz or 60Hz. Designers could configure the OSR[4:0] bits in register to change the output data rate, the maximum decimation ratio setting by OSR[4:0] is 32768.

Continuous conversion mode

In normal power-up sequence, continuous conversion mode is in default. AFE6160A continuously convert with EOC going low each time a conversion is completed. To read a conversion, the designer initiates a write command by I2C interface. The INTFG will toggle once when another conversion is completed again. The upcoming conversion data will overwrite the previous one if no external data access is initiated.

One-shot conversion mode

In one-shot conversion mode, the AFE6160A are placed in standby mode between conversions. When a one-shot mode conversion is initiated, the device will enable analog section, perform a single conversion, then return back to standby mode. The most important is the internal oscillator needs a few ms time to startup and stabilization. After a one-shot conversion is completed, the EOC will active-low to interrupt external controller to access conversion data. The register data can be read several times if EOC keeps in low without cleared. Please do not read the register data when EOC in high state.

Standby mode

In standby mode, most of the analog circuit is disabled with the linear regulator is active only. It consumes lower current consumption in standby mode but quickly response to the next data conversion. It could settle the analog signal into a stable stage in a short period of time to initiate an updated data acquisition.

Power-down mode

The FE8116x will stay into power-down mode if all the analog circuits are disabled and I/Os configure into Hi-impedance mode. It will disable all the analog circuits to minimize the power consumption of the device by lasting a longer lifetime by battery-powered operation.

Calibration

The FE8116x will go through factory calibrated flow during manufacturing and circuit testing, user could implement the measurements without user calibration. If the measurement system suffers from higher input impedance mismatch or system offset from temperature drift or environment changing, the designer could calibrate the system by facility manufacturing to remove systematic dc errors for zero-scale calibration, internal gain error calibration, system zero-scale calibration and system gain error calibration, which effectively reduce the offset error and gain error to the optimized measurement performance.

During an internal offset error and gain error calibration, the input multiplexer and are connected internally to the ADC input pins. However, a system calibration should apply the input voltages on the analog input pins before systematic calibration is initiated.

A calibration should be treated as a data converter operation. After each data conversion, the output data of digital filtering is scaled using the ADC calibration registers before being written to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient.

ADC Digital Data Output

The oversampling sigma-delta modulator could be configured into unipolar or bipolar input, the digital data output is a binary with 2’complement format. The differential input voltage with 0V will output 0x000000, and a full-scale input voltage results in a code of 0xFFFFF.

Reference Voltage

The FE8116x has 4 separate fully differential input channels wherein 2 channels by external reference voltage and 2 channels by internal reference voltage generator. While all the 4 reference signals are available for use with the data converter. There is embedded a 1.2V reference supply. The reference voltage of sigma-delta modulator can be applied from internal bandgap reference or external reference input. For external references, the

sigma-delta modulator has a fully differential input capability with the channels. There is a reference signals multiplexer configuration register. While ENMUXR=0, the reference input signals are connected to analog ground. When ENMUXR=1, it will active the reference multiplexer and the reference input signals will be selected by RINPMUX[1:0] and RINNMUX[1:0] register. The RP0/RN0 is a dedicated differential external reference input channel and another reference input channel, RP1/RN1, is a combo function with analog input channel AP6/AN6. User can select any external low noise discrete voltage reference source by configuring the reference input buffer to get the optimizing performance. When the internal reference voltage is selected, it is preferred to connect the external reference pins to analog ground to protect from noise crosstalk and coupling on multiplexer.

The reference inputs provide a high impedance, dynamic load to external connections. The RC anti-aliasing filter will cause dc gain errors depending on the output impedance of the source that is driving the reference inputs. The reference input can be configured in on-chip buffered or unbuffered circuits by VRBUF bit in register. When VRBUF=0, the reference input voltage will bypass the internal buffer and connect to switched-capacitor circuits in data modulator. If VRBUF=1, the reference input will buffer by internal amplifier to immune the gain error result from the excessive RC source impedance mismatch. The common-mode range for the differential inputs is from VSSA to VDDA-1V.

In application where the excitation current for the external sensor on the analog inputs also drive the reference voltage by ratio-metric. The steering current error will be cancelled by such connection architecture. Using external reference resistor of reference voltage generation, it is important to consider using a lower temperature coefficient external resistor with higher accuracy and a better temperature drift performance.

Sensor-Connection Fault Detection

For the harsh application environment where safety will be a high priority consideration, internal diagnostics are becoming part of the industry requirements. The embedded sensor-connection self-diagnostics in the FE8116x reduce the need for external components to implement diagnostics, resulting in an easy and BOM saving solution.

To help detect a possible sensor malfunction, the device provides internal burnout current sources. The FE8116x contains dual internal current sources output to diagnose the sensor connection status. The 2 weak output burn-out detection currents, where one analog I/O pin sources current from VDDA to AP6 and another analog I/O pin sinks current from AN6 to VSSA. The burn-out currents are configurable for use on AP6 and AN6. The dual burn-out current sources are selected by ENBODP and ENBODN bits in register configuration independently. The burn-out bit will setup when the detection level over the limiting register setup by user in power-up. The source/sink detection currents will stimulate the external sensor devices where the generated output voltage could be monitored by data converter. It could verify that an external sensor is working properly before attempting

to proceed signal measurements on the channel.

After the burn-out detection currents are enabled, the voltage level of analog I/O pins could ensure that it is within the specified operating range. If the detected voltage level is outside the nominal operation range, it could be discriminated the sensor is disconnected or burn-out by abnormal operation. A near full-scale reading from sourcing burnout current means the front-end sensor is overloaded or disconnected. On the other side, a near 0V voltage reading from sinking burnout current stands for the sensor-connection is disconnected or short circuiting. The source/sink burnout currents could be used as the system diagnostic in power-up or normal operation occasionally. We recommend to disable the current sources during normal operation of data conversion.

The diagnostics lead to a more robust solution for system safety consideration by data converter operation. Keep in mind that ADC readings of the functional sensor may be corrupted when the burnout current sources are enabled. Disable the burn-out current sources when performing the precision measurement, and only enable it while sensor fault conditioning test.

Digital Filters

The FE8116x incorporates a low-pass, sinc3 filter, it removes the quantization noise introduced by the sigma-delta modulator. It will filter out the high frequency noise power to minimize the output noise level in interested bandwidth. It limits the bandwidth of frequency response significantly lower than half of the modulator sampling frequency. The cutoff frequency and decimated output data rate of the filter is programmable by OSR[3:0] register. The notch frequency of the digital filter could be designed by specific application to reject unintended noise. The sigma-delta modulator will oversample the input analog signal and shape most of the noise power outside the signal bandwidth. The modulator digital data pulse train will feed into digital decimation with programmable oversampling ratio to setup the optimized output data rate of specific application. The output data of digital filter will store in the dedicate register location. The digital communication interface can access the registers and read out the data converter output.

To ensure the output data will be effective, the digital filter of FE8116x will be reset without affecting any of the setup conditions on the device. All the internal flipflops are refreshed by reset, the digital filter will start a new data conversion by band-limited filter and decimation without user configuration. The clock of digital filter will be synchronized with modulator data output. After the decimation filter, there will be a data ready indicator.

Noise and Resolution

There are 2 kinds of noise terminologies where one is rms noise, another is peak-to-peak

noise. The rms noise could derive into effective number of bits (ENOB) and peak-to-peak noise express into noise-free resolution for various output data rates. Of configuring the gain and oversampling ratio settings, designer could tradeoff the output data rate and resolution. The FE8116x is a differential, bipolar analog input sigma-delta converter with 24 bits 2's complement digital output. The most-significant bit of digital output data stands for sign-bit to indicate the analog input signal polarity.

It is important to note that the effective number of bits is calculated using the rms noise, where the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak noise is measured by histogram which represents the resolution for which there is no flicker code output.

The FE8116x integrates a sinc3 digital filter for signal filtering and decimation. User could configure the OSR]4:0] register to change the output data rate trading off the speed and performance. There should also cascade a FIR filter after the sinc3 digital filter by software which could be used as user-defined filter frequency transfer function to adapt system signal processing requirements.

ADC data measurement by PGA enabled, Noise-Free resolution (effective resolution) at T_A =25℃ and internal 1.2V Reference

	OSR							
PGAGN	512	1024	2048	4096	8192	16384	32768	65536
x1	13.8(16.6)	14.27(17.1)	14.86(17.57)	15.49(18.04)	16.15(18.52)	16.63(18.97)	17.25(19.51)	18.22(20.17)
x2	13.51(16.19)	13.92(16.69)	14.47(17.18)	15.1(17.67)	15.64(18.22)	16.57(18.82)	17.05(19.35)	17.79(20.11)
x4	13.77(16.45)	14.39(16.97)	14.71(17.47)	15.21(17.95)	15.46(18.36)	16.17(18.78)	16.65(19.23)	17.48(19.65)
x8	13.74(16.59)	14.37(17.07)	14.84(17.55)	15.32(18)	15.92(18.51)	16.43(19.04)	16.99(19.5)	17.48(19.8)
x16	13.56(16.34)	14.2(16.82)	14.69(17.28)	15.33(17.76)	15.75(18.24)	16.25(18.62)	16.8(19.12)	17.56(19.78)
x32	12.82(15.63)	13.42(16.14)	13.87(16.66)	14.58(17.15)	15.11(17.56)	15.66(17.95)	16.09(18.38)	16.53(18.84)
x64	12.18(15.01)	12.59(15.49)	13.46(15.99)	13.85(16.45)	14.53(16.91)	14.92(17.37)	15.57(17.7)	15.88(17.93)
x128	11.51(14.2)	12.21(14.7)	12.54(15.21)	13.02(15.72)	13.71(16.26)	14.23(16.8)	14.98(17.21)	15.81(17.8)

ADC data measurement by PGA enabled, Noise-Free resolution (effective resolution) at T_A =25℃ and external ratiometric measurement

	OSR							
PGAGN	512	1024	2048	4096	8192	16384	32768	65536
x1	14.39(17.27)	15.21(17.77)	15.85(18.27)	16.29(18.74)	16.69(19.26)	17.3(19.76)	18(20.41)	18.79(21.12)
x2	14.33(17.18)	14.95(17.67)	15.5(18.18)	16.19(18.73)	16.77(19.27)	17.42(19.84)	18.17(20.44)	18.87(21.13)
x4	14.04(17.01)	14.64(17.49)	15.31(18.02)	15.88(18.55)	16.71(19.12)	17.26(19.68)	17.85(20.23)	18.45(20.78)
x8	14.17(16.84)	14.62(17.32)	15.34(17.83)	15.81(18.38)	16.4(18.91)	16.99(19.37)	17.62(19.73)	17.89(20.11)
x16	13.2(15.9)	13.52(16.39)	14.09(16.87)	14.9(17.39)	15.54(17.98)	16.23(18.7)	16.92(19.51)	17.48(20.01)
x32	13.73(16.47)	14.24(16.94)	14.78(17.42)	15.36(17.91)	16.03(18.46)	16.57(19)	17.13(19.36)	17.66(19.83)
x64	12.56(15.2)	12.9(15.65)	13.5(16.14)	14.11(16.64)	14.76(17.15)	15.2(17.75)	15.87(18.33)	16.64(18.93)
x128	11.76(14.36)	12.21(14.85)	12.67(15.37)	13.27(15.87)	13.84(16.31)	14.41(16.8)	14.86(17.17)	15.48(17.7)

ADC data measurement by PGA disabled, Noise-Free resolution (effective resolution) at T_A =25℃ and internal 1.2V Reference

	OSR							
ADCGN	512	1024	2048	4096	8192	16384	32768	65536
x1	14(16.65)	14.31(17.14)	14.93(17.66)	15.62(18.2)	16.24(18.76)	16.84(19.34)	17.49(19.94)	18.33(20.51)
x2	13.82(16.67)	14.32(17.18)	14.98(17.68)	15.45(18.11)	16.09(18.56)	16.66(19.06)	17.15(19.54)	18.02(20.21)
x4	13.82(16.67)	14.32(17.18)	14.98(17.68)	15.45(18.11)	16.09(18.56)	16.66(19.06)	17.15(19.54)	18.02(20.21)
x8	13.58(16.39)	14.04(16.89)	14.77(17.4)	15.1(17.89)	15.82(18.37)	16.6(18.87)	17.14(19.35)	17.77(20)
x16	13.8(16.52)	14.49(17.04)	14.9(17.57)	15.38(18.09)	15.93(18.54)	16.6(18.93)	16.99(19.25)	17.56(19.46)

ADC data measurement by PGA disabled, Noise-Free resolution (effective resolution) at T_A =25℃ and external ratiometric measurement

OSR								
ADCGN	512	1024	2048	4096	8192	16384	32768	65536
x1	14.6(17.3)	15.06(17.82)	15.59(18.35)	16.25(18.88)	16.88(19.41)	17.31(19.97)	18.07(20.56)	18.71(21.16)
x2	14.73(17.32)	15.09(17.82)	15.54(18.33)	16.26(18.9)	16.89(19.41)	17.29(19.87)	17.91(20.37)	18.45(20.75)
x4	14.39(17.18)	15.03(17.68)	15.66(18.23)	16.12(18.82)	16.86(19.42)	17.4(19.9)	18.25(20.41)	18.51(20.69)
x8	14.19(17.08)	14.86(17.6)	15.45(18.12)	16.03(18.64)	16.63(19.14)	17.23(19.66)	17.91(20.21)	18.45(20.58)
x16	13.99(16.73)	14.51(17.25)	14.83(17.73)	15.46(18.27)	16.14(18.81)	16.78(19.36)	17.48(19.97)	18.17(20.61)

Reset

After initial VDD power up sequence, the supply voltage will ramp up and stable in a short period of time, the internal power on reset will refresh the digital register file into default values.

FE8116x includes a hardwire reset pin with external resistor and capacitor where the capacitor will charge up slowly by VDD power up. In situations where interface synchronization is lost, user could reset the device by VDD power on/off or hardware reset pin button discharged. After the power-on sequence, all the register data will reset into default values and abort any operation conditions. User can re-command the register configurations after power on process.

The FE8116x supports software reset where user could reset the device by a fixed I2C data pattern. The device responds to the two-wire general call address (0000 000) if the LSB bit is 0. The device acknowledges the general call address and responds to commands in the 2^{nd} byte. If the 2^{nd} byte is 0000 0110, the FE8116x resets the internal registers to default values after power-up sequence.

Low Voltage Detector (LVD)

The low voltage detector function is embedded into FE8116x for supply voltage drop by continuously power consumption or abnormal large current drain in operation. The low voltage detection circuit will monitor the power supply voltage, VDD, and issue a warning flag if the VDD voltage drop below a certain level which is setup by LVD[2:0]. The LVD function is useful in battery-powered application which could provide a low-voltage indicator to system for safety data storage or shutdown protection.

The LVD function will be active by ENLVD=1, and comparing the VDD voltage with internal reference by pre-configured voltage level. The voltage detection level could be programmed by LVD[2:0]. When the power supply voltage drops below the pre-configured voltage level, and the condition continuous for a hundred-us or longer, the LVDF will be set automatically. The LVD flag will be reset when the supply voltage, VDD, raise up to pre-configured voltage level.

IDAC Excitation Current Sources

The devices build in dual excitation current which could be used as the current excitation of sensors, it expresses as the current DAC output (IDAC) in datasheet. The dual IDAC excitation current source can be enabled individually by ENIDAC1 and ENIDAC2. The IDAC constant current sources that can be programmed up to 1.2mA by 7 bits in IDAC1[6:0] and IDAC2[6:0] register setting. Both excited source currents from the VDDA are directed to

AP6/AN6 pins which are combo-function pin configuration with analog input (AP6/AN6) and reference voltage input pins (RP1/RN1). The IDAC current sources can be used to stimulate external resistive bridge, thermisor, resistive-type sensors or RTD sensors.

On-Chip Sensor Switch

A low-side PSW switch connect between AN6 pin and VSSA. It is a sensor power on/off witch to control sensor current path. The sensor switch could be configured by PSW bit in IDACCTL register.

When the sensor stimulus path is active, either in current steering or voltage regulation mode, the on-chip switch should be turned on. As the on-chip sensor switch is enabled, the current loop will be closed where the sensor components will output electrical signals. The higher excitation current for sensor sourcing, the larger output voltage level will be generated. Most of the discrete passive sensors are resistive-type, ensuring to lower power consumption and self-heating effect, the lower excitation current is desired. On the other side, lower excitation current results in lower electrical signal output from sensor devices.

However, to minimize self-heating, the excitation current needs to be turned off when the measurement is disabled. The designer can turn on the on-chip sensor switch during measurements and turn off it without data conversion to save power consumption.

The timing is a design factor for the time frame of on-chip sensor switch on/off. It depends on system specification by different sensor application. Designer needs to determine the timing configuration to optimize the system performance. Design should balance the selection of stimulation current, signal gain, reference gain and external components to ensure that the analog input voltage is being optimized along with tuning the ADC speed to give better resolution and system performance, and results in lower noise and lower offset errors.

I2C Digital Communication Interface

The FE8116x has a 2-wire serial interface that is compatible with standard I2C specification. The I2C is a serial communication interface for data exchanging from one or more than one master or other hardware peripherals. It is operated as a slave device where a controller or master device could access the register data through I2C specified timing patterns. Connections to the bus are made through the open-drain or open-collector I/O line SDA and SCL input pin. External pull-up resistor is needed for each of the two terminals. There are Schmitt triggers at SDA/SCL input signal chain to minimize the effects of signal fluctuations from harsh environment which couple noisy signals on data bus. The FE8116x supports the I2C transmission protocol up to 1MHz clock frequency of fast mode.

I2C protocol

I2C transmission flag includes a START signal, STOP signal, and Acknowledge bit. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted.

START signal

When the bus is free meaning no master device is using the bus (both SDA and SCL are high), master can send a START signal which defined as a high to low transition of SDA when SCL is high. The Repeated START is no STOP condition before the second START.

STOP signal

The master can terminate the communication by generating STOP signal.
The STOP signal is defined as low to high transition of SDA when SCL is high.

Transfer mode

I2C interface can operate as a master/slave to execute the 8-bit serial data transmission/reception. Thus, the module can operate in one of two mode: Read mode and Write mode.

Write mode

Data transmission start when master generate a START signal. First byte after the START signal is called slave address. This is a 7-bits slave address followed by a R/W bit (set R/W bit as 0 because sending data to slave). when slave address transfer is completed, only the slave (as a receiver) with an address that matches the address transmitted by master will respond by returning an ACK bit by pulling the SDA to low at the 9th SCL clock cycle. when receive ACK bit, master send the address which would be written to slave. The slave responds an ACK if the received address is valid. In the following, the master transmits one or more than one data byte to the slave. After each data transfer completed, the master waits for the ACK from the slave. In the end, the master generates a STOP signal to terminate the data transmission.

Read mode

Data transmission start when master generate a START signal. First byte after the START signal is called slave address. This is a 7-bits salve address followed by a R/W bit (set R/W bit as 0 because sending data to slave). when slave address transfer is completed, only the slave (as a receiver) with an address that matches the address transmitted by master will respond by returning an ACK bit by pulling the SDA to low at the 9th SCL clock cycle. when

receive ACK bit, master generate a Repeated START for increasing the time for the slave to prepare data. After Repeated START, the following byte is content 7-bit slave address and R bit (set R bit as 1 for read data). The slave will respond if the slave address is valid. In the following, the slave transmits one or more than one data byte to the master. After each data transfer completed, the master will generate a NACK (ACK inverted) bit or generates a STOP signal to terminate the data transmission.

Slave Address

To communicate with the FE8116x, the master device must first address devices through a 7-bit device address, a direction bit indicating the intent of executing a read or write operation.

Timing Diagram

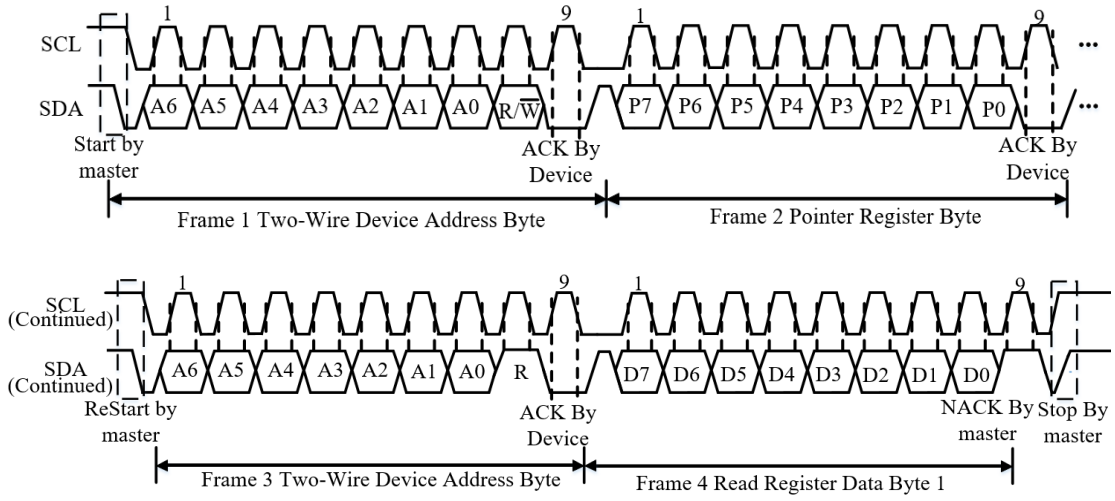


Figure. Two-Wire Timing Diagram for Read Word Format

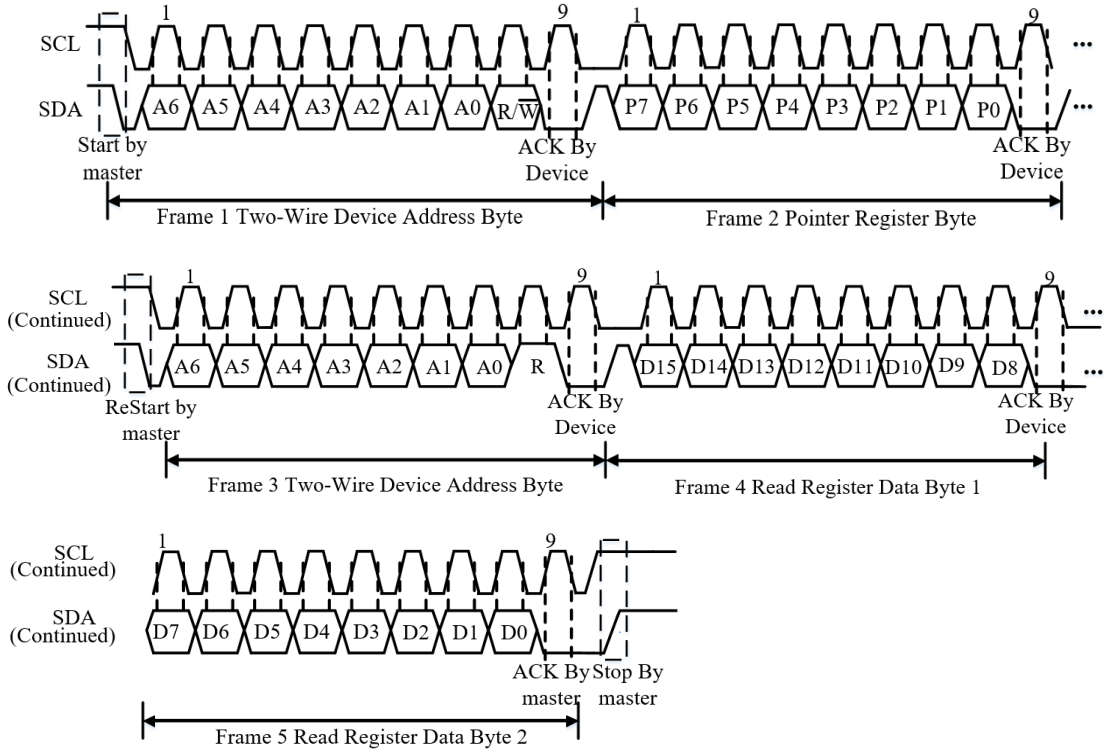


Figure. Two-Wire Timing Diagram for Read Word Format

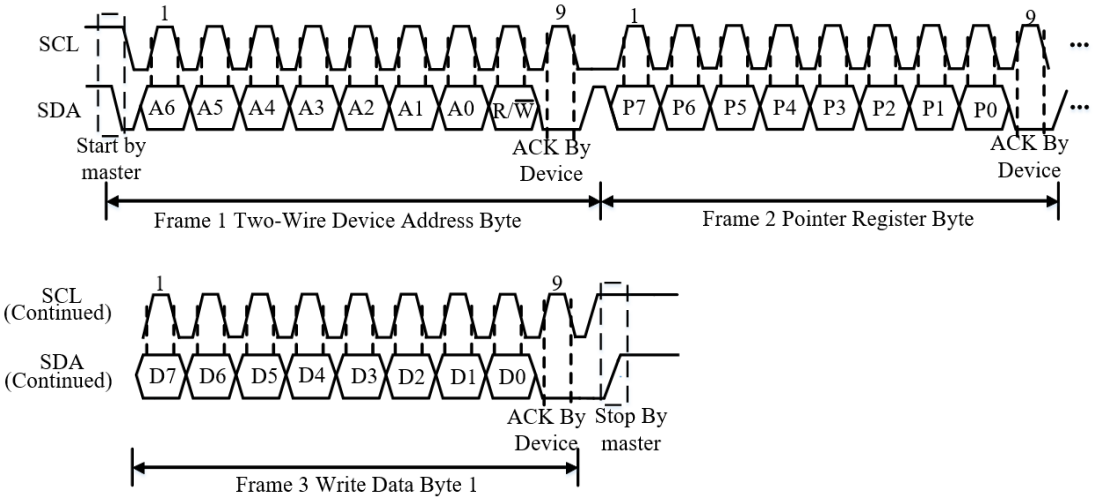


Figure. Two-Wire Timing Diagram for Write Word Format

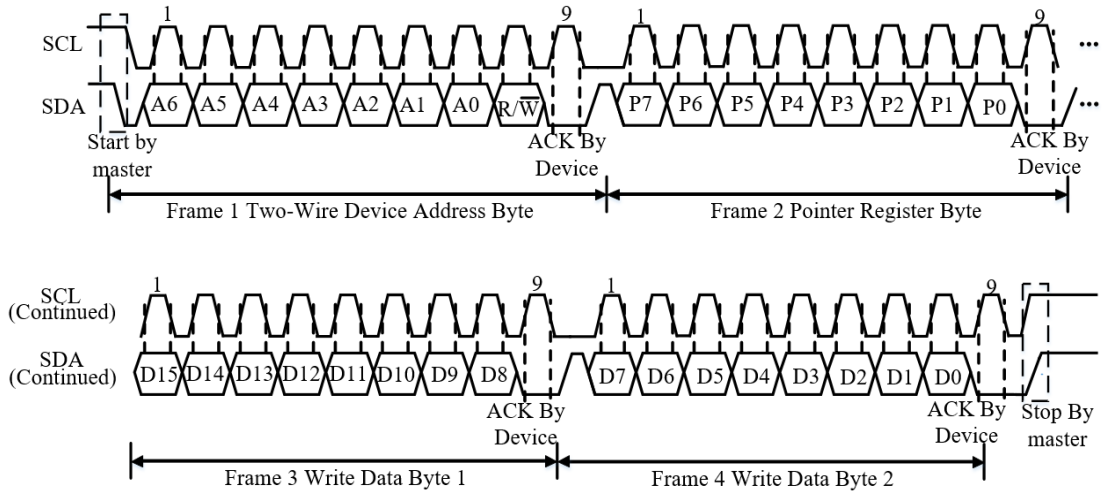


Figure. Two-Wire Timing Diagram for Write Word Format

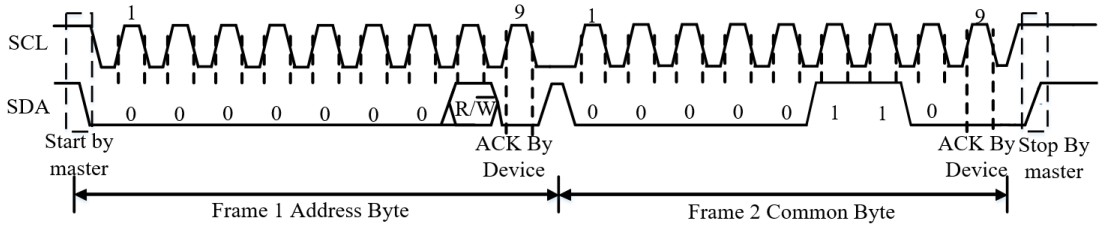


Figure. General-Call Reset Command Timing Diagram

Clocks

There are different clock sources for device operation, including HSRC, LSRC and XTAL. The versatile clock sources offer multi-functions and various application requirements. The optimized clock sources in multi-features can be achieved in saving power consumption. The oscillator source can be selected through ENXTAL, ENSHRC and ENLSRC bits in ENCLK register.

The internal HSRC oscillator runs at 12MHz or 8MHz which provides the master clock source of FE8116x. A FSET bit in ENCLK register is selected for 12MHz or 8MHz of HSRC frequency. The default clock source will be operated in specified value in factory-trimmed accuracy for ±1%. The master clock source can be power-down by ENHSRC=0.

LSRC is a low-speed oscillator for power-saving operation mode. It generates an internal 32KHz clock for watch-dog timer and bas interrupts.

User could use external crystal oscillator by external bias resistor and load capacitors in different oscillator frequency and supplier for the purpose of high precision clock requirements. There is a crystal selection bit XTALSEL in clock configuration register, which is used to select the crystal oscillator type. If designer uses the MHz crystal, please set the XTALSEL=0, else if the crystal is KHz-order, sets the XTALSEL=1 for optimized performance. We recommend using a 1MΩ resistor if the crystal oscillates higher than 4MHz and 10MΩ resistor if it is 32768Hz oscillator.

Clock sources	Frequency	ENHSRC	ENLSRC	ENXTAL	FSET	XTALSEL
HSRC	12MHz	1	0	0	0	0
	8MHz	1	0	0	1	0
LSRC	32KHz	0	1	0	0	0
XTAL	MHz	0	0	1	0	0
	KHz	0	0	1	0	1

GPIO

The FE8116x supports 5 GPIO modes includes digital input mode, push-pull mode, open-drain mode, open-drain with internal pull-up mode, and high-impendence mode for analog I/O. There are 4 GPIO ports which are combo-pins wherein the I/Os are multiple functions by configuring PxCTL0 and PxCTL1 bits in GPIO control table.

Layout Note and Grounding Guidelines

The FE8116x has a single power supply, VDD and VSS. The analog circuit is powered by VDDA which supplied from internal LDO with external filtering capacitor to immune the system noise. The digital circuit is powered by VDD which could protect and isolate the digital switching noise to interfere the analog circuits and minimizing coupling between analog power and digital power sections. Decoupling capacitors are important when FE8116x operates in high resolution data conversion. The VDDA pin is referenced to VSSA pin with dual decoupling capacitor. Decouple VDDA with a 1.5uF capacitor in parallel with a 0.1uF capacitor to VSSA. The higher decoupling capacitor value could use as a power supply tank and lower-order capacitor to high-frequency noise filtering. Referring to VDDA power lines, the digital power lines VDD pin is reference to VSS pin as the same function and connection with VDDA and VSSA pins. The power lines are necessary to use as wide trace as possible to have lower impedance path to reduce the voltage drop and glitches on power lines.

The analog signal inputs and reference voltage input are differential and referred to common-mode voltage. There is a common-mode voltage filtering capacitor pin to filtering out the high-frequency noises. Because of differential input signals, the high common-mode rejection of the FE8116x removes common-mode noise on the analog input signals. The analog ground plane should route as large as possible under FE8116x to ensure that the noisy signal will not couple into the device. Designer should avoid to routing digital signals under the device or running in parallel in sensitive signals because these traces will couple noise into the device or analog and reference signals.

The sigma-delta modulator architectures implement oversampling and using noise shaping techniques to move the low-frequency noise power forward to higher frequency band. The digital filter after modulator removes the noise power from the low-frequency analog and reference inputs. The notch frequency of digital filter is configurable adapting to different applications which immune to noise interference than conventional Nyquist rate data converters. Because of high resolution and low noise levels from FE8116x, care must be taken regarding grounding placement and layout floorplan.

The ground and power traces around FE8116x should be separated on PCB which is sensitive to any switching noise. With large ground planes with multi-through holes and shorter return path to reduce the ground impedance could minimize the disturbance voltage. Also, the shielding technique could protect the sensitive analog input and reference input signals from noisy environment. Digital interface clock and data signals are fast switching traces, using ground shield to prevent radiating noise to other sections of the PCB. Please be noted that never run digital signals near the analog and reference input signals. Double-sided board with large ground plane is preferred to have the best performance.

The layout engineer must ensure that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

ADC Output Data Rate Configuration Registers

0xE618	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
FIRCFG	—	—	—	—	OSR[3]	OSR[2]	OSR[1]	OSR[0]
R/W	—	—	—	—	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register	Address	R/W	Description	Default
FIRCFG	0xE618	R/W	FIR digital filter decimation ratio	0x00

Bits	Bit Name	Description
[7:4]	NC	No connected
[3:0]	OSR[3:0]	**Decimation ratio of digital filter** 0000：32768 0001：16384 0010： 8192 0011： 4096 0100： 2048 0101： 1024 0110： 512 0111： 256 1111： 128

Multiplexing Configuration Registers

0xE619	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
MUXSIG	ENMUXS	—	INL[2]	INL[1]	INL[0]	INH[2]	INH[1]	INH[0]
R/W	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register	Address	R/W	Description	Default
MUXSIG	0xE619	R/W	Input signal channel multiplexer	0x00

Bits	Bit Name	Description
[7]	ENMUXS	**Input signal channel multiplexer control** 0：Disabled 1：Enabled
[6]	NC	No connected
[5:3]	INL[3:0]	**Inverting signal input channel** 000：CH0 001：CH1 010：CH2 011：CH3 100：CH4 101：CH5 110：CH6 111：CH7
[2:0]	INH[3:0]	**Non-Inverting signal input channel** 000：CH0 001：CH1 010：CH2 011：CH3 100：CH4 101：CH5 110：CH6 111：CH7

Reference Signal Multiplexing Configuration Register

0xE61A	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
MUXREF	ENMUXR	—	—	—	VRL[1]	VRL[0]	VRH[1]	VRH[0]
R/W	R/W	—	—	—	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
MUXREF	0xE61A	R/W	Reference channel multiplexer	0x00

Bits	Bit Name	Description
[7]	ENMUXR	**Reference signal channel multiplexer control** 0：Disabled 1：Enabled
[6:4]	NC	No connected
[3:2]	VRL[1:0]	**Inverting signal input channel** 00：CH0 01：CH1 10：CH2 11：CH3
[1:0]	VRH[1:0]	**Non-Inverting signal input channel** 00：CH0 01：CH1 10：CH2 11：CH3

Signal Buffering Configuration Register

0xE61B	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
BUFCFG	—	VRBUF	PGACH	ENPGA	—	PGA[2:0]		
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
BUFCFG	0xE61B	R/W	Input buffer configuration	0x00

Bits	Bit Name	Description
[7]	NC	No connected
[6]	VRBUF	**Reference input buffer control** 0：reference inputs connect to ADC directly 1：reference inputs by input buffers
[5]	PGACH	**PGA amplifier chopper control** 0：PGA chopper disabled 1：PGA chopper enabled
[4]	ENPGA	**PGA amplifier control** 0：PGA disabled 1：PGA enabled
[3]	NC	**No connected**
[2:0]	PGAGN[2:0]	**PGA amplifier gain configuration** 000：1X 001：2X 010：4X 011：8X 100：16X 101：32X 110：64X 111：128X

ADC Input Signal Scaling Configuration

0xE61C	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
ADCCFG	ENADC	ADCCH	VRGN[1]	VRGN[0]	ADCGN[3]	ADCGN[2]	ADCGN[1]	ADCGN[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
ADCCFG	0xE61C	R/W	ADC parameters configuration	0x00

Bits	Bit Name	Description
[7:6]	ENADC	**ADC conversion control** 00：ADC disabled 11：ADC enabled
[5:4]	VRGN[1:0]	**Reference voltage gain configuration** 00：1X 01：0.50X 10：0.75X 11：0.25X
[3:0]	ADCGN[3:0]	**Sigma-delta modulator input gain configuration** 0000：1X 0001：2X 0011：4X 0111：8X 1111：16X

DC Offset Configuration Register

0xE61D	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
DCCFG	—	—	—	—	—	DCSET[2]	DCSET[1]	DCSET[0]
R/W	—	—	—	—	—	R/W	R/W	R/W

Register	Address	R/W	Description	Default
DCCFG	0xE61D	R/W	DC offset configuration	0x00

Bits	Bit Name	Description
[7:3]	NC	**No connected**
[2:0]	DCSET[2:0]	**Modulator input offset configuration** 000：No offset 001：1/16Vref 010：2/16Vref 011：3/16Vref 100：4/16Vref 101：5/16Vref 110：6/16Vref 111：7/16Vref

Reference and TEMP Sensor Configuration Register

0xE61E	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
REFCNG	—	—	—	—	—	ENDEM	TSCH	ENVREF
R/W	—	—	—	—	—	R/W	R/W	R/W

Register	Address	R/W	Description	Default
REFCFG	0xE61E	R/W	Reference voltage generator	0x00

Bits	Bit Name	Description
[7:3]	NC	**No connected**
[2]	ENDEM	**VREF dynamic element matching control** 0：DEM disabled 1：DEM enabled
[1]	TSCH	**Temperature chopper function control** 0：TEMP sensor chopper disabled 1：TEMP sensor chopper enabled
[0]	ENVREF	**Reference voltage generator control** 0：VREF disabled 1：VREF enabled

ADC Data Ready Interrupt Configuration Register

0xE61F	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
INTSTA	INTFG	—	—	—	—	—	—	ENINT
R/W	R	—	—	—	—	—	—	R/W

Register	Address	R/W	Description	Default
INTSTA	0xE61F	R/W	ADC data conversion ready interrupt flag	0x00

Bits	Bit Name	Description
[7]	INTFG	**Data ready interrupt flag** 0：A/D data converting 1：A/D data ready
[6:1]	NC	**No connected**
[0]	ENINT	**Data ready interrupt control** 0：Data ready flag disabled 1：Data ready flag enabled

Input Signal Network Configuration Register

0xE680	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
INCH	—	—	—	—	—	INCH[1]	INCH[0]	—
R/W	—	—	—	—	—	R/W	R/W	—

Register	Address	R/W	Description	Default
INCH	0xE680	R/W	Signal input configuration	0x00

Bits	Bit Name	Description
[7:3]	NC	**No connected**
[2:1]	INCH[1:0]	**Input signal architecture configuration** 00：INH connects to SDM+ and INL connects to SDM- 01：INL connects to SDM+/SDM- 10：INH connects to SDM+/SDM- 11：INH connects to SDM- and INL connects to SDM+
[0]	NC	**No connected**

Comparator Configuration Registers 1

0xE800	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
CMPCFG	HYS[2]	HYS[1]	HYS[0]	VTH[1]	VTH[0]	ENINT	ENCMPH	ENCMPR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
CMPCFG	0xE800	R/W	Comparator Configuration 1	0x00

Bits	Bit Name	Description
[7:5]	HYS[2:0]	**Hysteresis Comparator input Offset Voltage** 000：Minimum hysteresis level 111：Maximum hysteresis level
[4:3]	VTH[1:0]	**R2R Comparator Internal Reference Voltage Configuration** 00：180mV 01：260mV 10：350mV 11：430mV
[2]	ENINT	**Internal Reference Voltage Control** 0：Internal Reference Disabled 1：Internal Reference Enabled
[1]	ENCMPH	**Hysteresis Comparator Control** 0：Hysteresis Comparator Disabled 1：Hysteresis Comparator Enabled
[0]	ENCMPR	**Rail-to-Rail Comparator Control** 0：R2R Comparator Disabled 1：R2R Comparator Enabled

Comparator Configuration Registers 2

0xE801	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
CMOUT	—	—	—	—	—	—	—	CMPOUT
R/W	—	—	—	—	—	—	—	R

Register	Address	R/W	Description	Default
CMPOUT	0xE801	R/W	Comparator Flag	0x00

Bits	Bit Name	Description
[7:1]	NC	**No connected**
[0]	CMPOUT	**Comparator Output Flag** 0：Non-inverting terminal input voltage less than Inverting terminal input voltage 1：Non-inverting terminal input voltage greater than Inverting terminal input voltage

LVD Configuration Register

0xE802	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
LVCFG	LVDF	LVD[2]	LVD[1]	LVD[0]	LVR[1]	LVR[0]	ENLVD	ENLVR
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
LVCFG	0xE802	R/W	Low-voltage configuration register	0x00

Bits	Bit Name	Description
[7]	LVDF	Low voltage detector flag
[6:4]	LVD[2:0]	**LVD voltage level configuration** 000：3.0V 001：2.8V 010：2.6V 011：2.4V 100：2.2V 101：2.0V 110：1.8V 111：1.6V
[3:2]	LVR[1:0]	**LVR voltage level configuration** 00：2.6V 01：2.4V 10：2.2V 11：2.0V
[1]	ENLVD	**LVD enabled** 0：Disable 1：Enable
[0]	ENLVR	**LVR enabled** 0：Disable 1：Enable

LVD Interrupt Registers

0xE803	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
LVDINT	—	—	—	—	—	—	—	ENLVDINT
R/W	—	—	—	—	—	—	—	R/W

Register	Address	R/W	Description	Default
LVDINT	0xE803	R/W	Low-voltage interrupt register	0x00

Bits	Bit Name	Description
[7:1]	—	NC
[0]	ENLVDINT	**LVD interrupt function enabled** 0：Disable 1：Enable

POWER Configuration Registers

0xE804	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
PWRCFG	—	ENOP	ENBODN	ENBODP	ENPDET	ENVCM	ENLDO	ENCHIP
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
PWRCFG	0xE804	R/W	Chip Function Enable Configuration	0x00

Bits	Bit Name	Description
[7]	NC	No connected
[6]	EMOP	**Internal Rail-to-Rail Operational Amplifier** 0：Disabled 1：Enabled
[5]	ENBODN	**Sinking current of Sensor Diagnostic** 0：Disabled 1：Enabled
[4]	ENBODP	**Sourcing current of Sensor Diagnostic** 0：Disabled 1：Enabled
[3]	ENPDET	**Power Supply Monitoring Control** 0：Disabled 1：Enabled
[2]	ENVCM	**Common-mode Voltage Generator Control** 0：Disabled 1：Enabled
[1]	ENLDO	**LDO Enable Control** 0：Disabled 1：Enabled
[0]	ENCHIP	**Chip Enable Control** 0：Disabled 1：Enabled

IDAC Channel Configuration Register

0xE805	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
IDACCTL	—	—	—	PSW	IDAC2N	IDAC1N	IDAC2P	IDAC1P
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
IDACCTL	0xE805	R/W	IDAC control register	0x00

Bits	Bit Name	Description
[7:5]	NC	No connected
[4]	PSW	**Sensor power path switch** 0：PSW switch turn-off 1：PSW switch turn-on
[3]	IDAC2N	**IDAC2 output selection** 0：IDAC2 disconnects to AN6 1：IDAC2 connects to AN6
[2]	IDAC1N	**IDAC1 output selection** 0：IDAC1 disconnects to AN6 1：IDAC1 connects to AN6
[1]	IDAC2P	**IDAC2 output selection** 0：IDAC2 disconnects to AP6 1：IDAC2 connects to AP6
[0]	IDAC1P	**IDAC1 output selection** 0：IDAC1 disconnects to AP6 1：IDAC1 connects to AP6

IDAC1 Output Current Configuration Register

0xE806	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
IDAC1	ENIDAC1	IDAC1[6]	IDAC1[5]	IDAC1[4]	IDAC1[3]	IDAC1[2]	IDAC1[1]	IDAC1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
IDAC1	0xE806	R/W	IDAC1 current excitation source	0x00

Bits	Bit Name	Description
[7]	ENIDAC1	**IDAC1 enabled** 0：Disable 1：Enable
[6:0]	IDAC1[6:0]	**IDAC1 excitation current output** 0000000：10uA 0000001：18uA 0000010：30uA 0000100：55uA 0001000：100uA 0010000：180uA 0100000：340uA 1000000：600uA ……. 11111111：1.2mA

IDAC2 Output Current Configuration Register

0xE807	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
IDAC2	ENIDAC2	IDAC2[6]	IDAC2[5]	IDAC2[4]	IDAC2[3]	IDAC2[2]	IDAC2[1]	IDAC2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
IDAC2	0xE807	R/W	IDAC2 current excitation source	0x00

Bits	Bit Name	Description
[7]	ENIDAC2	**IDAC2 enabled** 0：Disable 1：Enable
[6:0]	IDAC2[6:0]	**IDAC2 excitation current output** 0000000：10uA 0000001：18uA 0000010：30uA 0000100：55uA 0001000：100uA 0010000：180uA 0100000：340uA 1000000：600uA ……. 11111111：1.2mA

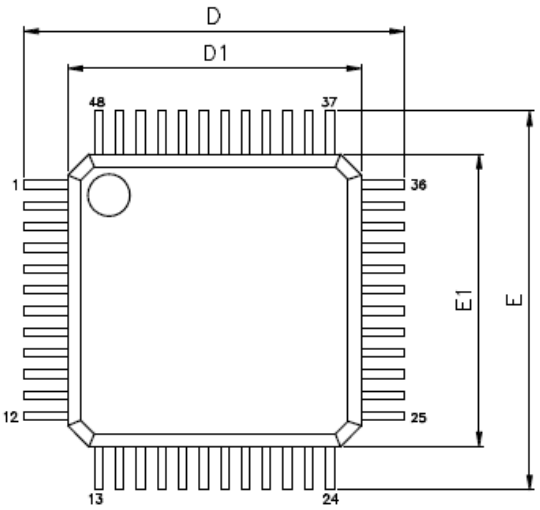
LCD Configuration Register

0xF200	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
LCMCTL	—	ENBUF	—	LEVEL	VCTR[3]	VCTR[2]	VCTR[1]	VCTR[0]
R/W	—	R/W	—	R/W	R/W	R/W	R/W	R/W

Register	Address	R/W	Description	Default
LCMCTL	0xF200	R/W	LCM Function Configuration	0x00

Bits	Bit Name	Description
[7]	NC	No connected
[6]	EMBUF	**LCD Output Driver Control** 0：Output Driver Disabled 1：Output Driver Enabled
[5]	NC	No connected
[4]	LEVEL	**LCD Bias Voltage Configuration** 0：1/3 Bias 1：1/2 Bias
[3:0]	VCTR[3:0]	**LCM Contrast Adjustment** 0000：No Contrast Skew ……. 1111：Maximum Contrast Skew

Package Outline Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°