32-bit ARM® Cortex™-M0+ MCU With 3-Channel 20-Bit 1KSPS Low Noise, Low Power AFE

Features

MCU Block

- Core:32-bit ARM ® Cortex™-M0+ CPU
  - 24 MHz maximum frequency
  - support 0 wait state access
- Memories
  - 64Kbytes Flash
  - 4KB SRAM
- Power Supply: 2.7V~3.6V
- Operation temperature: (-40~85°C)
- Low Voltage Detector (LVD) / Voltage Comparator (VCMP)
- Clock management
  - 4 ~24MHz External high speed clock(HSE)
  - 4 ~24MHz Internal high speed clock(HIS)
  - 32.768KHz External low speed clock(LSE)
  - 38.4/32.768KHz Internal low speed clock(LSI)
- Three operation: run mode, sleep mode, deep sleep mode
- Maximum 16 I/O ports
- Debug mode
  - Serial wire debug (SWD) , 2 watch points/4 break points
- 128-bit unique ID
- 6 communication interfaces
  - Up to 2 UART
  - 1 LPUART
  - 1 SPI
  - 1 I2C
  - one 1-wire
- Buzzer generator
- Up to 10 timers
  - 1 16-bit advanced timers ，3 pairs of complementary outputs
  - 1 16-bit general purpose timer
  - 1 16-bit programmable timer
  - Up to two 16/32bit basic timer
  - 2 watchdog timers (Independent and Window)
  - 1 16-bit low power timer
  - 1 SysTick timer
  - 1 8-bit automatic wake-up timer
- RTC clock counter(record the year, month, day, hour, minute and second)
- One 12-bit ADC(SAR)
  - Max convert rate: 1Msps
  - Maximum 16 channels
- CRC-16 calculation Unit

AFE Block

- 2.7V to 3.6V operation voltage range
- Up to 20 bits ENOB
- RMS noise
  - 1.14uV RMS noise @4Hz, PGA=1X
  - 82nV RMS noise @ 4Hz, PGA=128X
- 300uA ultra-low current consumption
- 6uA (typ.) standby-mode current
- ADC I/O Channels
  - 3CH fully differential analog input channels
  - 2CH fully differential VREF input channels
- Internal temperatures sensor
- Power supply voltage detector
- Sensors burn-out diagnostic
- Internal precision clock oscillator
- 2-stage Programmable gain amplifier
  - x1 ~ x128 1st-stage gain
  - x1 ~ x16 2nd-stage gain
- Programmable 2x IDACs current sources
- -40 ~ 85℃ operation temperature
- 4Hz to 1KHz data rates

Content

MCU Block Diagram

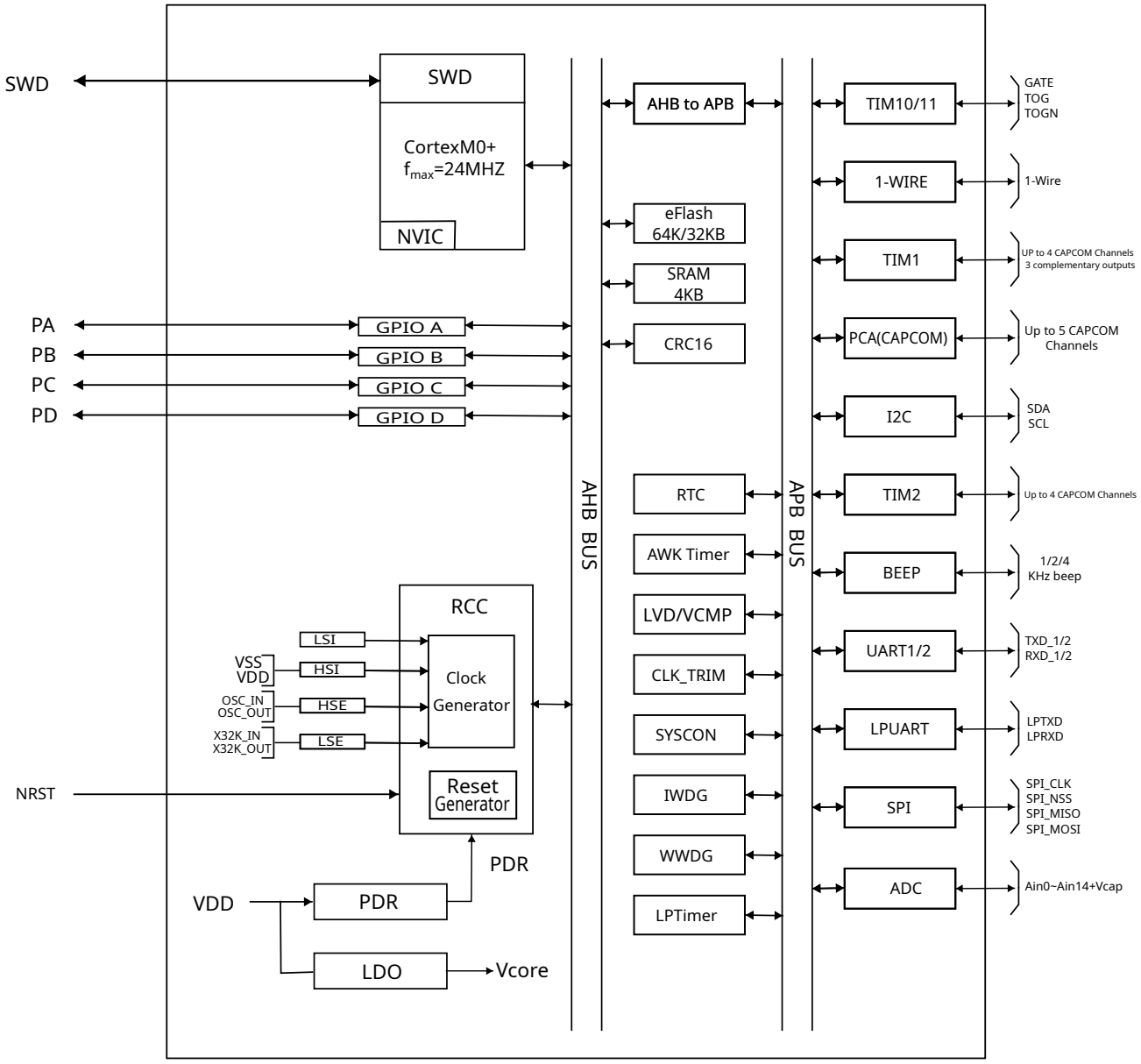


Figure1. MCU Block Diagram of FE82160

AFE Block Diagram

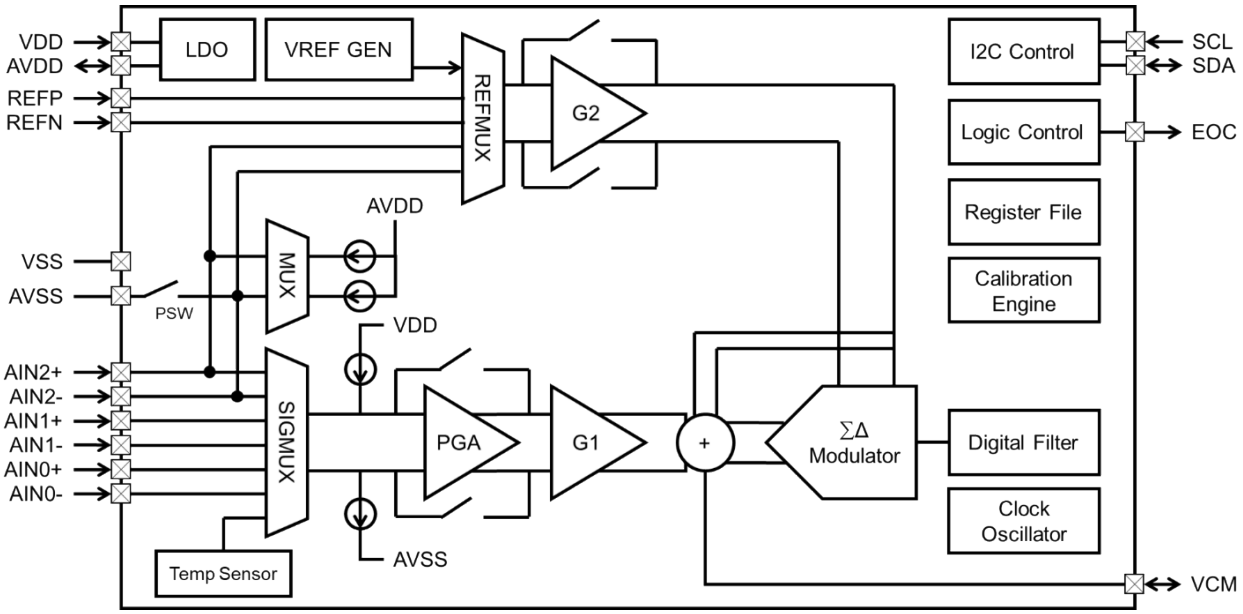


Figure 2. AFE Block Diagram

Package Outline and Pin Configuration

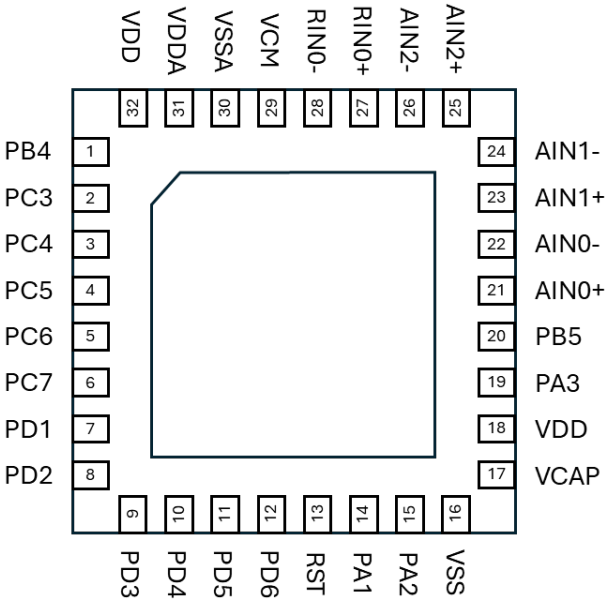


Figure 3. FE82160 Pin Configuration (QFN32 4x4)

Table. QFN32-4x4 pins

Pin	Name	Type	Function
1	SCL/PB4	X32K_OUT	32K Clock source output
		PB4	PB4 GPIO
		LPTIM_GATE	LPTIM gating
		PCA_ECI	PCA External clock
		SPI_NSS	SPI module slave chip selects signals
		I2C_SCL	I2C clock
		UART1_TX	UART1 TX
		TIM11_TOGN	TIM11 Toggle inverting output
		SCL	AFE I2C digital interface clock input
2	PC3/EOC	PC3	PC3 GPIO
		TIM1_CH3	TIM1 PWM output 3
		TIM1_CH1N	TIM1 PWM output 1 Inverting
		I2C_SDA	I2C data
		UART2_TX	UART2 TX
		PCA_CH1	PCA Input capture/Output compare 1
		1-WIRE	1-wire Input/output
		TIM2_CH3	TIM2 Input capture/Output compare 3
		AIN1	ADC Analog input channel 1
		EOC	AFE Data converter end of conversion interrupt
3	PC4	PC4	PC4 GPIO
		TIM1_CH4	TIM1 PWM output 4
		TIM1_CH2N	TIM1 PWM output 2 Inverting
		I2C_SCL	I2C clock
		UART2_RX	UART2 RX
		PCA_CH0	PCA Input capture/Output compare 0
		CLK_MCO	CPU Clock output
		TIM2_CH4	TIM2 Input capture/Output compare 4
		AIN2	ADC Analog input channel 2
4	PC5	PC5	PC5 GPIO
		TIM1_BKIN	TIM1 Brake signal input
		PCA_CH0	PCA Input capture/Output compare 0
		SPI_CLK	SPI Module clock signal
		LPUART_TX	LPUART TX
		TIM11_GATE	TIM11 gating
		LVD_OUT	Low voltage detection comparator output
		TIM2_CH1	TIM2 Input capture/Output compare 1
		VCMPIN1	Analog input

Pin	Name	Type	Function
5	PC6	PC6	PC6 GPIO
		TIM1_CH1	TIM1 PWM output 1
		PCA_CH3	PCA Input capture/Output compare 3
		SPI_MOSI	SPI module host output slave input signal
		LPUART_RX	LPUART RX
		TIM11_EXT	TIM11 External pulse input
		CLK_MCO	CPU Clock output
		TIM2_CH4	TIM2 Input capture/Output compare 4
		AIN0	ADC Analog input channel 0
6	PC7	SWDIO	SWD IO
		PC7	PC7 GPIO
		TIM1_CH2	TIM1 PWM output 2
		PCA_CH4	PCA Input capture/Output compare 4
		SPI_MISO	SPI module host input slave output signal
		UART2_RX	UART2 RX
		LSI_OUT	Internal low frequency RC clock 38.4KHZ output
		X32K_OUT	External low frequency crystal output
7	PD1	SWDCLK	SWD clock
		PD1	PD1 GPIO
		PCA_ECI	PCA External clock
		UART2_TX	UART2 TX
		HSE_OUT	Internal high frequency RC clock 24MHZ output
		VCMP0_OUT	VCMP0 output
8	PD2	PD2	PD2 GPIO
		TIM1_CH2	TIM1 PWM output 2
		PCA_CH2	PCA Input capture/Output compare 2
		SPI_MISO	SPI module host input slave output signal
		RTC_1HZ	RTC 1HZ output
		LPUART_TX	LPUART TX
		LPTIM_TOG	LPTIM Toggle output
		1-WIRE	1-wire Input/output
		TIM2_CH3	TIM2 Input capture/Output compare 3
		VCMPIN0	VCMP input channel 0
		AIN3	ADC Analog input channel 3

Pin	Name	Type	Function
9	PD3	PD3	PD3 GPIO
		TIM1_CH3N	TIM1 PWM output 3 Inverting
		PCA_CH1	PCA Input capture/Output compare 1
		SPI_MOSI	SPI module host output slave input signal
		LSE_OUT	External high frequency crystal output
		UART1_RX	UART1 RX
		LPTIM_TOGN	LPTIM Toggle inverting output
		TIM2_CH2	TIM2 Input capture/Output compare 2
		AIN4	ADC Analog input channel 4
10	PD4	PD4	PD4 GPIO
		TIM1_CH1	TIM1 PWM output 1
		PCA_CH0	PCA Input capture/Output compare 0
		RTC_1HZ	RTC 1HZ output
		TIM10_TOG	TIM10 Toggle output
		UART1_TX	UART1 TX
		TIM10_EXT	TIM10 External pulse
		BEEP	Buzzer output
		TIM2_CH1	TIM2 Input capture/Output compare 1
		VCIN2	VC input channel 2
11	PD5	PD5	PD5 GPIO
		TIM1_CH1N	TIM1 PWM output 1 Inverting
		PCA_CH4	PCA Input capture/Output compare 4
		SPI_MISO	SPI module host input slave output signal
		I2C_SCL	I2C clock
		UART2_TX	UART2 TX
		TIM10_GATE	TIM10 gating
		UART1_TX	UART01 TX
		TIM2_CH4	TIM2 Input capture/Output compare 4
		AIN5	ADC Analog input channel5
12	PD6	PD6	PD6 GPIO
		TIM1_CH2	TIM1 PWM output 2
		PCA_CH3	PCA Input capture/Output compare 3
		SPI_MOSI	SPI module host output slave input signal
		I2C_SDA	I2C data
		UART2_RX	UART2 RX
		LPTIM_EXT	LPTIM External pulse input
		UART1_RX	UART1 RX
		TIM2_CH2	TIM2 PWM output 2

		AIN6	ADC Analog input channel 6

Pin	Name	Type	Function
13	RST	NRST	Reset input port, low valid, chip reset
14	PA1	OSC_IN	External clock source input
		PA1	PA1 GPIO
		TIM1_CH2N	TIM1 PWM output 2 Inverting
		SPI_CLK	SPI Module clock signal
		I2C_SDA	I2C data
		UART1_RX	UART1 RX
		TIM10_TOG	TIM10 Toggle output
		UART2_RX	UART2 RX
15	PA2	OSC_OUT	External clock source output
		PA2	PA2 GPIO
		TIM1_CH3	TIM1 PWM output 3
		SPI_NSS	SPI module slave chip selects signals
		I2C_SCL	I2C clock
		UART1_TX	UART1 TX
		TIM10_TOGN	TIM10 Toggle inverting output
		UART2_TX	UART2 TX
		TIM2_CH2	TIM2 Input capture/Output compare 2
16	VSS	GND	Ground
17	VCAP	Power	LDO kernel power supply (internal circuit use, external capacitor)
18	VDD	Power	power
19	PA3	PA3	PA3 GPIO
		TIM1_CH3N	TIM1 PWM output 3 Inverting
		PCA_CH2	PCA Input capture/Output compare 2
		SPI_NSS	SPI module slave chip selects signals
		RTC_1HZ	RTC 1HZ output
		LPUART_RX	LPUART RX
		PCA_ECI	PCA External clock
		VCMP0_OUT	Voltage comparator 0 output
		TIM2_CH3	TIM2 Input capture/Output compare 3
		UART2_TX	UART2 TX

Pin	Name	Type	Function
20	PB5/SDA	X32K_IN	32K Clock source input
		PB5	PB5 GPIO
		TIM1_BKIN	TIM1 Brake signal input
		PCA_CH4	PCA Input capture/Output compare 4
		SPI_CLK	SPI Module clock signal
		I2C_SDA	I2C data
		UART1_RX	UART1 RX
		TIM11_TOG	TIM11 Toggle output
		LVD_OUT	LVD comparator output
		TIM2_CH1	TIM2 Input capture/Output compare 1
		SDA	AFE I2C digital interface data I/O
21	VIP0	Analog input	AFE CH0 differential analog signal input
22	VIN0	Analog input	AFE CH0 differential analog signal input
23	VIP1	Analog input	AFE CH1 differential analog signal input
24	VIN1	Analog input	AFE CH1 differential analog signal input
25	VIP2	Analog input	AFE CH2 differential analog/reference signal input
26	VIN2	Analog input	AFE CH2 differential analog/reference signal input
27	RIP0	Analog input	AFE CH0 differential reference voltage input
28	RIN0	Analog input	AFE CH0 differential reference voltage input
29	VCM	Input	AFE Common-mode voltage regulation
30	AVSS	GND	AFE Analog ground
31	AVDD	Power	AFE Analog power
32	VDD	Power	AFE Digital power

Electrical Characteristics

● AFE

Table. Electrical Characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
I_{VDD}	Supply current	PGA bypass	—	260	310	uA
		PGA mode, gain=1	—	300	350	uA
		Power-down mode	—	6	9	uA
PGA						
PGAGN	PGA Gain setting		1,2,4,8,16,32,64,128			V/V
	RFI filter 3dB frequency	Design guaranteed	—	12.8	—	MHz
VCM_{PGA}	Input common-mode voltage		0.4		AVDD-0.6	V
PERFORMANCE						
	Resolution		—	20	—	bits
ODR	Output data rate		2	—	2000	SPS
V_{OS}	Offset voltage	20 bits resolution	—	1	—	LSB
$V_{OS,TC}$	V_{OS} temperature drift		—	1	—	LSB/℃
GE	Gain error		-1	±0.5	+1	%
CMRR	common-mode rejection ratio	ODR=500SPS@60Hz	—	80	—	dB
PSRR	power-supply rejection ratio	VDD to VSS	—	90	—	dB
R_{PSW}	Sensor switch	I_{PSW} =1mA	8	10	12	Ω
ANALOG INPUTS/OUTPUTS						
V_{AINx}	Absolute input voltage	PGA enabled	Note(1)			
		PGA disabled	AVSS-0.1	—	AVDD+0.1	V
V_{IN}	Differential input voltage	$V_{IN} = V_{AINP} – V_{AINN}$	—	$\pm V_{REF}$/Gain	—	V
V_{AVDD}	LDO output voltage		2.5	2.8	3.1	V
LR_{AVDD}	AVDD load regulation	IOUT=30mA	-1%	—	+1%	%
VCM	Common-mode voltage		-5%	AVDD/2	+5%	V
TC_{VCM}	VCM temperature coefficient	AVDD=3.3V	-4	—	+4	%
REFERENCE INPUTS						
V_{RINX}	Differential reference voltage	$V_{REF} = V_{REFP} – V_{REFN}$	0.3	—	AVDD-AVSS	V
V_{REFP}	Positive reference voltage		V_{REFN} + 0.3	—	AVDD	V
V_{REFN}	Negative reference voltage		AVSS	—	V_{REFP} - 0.3	V
VRGN	Reference voltage ratio	VRGN[1:0]=00	—	1	—	V/V
		VRGN[1:0]=01	—	0.5	—	V/V

		VRGN[1:0]=10	—	0.75	—	V/V
		VRGN[1:0]=11	—	0.25	—	V/V
$VREF_{IN1}$	Internal VREF1	RxMUX[1:0]=10	—	1.2	—	V
$VREF_{IN2}$	Internal VREF2	RxMUX[1:0]=11	—	1.0	—	V
DC INPUT OFFSET						
DCSET	Input DC offset adjustment	DCSET[2:0]=000	—	0	—	V
		DCSET[2:0]=001	—	1/12VREF	—	V
		DCSET[2:0]=010	—	2/12VREF	—	V
		DCSET[2:0]=011	—	3/12VREF	—	V
		DCSET[2:0]=100	—	4/12VREF	—	V
		DCSET[2:0]=101	—	5/12VREF	—	V
		DCSET[2:0]=110	—	6/12VREF	—	V
		DCSET[2:0]=111	—	7/12VREF	—	V
IDAC CURRENT SOURCES (IDAC1, IDAC2)						
IDACx	Current settings@V_{CM} =1.0V	IDACx[6:0]=0000000	—	5	—	uA
		IDACx[6:0]=0000001	—	10	—	uA
		IDACx[6:0]=0000010	—	20	—	uA
		IDACx[6:0]=0000100	—	40	—	uA
		IDACx[6:0]=0001000	-1%	80	+1%	uA
		IDACx[6:0]=0010000	—	160	—	uA
		IDACx[6:0]=0100000	—	320	—	uA
		IDACx[6:0]=1000000	—	700	—	uA
		IDACx[6:0]=1111111	—	1200	—	uA
	Compliance voltage		AVSS	—	AVDD-0.6	V
BURN-OUT CURRENT						
I_{BODP}	Burn-out source current	VDD=3.3V	4	5	6	uA
I_{BODN}	Burn-out sink current	VDD=3.3V	3.5	4.5	5.5	uA
DIGITAL INPUTS/OUTPUTS (SDA, SCL, EOC)						
V_{OL}	Low-level output voltage	I_{SINK}=4mA	—	—	0.4	V
V_{IL}	Low-level input voltage	SDA, SCL	0.7VDD	—	—	V
V_{IH}	Low-level output voltage	SDA, SCL	—	—	0.3VDD	V
I_{LEAK}	Input leakage current	SDA, SCL	—	—	1	uA
INTERNAL CLOCK OSCILLATOR						
F_{CLK}	Master clock frequency	VDD=3.3V	-1%	1.024	+1%	MHz
T_{SUP}	Clock start-up time	VDD=3.3V	1	—	—	ms

INTERNAL TEMPERATURE SENSOR						
	Temperature accuracy	-40 to 85℃	—	± 3	—	℃
	Current consumption		28	32	36	uA
SUPPLY VOLTAGE DETECTOR						
	VDD DIVIDER		0.2	0.25	0.3	V/V
OPERATION TEMPERATURE						
T_A	Ambient temperature		-40	—	85	℃

- **MCU**

Table. DC supply characteristics

Symbol	parameter	Condition			Typical	Max	Unit
I_{DD}(active mode)	Peripheral clock on,code runs from Flash	VDD=3.3V	HSI clock source	4M	468		μA
				8M	839		
				16M	1575		
				24M	2298		
	Peripheral clock off,code runs from Flash	VDD=3.3V	HSI clock source	4M	397		μA
				8M	696		
				16M	1291		
				24M	1871		
	Peripheral clock on,code runs from Flash	VDD=3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	34		μA
	Peripheral clock off,code runs from Flash	VDD=3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	34		μA
	Peripheral clock on,code runs from Flash	VDD=3.3V	HSE clock source	Ta=-40 to 25°C	2556		μA
	Peripheral clock off,code runs from Flash	VDD=3.3V	HSE clock source	Ta=-40 to 25°C	2145		μA
IDD(sleep mode)	Peripheral clock on	VDD=3.3V	HSI clock source	4M	181		μA
				8M	282		
				16M	486		
				24M	689		
	Peripheral clock off	VDD=3.3V	HSI clock source	4M	122		μA
				8M	166		
				16M	252		
				24M	338		
	Peripheral clock on	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	26		μA
	Peripheral clock off	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	25		μA
	Peripheral clock on	VDD =3.3V	HSE 32.768KHzclock source	Ta=-40 to 25°C	884		μA
	Peripheral clock off	VDD =3.3V	HSE 32.768KHzclock source	Ta=-40 to 25°C	534		μA
IDD(Deep sleep mode)	Peripheral clock off,exclude AWK, IWDG, LTIM, RTC	VDD =3.3V	LSE 32.768KHzclock source	Ta=-40 to 25°C	1.20		μA
	Peripheral clock off,exclude IWDG	VDD =3.3V	LSE 32.768KHzclock source	Ta=-40 to 25°C	1.20		μA

symbol	parameter	Condition			Typical	Max	Unit
	Peripheral clock off,exclude LPTIM	VDD =3.3V	LSE 32.768KHzclock source	Ta=-40 to 25°C	1.18		μA
	Peripheral clock off,exclude RTC	VDD =3.3V	LSE 32.768KHzclock source	Ta=-40 to 25°C	1.19		μA
	Peripheral clock off	VDD =3.3V	。	Ta=-40 to 25°C	0.89		μA

Table. Power-on/Power-down reset

Symbol	Parameter	Min	Typical	Max	Unit
V_{POR} V_{BOR}	POR voltage(power-up) BOR voltage(brownout)	2.2	2.25	2.3	V

Table. AC supply current characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OH}	High level output source current	Source 4 mA, VDD = 3.3 V	VDD-0.2		V
		Source 6 mA, VDD = 3.3 V	VDD-0.3		
V_{OL}	Low level output sink current	sink 4 mA, VDD = 3.3 V		VSS+0.2	V
		sink 6 mA, VDD = 3.3 V		VSS+0.3	
V_{OHD}	High level output dual source current	Source 8 mA, VDD = 3.3 V	VDD-0.2		V
		Source 12 mA, VDD = 3.3 V	VDD-0.3		
V_{OLD}	Low level output dual current sink	sink 8 mA, VDD = 3.3 V		VSS+0.2	V
		sink 12 mA, VDD = 3.3 V		VSS+0.3	

Table. Port characteristic - PA, PB, PC, PD

Symbol	Parameter	Condition	VDD	Max	Unit
I_{lkg}	leakage current	V	2.5V / 3.6V	±50	nA

Table. Port PA, PB, PC, PD

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{IT+}	Positive Input Threshold Voltage	VDD=2.5	1.4			V
		VDD=3.3	1.8			V
		VDD=3.6	3			V
V_{IT-}	Reverse Input Threshold Voltage	VDD=2.5			0.9	V
		VDD=3.3			1.3	V
		VDD=3.6			2.4	V
V_{hys}	Input voltage hysteresis (VIT+ - VIT-)	VDD=2.5		0.5		V
		VDD=3.3		0.5		V
		VDD=3.6		0.6		V
$R_{pullhigh}$	Pull-up resistor	pull-up enable	40	50	60	Kohm
C_{input}	input capacitance			5		pf

Table. Timer input sampling requirements

Symbol	Parameter	Condition	Min	Max	Unit
T(int)	external interrupt	External trigger interrupt flag	30		ns
T(cap)	Timer capture time	TIM1/2 capture pulse width f_{systme} =4MHz	0.5		μs
f_{EXT}	Timer clock frequency	TIM1/2/10/11 External clock input Fsystme =4MHz	0	$f_{TIMxCLK}/2$	MHz
$T_{(PCA)}$	PCA clock frequency	PCA External clock input f_{systme} =4MHz	0	$f_{PCACLK}/2$	MHz

Table. Internal High Speed Oscillator（HSI）

Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{MCLK}	Internal Oscillator Frequency		4.0	16	24	MHz
T_{Mstart}	build time	F_{MCLK}=4MHz	2	2.4	4.7	μs
		F_{MCLK}=8MHz	1.15	1.47	3.01	μs
		F_{MCLK}=16MHz	1.04	1.31	2.74	μs
		F_{MCLK}=24MHz	1.1	1.30	2.71	μs
T_{MCLK}	current consumption	F_{MCLK}=4MHz	31	56	113	μA
		F_{MCLK}=8MHz	40	72	151	μA
		F_{MCLK}=16MHz	71	143	298	μA
		F_{MCLK}=24MHz	93	196	383	μA
DC_{MCLK}	duty cycle		45	50	55	%
D_{evM}	frequency deviation	VDD = 2.5V ~ 3.6V TAMP = -40°C ~ 85°C	-2.5	±1	+2.5	%
		VDD = 2.5V ~ 3.6V TAMP = -40°C ~ 50°C	-2.0	±1	+2.0	%

Table. Internal low-speed oscillator (LSI)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{ACLK}	Internal Oscillator Frequency		37.8 32.21	38.4 32.766	38.7 33.26	KHz
T_{Astart}	build time		50	75	150	μs
I_{ACLK}	current consumption		0.2	0.25	0.35	μA
DC_{ACLK}	duty cycle		45	50	55	%
D_{evA}	frequency deviation	VDD = 2.5V ~ 3.6V TAMP = -40°C ~ 85°C	-2.0	±1	+2.0	%
		VDD = 2.5V ~ 3.6V TAMP = -40°C ~ 50°C	-1.5	±1	+1.5	%

Table. External low-speed crystal (LSE)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{SCLK}	Crystal frequency		32.75	32.768	32.78	KHz
ESR_{SCLK}	Equivalent resistance		40	65	85	KOhm
C_{SCLK}	Crystal external load			12(2)		pF
I_{dd}(1)	electric current	ESR=65kOhm C_{SCLK}=12pF	200	250	350	nA
DC_{SCLK}	duty cycle		40	50	60	%
T_{start}	build time	ESR=65kOhm CSCLK=12pF 40%-60%duty cycle		2		s

Table. External High Speed Crystal (HSE)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{FCLK}	Crystal frequency		4	16	24	MHz
ESR_{FCLK}	Equivalent resistance		30	60	1500	Ohm
C_{FCLK}	Crystal external load			12		pF
I_{dd}	electric current	24MHz Crystal ESR=30Ohm CFCLK=12pF		300		μA
D_{CFCLK}	duty cycle		40	50	60	%
T_{start}	build time	4M~24MHz		250		μs

Figure 4. 12 bit A/D Converter

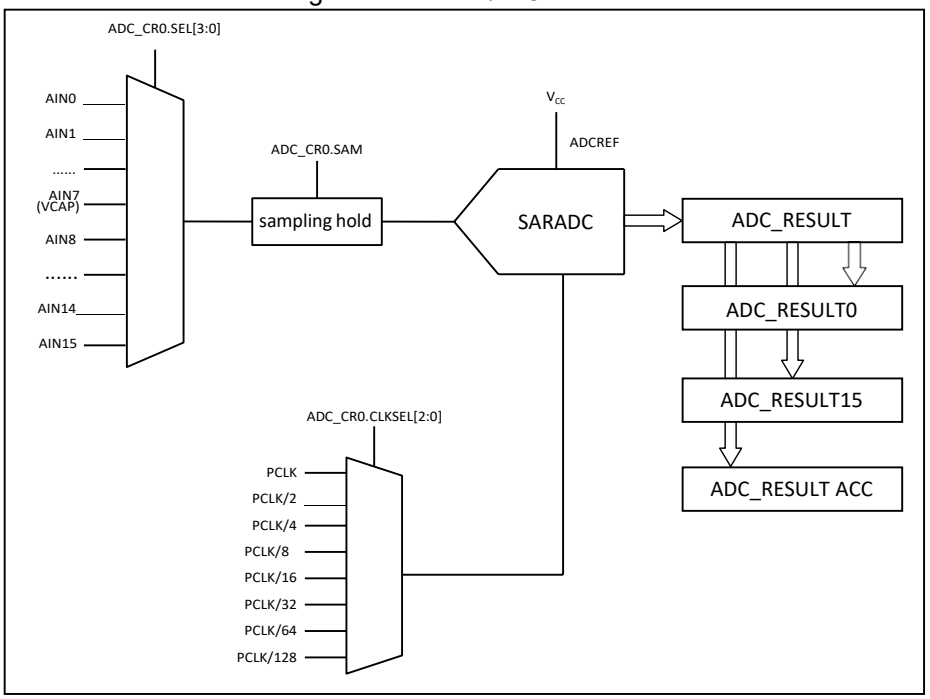


Table. 12 bit A/D Converter

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{ADCIN}	Input voltage range	single ended	0		VDD	V
V_{REF}	reference voltage			VDD		V
I_{ADC}			0.65	0.9	1.23	mA
C_{ADCIN}	input resistance		3.5	4	4.5	pF
F_{ADCCLK}	Clock frequency		0.5	4	16	MHz
$T_{ADCSTART}$	Bias Current Settling Time		2	3	4	μs
$T_{ADCCONV}$	conversion time		16	16	20	cycle
ENOB			10	10.5	11	Bit
DNL	differential nonlinearity		-1.5	±1	1.5	LSB
INL	integral nonlinearity		-2	±1	2	LSB
E_o	bias error		-2	±1	2	LSB
E_g	gain error		-2	±1	2	LSB

Figure 5. Analog Voltage Comparator

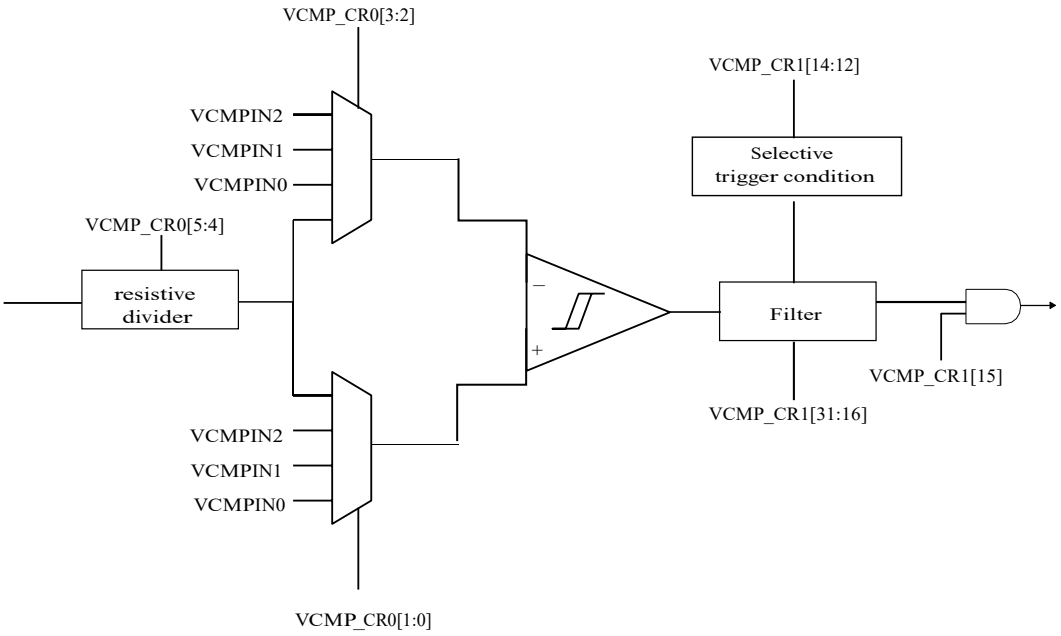


Table. Analog Voltage Comparator

Symbol	Parameter	Min	Typical	Max	Unit
V_{in}	Input voltage range	0		3.6	V
V_{incom}	Input Common Mode Range	0		3.6	V
V_{offset}	input bias	-10	±5	+10	mV
I_{comp}	comparator current		12		μA
$T_{response}$	Comparator Response		5		μs

Figure 6. Low voltage detection

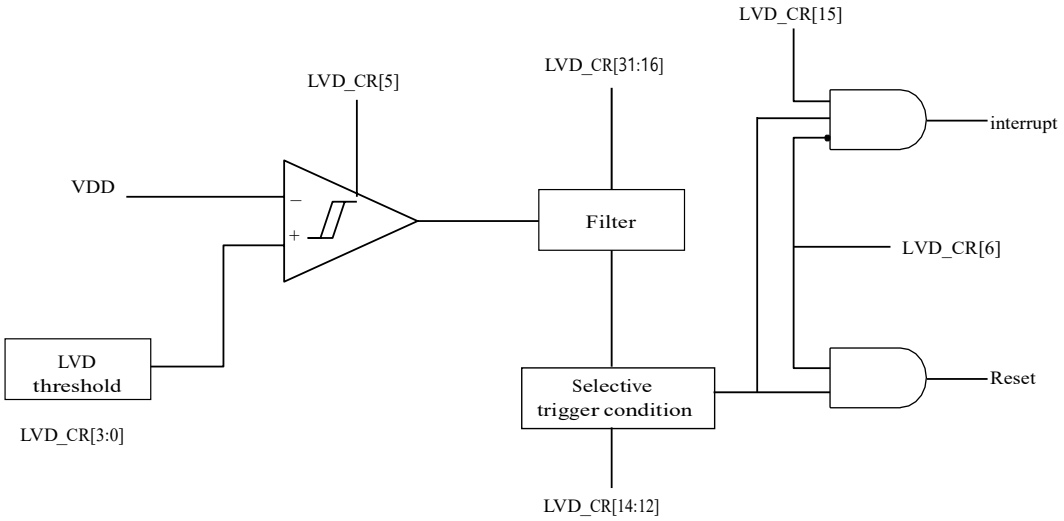


Table. Low voltage detection characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{level}	VDD detectable Threshold (TSSOP20, QFN20, SOP20)	LVD_CR[3:0] = 0000 LVD_CR[3:0] = 0001 LVD_CR[3:0] = 0010 LVD_CR[3:0] = 0011 LVD_CR[3:0] = 0100 LVD_CR[3:0] = 0101 LVD_CR[3:0] = 0110 LVD_CR[3:0] = 0111	Typ -0.1	4.4 4.0 3.6 3.3 3.1 2.9 2.7 2.5	Typ+0.1	V
V_{level}	VDD detectable Threshold (LQFP32 QFN32)	LVD_CR[3:0] = 0000 LVD_CR[3:0] = 0001 LVD_CR[3:0] = 0010 LVD_CR[3:0] = 0011 LVD_CR[3:0] = 0100 LVD_CR[3:0] = 0101 LVD_CR[3:0] = 0110 LVD_CR[3:0] = 0111 LVD_CR[3:0] = 1000 LVD_CR[3:0] =1001 LVD_CR[3:0] = 1010 LVD_CR[3:0] = 1011 LVD_CR[3:0] = 1100 LVD_CR[3:0] = 1101 LVD_CR[3:0] =1110 LVD_CR[3:0] =1111	Typ-0.1	4.6 4.4 4.2 4.0 3.8 3.6 3.4 3.2 3.0 2.8 2.6 Reserved Reserved Reserved Reserved Reserved	Typ+0.1	V
I_{comp}	Detection current		1	1.5	2	μA
$T_{response}$	VDD response time of monitor after falling below or above threshold		30	50	80	μs
T_{setup}	Monitor build time		3	5	10	μs

Table. Flash memory characteristics

Symbol	Parameter	Min	Typical	Max	Unit
EC_{flash}	block erase	20K			one
RET_{flash}	data retention	20			year
T_{prog}	byte programming			20	μs
$T_{Sector-erase}$	block erase			8	ms
$T_{Chip-erase}$	Full Chip Erase	20		40	ms

Table. Low power mode wakeup

Symbol	Parameter	Condition	Min	Typical	Max	Unit
T_{wakeup}	Deep Sleep to operation	4M	11.8	12.5	12.8	μs
		8M	11.3	11.6	12.5	
		16M	11.2	11.4	12.0	
		24M	10.5	11.3	11.8	

Description

● Analog Front End (AFE)

The FE82160 has a 3-channel, low noise, ultra-low power 20-bit sigma-delta analog-to-digital data converter for high precision measurement applications. Embedding with on-chip temperature sensor, supply voltage detector, the device can monitor environment conditions dynamically for self-data calibration. Operating with internal calibrated precisely 1MHz clock oscillators, no extra external crystal oscillator needed for BOM and area saved.

The FE82160 builds up 2-stage programmable PGA gain amplifiers. The gain of ach amplifier could be configured independently. The 1st-stage gain could program from x1 to x128 and the 2nd stage could program from x1 to x16. User could allocate the gain in each stage to acquire the low-noise and supreme stable analog signals.

The devices contain 3 external independent differential input signals, and 2 external independent reference voltages. Two on-chip IDACs on-chip could source independent currents to stimulate external sensor devices to generate electricalsignals.

The FE82160 is an oversampling sigma-delta data converter with a decimation filter to decimate the output data from modulator. The configurable output data rate from 4Hz to 1KHz, tradeoff the resolution and conversion speed in applications requirements.
The parts operate with a power supply from 2.5V to 3.6V. The data transacts through standard I2C digital interface with MCU. The device consumes 300uA ultra-low current consumption in typical.

➢ System Description

The AFE is a low-noise, low power 20-bit ΣΔ ADC that offers many integrated features to reduce system BOM cost and component counts in measuring sensor signals. The device has 2 conversion modes, one-shot conversion and continuous conversion mode. Data can be read at any time if EOC signal is interrupted, it could avoid to access the corruption data and always reflect the most recently completed conversion.

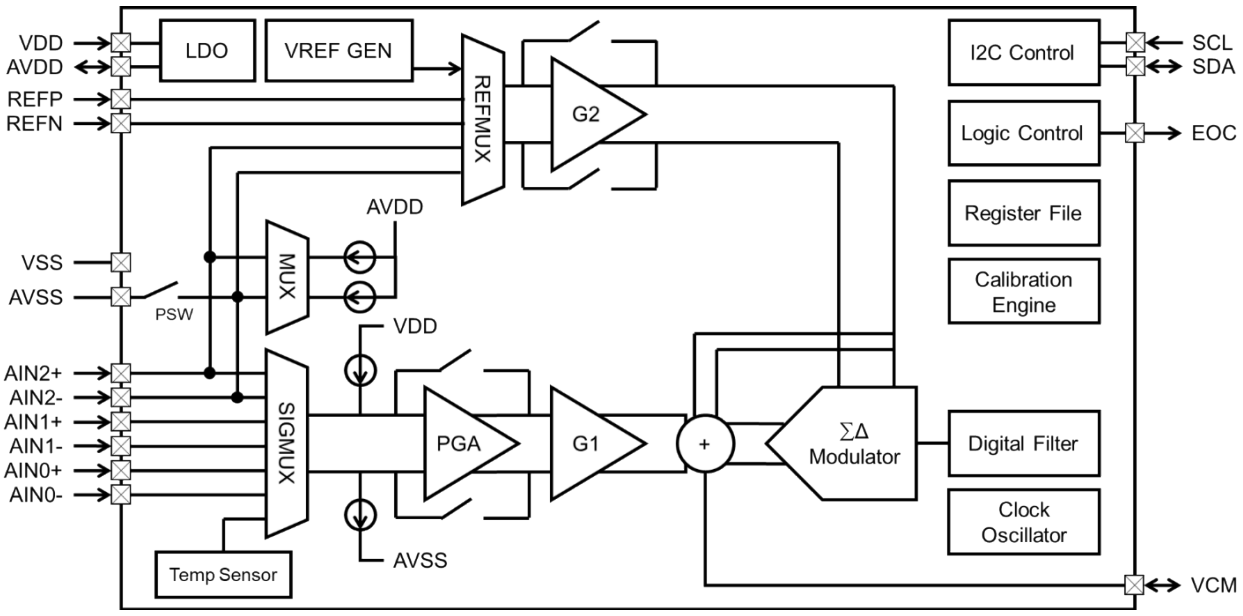


Figure 7. Function Block Diagram of AFE

➢ Power Supplies

The AFE has 2 independent power supply pins, AVDD and DVDD. AVDD powers theinternal analog linear regulator. The regulator supplies a regulated voltage to critical analogsection of the device contains programmable gain amplifier and delta-sigma data converters. AVDD is referenced to AVSS and the maximum voltage rating is 4.0V.

DVDD powers the digital section the AFE including clock generator and digital processing circuits. After the supply voltage is stable, internal power on sequence will resetall the circuits into an initial condition and register map will return to default value. The DVDD is reference to DVSS and the maximum voltage rating is 4.0V as same as AVDD.

➢ Reset

There is no external hardwire reset pin in AFE. In situations where interface synchronization is lost, user could power on/off the devices to reset the register data intodefault values and abort any operation conditions. User can re-command the register configurations after power on.

The AFE supports software reset where user could reset the device by a fixed I2Cdata pattern. The device responds to the two-wire general call address (0000 000) if the LSB bit is 0. The device acknowledges the general call address and responds to commands in the 2^{nd} byte. If the 2^{nd} byte is 0000 0110, the AFE resets the internalregisters to the power-up reset values.

➢ Power Supply Monitors

Regard to monitor the supply voltage quality, the AFE build-in supply voltage detection function. The AVDD voltage will be attenuated internally by one-fourth and appliesto data converter. The function is useful because of voltage variation from power supply could be monitored.

After initial power up sequence, the supply voltage will ramp up and stable in a short periodof time, the internal power on reset will reset the digital register file into default value.

➢ Digital Communication Interface and Data Ready Indicator

The AFE has a 2-wire serial interface that is compatible with standard I2C specification. It is operated as a slave device where a controller or master device could access the register data through I2C specified timing patterns. Connections to the bus are made through the open-drain I/O line SDA and SCL input pin. External pull-up resistor is needed for each of the two terminals. There are Schmitt triggers at SDA/SCL input signal chain to minimize the effects of signal fluctuations from harsh environment which couples noisy signals on data bus. The AFE supports the I2C transmission protocol up to 1MHz clock frequency of fast mode.

➢ Bus Fault Timeout

The AFE supports SMBus timeout feature. If the host holds the SCL pin in “L” morethan 16ms(typ.) between a START and STOP condition, the AFE would reset its internal state machine to prevent a system bus hang-up. This feature is turned on by default and release SDA and waits for a START condition.

➢ I2C Digital Communication Timing Diagrams

SYMBOL	CONDITION	MIN	MAX	UNIT
f_{SCL}	SCL operating frequency	2.5	–	us
f_{BUF}	Bus free time between STOP and START	1.3	–	us
t_{HDSTA}	Hold time after repeated START condition.	600	–	ns
t_{SUSTA}	Repeated START condition setup time	600	–	ns
t_{SUSTO}	STOP condition setup time	600	–	ns
t_{HDDAT}	Data hold time (*2)	0	–	ns
t_{HSUDAT}	Data setup time	100	–	ns
t_{LOW}	SCL clock low period	1300	–	ns
t_{HIGH}	SCL clock high period	600	–	ns
t_{VDAT}	Data valid time (*3)	–	900	ns
t_{FDA}	Data fall time	–	300	ns
t_R	Clock rise time	–	300	ns
t_F	Clock fall time	–	300	ns
Time out	Clock fall time	100	–	ms
$t_{RCClock/data}$	rise time for SCL=100KHz	–	1	us

(*1) The host and device have the same VDD voltage. The voltages are based on statisctical analysis of samplestested during initial release.

(*2) The maximum t_{HDDAT} can be 0.9us for fast mode, and is less than the maximum t_{VDAT} by a transition time.

(*3) t_{VDAT}=time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worst). =time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

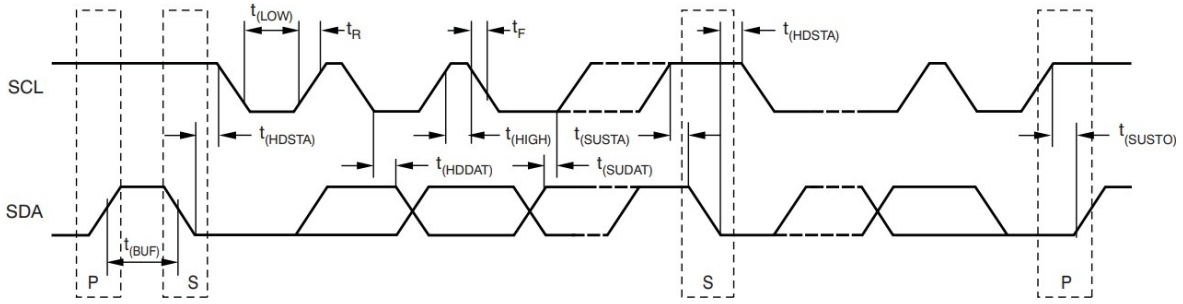


Figure 8. I2C Timing

➢ Slave Address

To communicate with the AFE, the master device must first address devices through a 7-bit device address, a direction bit indicating the intent of executing a read or write operation.

Timing Diagram

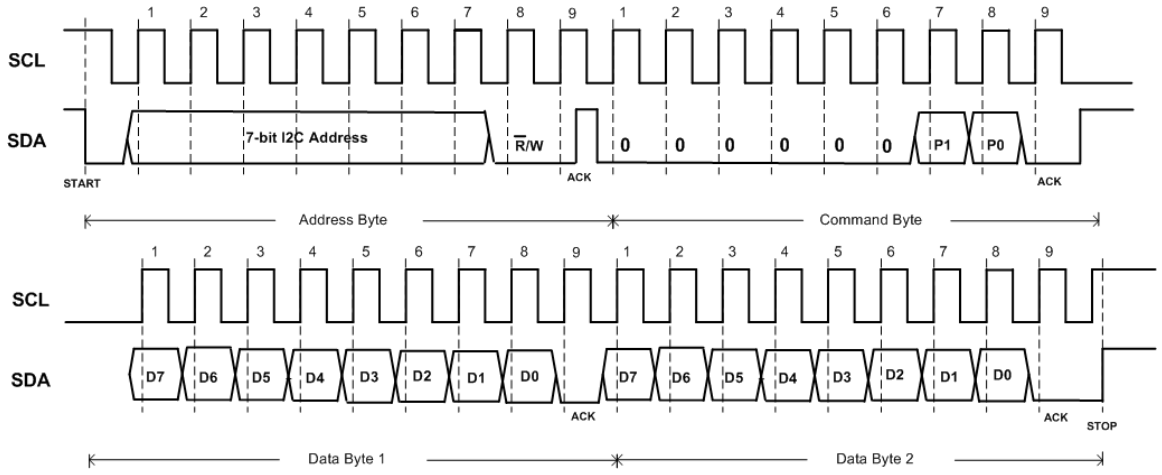


Figure 9. Two-wire timing diagram for Write Two Bytes format

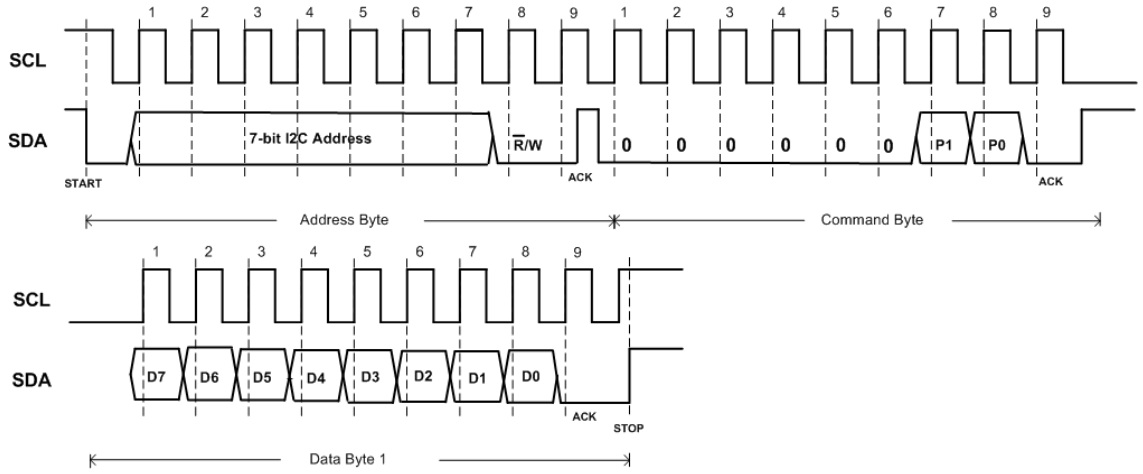


Figure 10. Two-wire timing diagram for Write Single Byte format

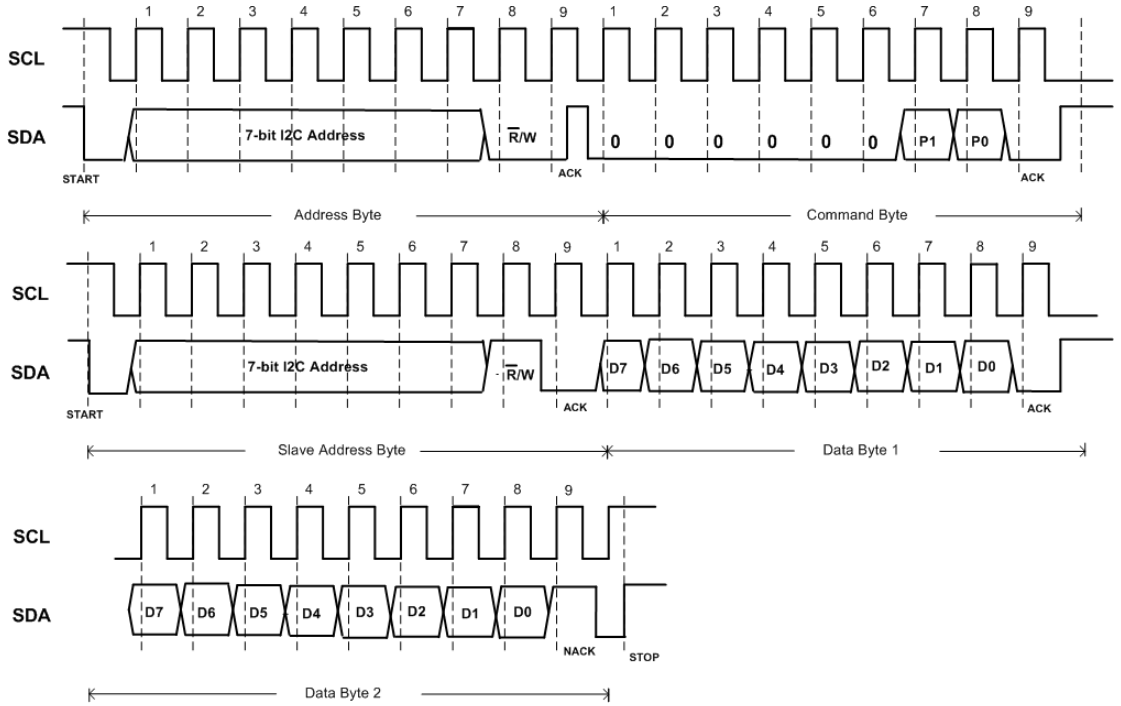


Figure 11. Two-wire timing diagram for Read Two Bytes format

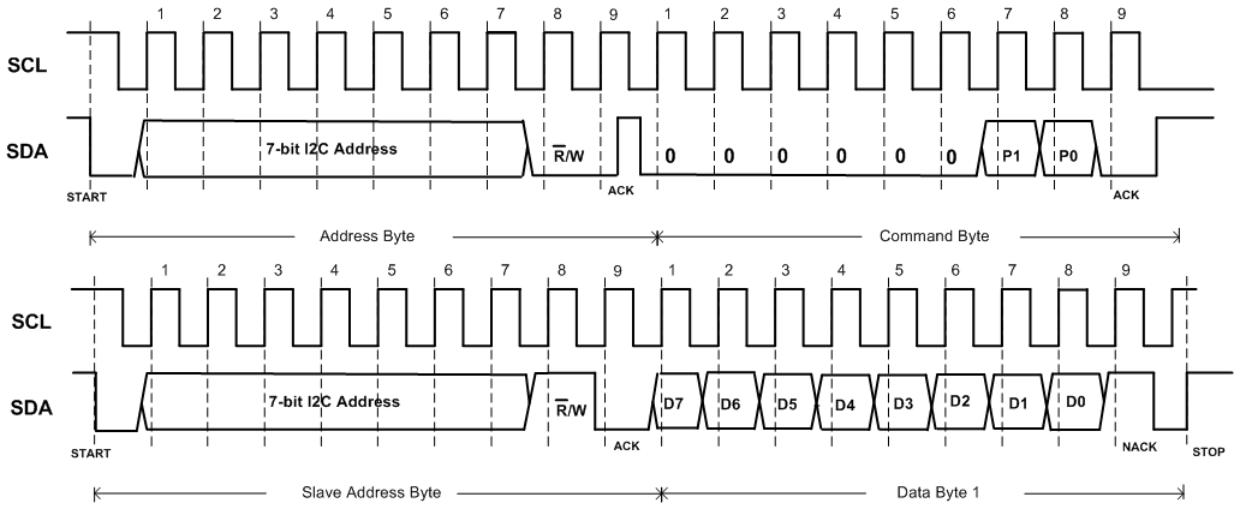


Figure 12. Two-wire timing diagram for Read Single Byte format

➢ Register File

The AFE build-in register files which can be configured to control the functions of analog front end. After powering up, the internal power on reset circuit will clear the registerdata into default value.

➢ Channel Multiplexer Configuration

AFE is 3 channels multiplexed data acquisition system utilized in industrial process control, portable medical devices, and automated test equipment need increased channel density where the user can measure the signals from multipole sensors, monitor and scan many input channels into a single sigma-delta ADC. The input multiplexer selects the signalfor measurement which could save PCB space, power and total system cost. The sigma-delta data converter is conventionally monotonic and uses integrated modulator for oversampling and digital decimation filtering that requires a internal clock source to synchronize all the functionality circuit blocks, resulting in a nonzero cycle latency. The multiplexer input faces limited bandwidth, settling time and input range which will degradethe system performance requiring to be designed carefully.

Since sigma-delta data converter is an oversampling analog input, the transition band ofanti-aliasing filter could be greatly simplified rather than brick-wall stop band filter in Nyquist-rate data converters. In most applications, aa simple single-pole RC filter is required for easy implementation.

The AFE has 3 differential analog input channels. The analog input signals are connected to internal programmable gain amplifier when the devices are operated in buffered mode. The unbuffered mode could be configured by register, the input channels connect to 2^{nd} gain stage and feed through the sigma-delta modulator directly. By unknownor higher source impedance, the input channel should set to using buffer mode where the input signals acquires by a high impedance input stage. Therefore, the AFE can tolerate any signal source impedances which connect to external resistive-type sensors directly. User could enable buffered mode to set the INBUF=1. It should be noted that the input common mode range of buffer mode between AVSS+100mV to AVDD-1V.

When INBUF=0, the devices operate in unbuffered mode. User can configure the ADCGN to setup the 2^{nd} gain stage to amplify the input signals without buffer. If the input source impedance is low enough compared to input impedance of sigma-delta modulator, it will notresult in much gain error on data converter output.

The AFE can be configured with gain equals to 1, 2, 4, 8 or 16 when it is operated inunbuffered mode. The absolute input voltage in unbuffered mode is restricted between AVSS-30mV to AVDD+30mV.Because no buffer circuits enabled during unbuffered mode, the power consumption could be minimized in data conversion.

➢ Instrumentation Amplifier

There is a programmable gain amplifier in front of sigma-delta modulator which could be used as an input analog buffer. User could configure the INBUF bit in register to enable thePGA amplifier. If the INBUF=1, the amplifier will active, and the amplifier will dis-active when INBUF=0. The PGA amplifier will be active automatically as the gain setting greater than 1. If the gain setting is equal to 1, user could configure to enable the buffer or not to adapt the input source connections. Although its wide input dynamic range of PGA and analog-to-digital converter, it is necessary to ensure that the headroom required for correctoperation is met with gain configuration.

When the PGA amplifier is enabled, the input channel multiplexer will apply to input of theinstrumentation amplifier. The low-noise programmable gain amplifier can amplify small amplitude signals to be gained while still maintaining excellent noise performance. The input gain in buffered mode could be set by 1, 2, 4, 8, 16, 32, 64 and up to 128 in the configuration register. For example, with an internal 1.2V reference voltage, the unipolar input range is from 1.2V and the bipolar range is from ±1.2V.

If the AFE is operated with external reference that has a value equal to AVDD, the analog input signal must be limited to 90% of VREF/PGAGN[2:0] when the programmablegain amplifier is enabled.

➢ ADC Configuration

The AFE are low noise, low power analog-to-digital data converter that incorporate asigma-delta modulator, programmable instrumentation amplifier, and on-chip digital decimation filter intended for the measurement of low-frequency signals such as those in RTD, thermocouple, thermopile, pressure transducer and scales.

AFE allocates 3 input channels that can be buffered or unbuffered. User could adapt to different application from input source impedance to configure the buffer on/off. The input buffer incorporates with programmable gain stage to amplify low-level sensor input signals. In addition to the input gain stage configuration, the reference volage of sigma-delta data converter could be configured also. If the full-scale of input signal after PGA amplifier stage is far below the default reference voltage, user could setup the gain of reference by x1, x3/4, x1/2 and x1/4 referred to analog input voltage.

There is programmable input DC offset voltage setup if the analog input voltage is not equally equipped in full-scale input dynamic range. Designer could configure the DCSET[2:0] which could adjust the input DC level by 1/12VREF to 7/12VREF from analoginput voltage.

Upon the input offset voltage from sensors, the input of the sigma-delta modulator has a system chopper switch to remove the system offset effect. User could average output datafrom toggling input chopper switch to have an offset-free output.

The output data rate of the AFE is user programmable. The allowable update ratesalong with different settling times could be configured by oversampling ratio register.
Normal mode signal bandwidth noise rejection is the major function of the digital filter. If user would like to immune 50Hz/60Hz power buzz, it could be implemented by placing thefrequency response of the digital filter with output notches at 50Hz or 60Hz.

➢ Calibration

The AFE will go through factory calibrated flow during manufacturing and circuit testing, user could implement the measurements without user calibration. If some the measurement system suffers from higher input impedance mismatch or system offset fromtemperature drift or environment changing, the AFE reserves a user-calibrated registers to remove systematic dc errors. It means that the devices have internal zero-scalecalibration, internal gain error calibration, system zero-scale calibration and system gain error calibration, which effectively reduce the offset error and gain error to the optimized measurement performance.

During an internal offset error and gain error calibration, the input multiplexer and are connected internally to the ADC input pins. However, a system calibration should apply theinput voltages on the analog input pins before systematic calibration is initiated.

A calibration should be treated as a data converter operation. After each data conversion,the output data of

digital filtering is scaled using the ADC calibration registers before beingwritten to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient. The EOC pin determine the end of calibration via a polling sequence or an interrupt-driven routine.

➢ IDAC Excitation Current Sources for Sensor Stimulation

The devices build in dual matched excitation current output, it expresses as the current DAC output (IDAC) in datasheet. The IDAC constant current sources that can be programmed to equal 10uA, 50uA and up to 1.5mA with 7 steps by register setting. Both excited source currents from the AVDD are directed topins which are combo-function pin configuration with analog input (AIN2+ and AIN2-) and reference voltage input pins (RIN1+and RIN1-). The IDAC current sources can be used to stimulate external resistive bridge, thermisor or RTD sensors.

➢ Reference Signal Configuration

The AFE has embedded a 1.2V reference supply. The reference voltage of sigma-delta modulator can be applied from internal bandgap reference or external reference input. For external references, the sigma-delta modulator has a fully differential input capability for the channel. The RIN0 is a dedicated differential external reference inputchannel and another reference input channel, RIN1, is a combo function with analog input channel AIN2. The reference sources of the AFE can be configured by internal register. User can select any external voltage reference source by configuring the referenceinput buffer to get the optimizing performance. When the internal reference voltage is selected, it is preferred to connect the external reference pins to analog ground to protect from noise coupling on multiplexer.

The reference inputs can be configured in buffered or unbuffered by VRBUF bit in register.When VRBUF=0, the reference input voltage will bypass the internal buffer and connect to switched-capacitor circuits in data modulator. If VRBUF=1, the reference input will buffer byinternal amplifier to immune the gain error result from the excessive RC source impedancemismatch. The common-mode range for the differential inputs is from AVSS to AVDD-1V.

In application where the excitation current for the external sensor on the analog inputs alsodrive the reference voltage by ratio-metric. The steering current error will be cancelled by such connection architecture.

Using external reference resistor of reference voltage generation, it is important to considerusing a lower temperature coefficient external resistor with higher accuracy and a better temperature drift performance.

➢ Clock Oscillator

The internal oscillator runs at 1MHz which provides the master clock source of digital circuitand ADC. The AD6110A default clock source is specified with n factory-trimmed accuracy for ±3%.

There are options for the internal oscillator to divide into different clock sources through clock generator. The output frequency of configurable clock generator could dynamicallyprogram the digital operation clock and ADC data rate.

➢ Sensor Fault Detection

For the harsh application environment where safety will be a high priority consideration,internal diagnostics are becoming part of the industry requirements. The embedded self-diagnostics in the AFE reduce the need for external components to implementdiagnostics, resulting in an easy and BOM saving solution.

To help detect a possible sensor malfunction, the device provides internal burnout current sources. The AFE contains dual internal current sources output to diagnose the sensor connection status. There are 2 weak output burn-out detection currents, one analogI/O pin sources current from AVDD to AIN2+/AIN2- and another analog I/O pin sinks currentfrom AIN2-/AIN2+ to AVSS. The dual currents are switched to the selected analog pin by register configuration independently. The burn-out bit will setup when the detection level over the limiting register setup by user in power-up. The source/sink detection currents willstimulate the external

sensor devices where the generated output voltage could be monitored by data converter. It could verify that an external sensor is still operational beforeattempting to take measurements on the channel.

After the burnout detection currents are enabled, the voltage level of analog I/O pins could ensure that it is within the specified operating range. If the detected voltage level is outside the normal operation range, it could be discriminated the sensor is disconnected or
burn-out by abnormal operation. A near full-scale reading from sourcing burnout current means the front-end sensor is overloaded or disconnected. On the other side, a near 0V voltage reading from sourcing or sinking burnout currents mean the front-end sensor is disconnected or external sensor short circuiting. The source/sink burnout currents could beused as the system diagnostic, we recommended disabling the current sources during normal operation of data conversion.

The diagnostics lead to a more robust solution for system safety consideration by data converter operation. Keep in mind that ADC readings of the functional sensor may be corrupted when the burnout current sources are enabled. Disable the burn out current sources when performing the precision measurement, and only enable the current sourceswhile sensor fault condition testing.

➢ Linear Regulators

There is a build-in on-chip linear regulator for analog section to enhance the capability of supply voltage noise rejection. The regulator could be enabled by register configuration before data converter active. There are external decoupling capacitors on AVDD pin to filterhigh-frequency noise. In power saving mode, designer could turn off the LDO to reduce power consumption. During LDO disabled, off-chip microcontroller could access the register data from I2C digital interface.

➢ Digital Filters

The sigma-delta modulator will oversample the input analog signal and shape most of thenoise power outside the signal bandwidth. An on-chip digital filter after data modulator willfilter out the high frequency noise power to minimize the output noise level in interested bandwidth.

To ensure the output data will be effective, the digital filter of AFE will be reset withoutaffecting any of the setup conditions on the device. After reset, the digital filter will start a new data conversion and decimation without user configuration. The clock of digital filter will be synchronized with modulator data output. After the decimation filter, there will be a data ready indicator output, EOC pin. The EOC pin is an open-drain output with an externalpull-up resistor which could be an interrupt signal for microprocessor to access the data converter output data. The /EOC pin indicates when the conversion is complete. The settling time and output data rate could be configured by registers.

➢ PDM data input

The devices could input a PDM data from off-chip oversampling sigma-delta modulator, user could enable AFE internal decimation filter connecting with the external modulator output data and clocks pins into AIN2+ and AIN2- by digital input configuration. The modulator digital data will feed into digital decimation with programmable oversamplingratio to setup the optimized output data rate of specific application. The output data of digital filter will store in the dedicate register location. Using external controller by I2C interface can access the registers and read out the data converter digital data.

➢ Local Temperature Sensor

The AFE offers an internal precision temperature sensor. The temperature sensor iscomprised of multi-internal diodes. The difference in current density of diodes yields a voltage which is proportional to absolute temperature(PTAT). The temperature sensor measurement could be initiated by the analog input signal multiplexers, VINHMUX[2:0] andVINLMUX[2:0] switch to 011.

Temperature readings follow the same process as the analog inputs, but only relevant MSB14 bits are used to indicate the temperature measurement result. 1LSB stands for 0.0625℃in temperature where the MSB is the sign-bit to represent the positive or negative temperature. The DATA[15:4] is the output data of temperature measurement. DATA[15] stands for the sign-bit of temperature, 0 represents the junction temperature above 0℃ and 1 represents below 0℃. It is recommended that the PGA gain setup to x1 and disable burn-out current output when measuring the temperature sensor.

➢ On-Chip Sensor Switch

A low-side PSW switch connect between AIN2- pin and AVSS. It is a sensor power on/off toenable sensor current path.

When the sensor stimulus path is active, either in current steering or voltage regulation mode, there is an on-chip switch need to be turned on. As the on-chip sensor switch is enabled, the current loop will be closed where the sensor components will output electricalsignals. The higher excitation current for sensor sourcing, the larger output voltage level willbe generated. Since most of the sensor is resistive, to ensure lower power consumption and self-heating effect, the lower excitation current is desired. On the other side, lower excitation current results in lower electrical signal output from sensor devices.

However, to minimize self-heating, the excitation current needs to be turned off betweenmeasurements. The designer could turn on the on-chip sensor switch during measurements and turn off it without data conversion to save power consumption.

The timing is a design factor for the time frame of on-chip sensor switch on/off. It depends on system specification by different sensor application. Designer needs to determine the timing configuration to optimize the system performance. Design should balance the selection of stimulation current, signal gain, reference gain and external components to ensure that the analog input voltage is being optimized along with tuning the ADC speed togive better resolution and system performance, and results in lower noise and lower offset errors.

➢ Operation ModeOverview

The AFE is a low-noise, low-power and multi-function configurable sigma-delta dataconverter which incorporates buffers, reference voltages, programmable gain stages, internal digital filtering, sensor diagnostics and on-chip temperature sensor. The devices are intended to applicable into wide dynamic range, low-frequency input signals, scales, pressure and temperature measurements.

- Continuous conversion mode

In normal power-up sequence, continuous conversion mode is in default. AFE continuously convert with EOC going low each time a conversion is completed. To read aconversion, the designer initiate a write command by I2C interface. The EOC will toggle once when another conversion is completed again. The upcoming conversion data will overwrite the previous one if no external data access is initiated.

- One-shot conversion mode

In one-shot conversion mode, the AFE are placed in standby mode between conversions. When a one-shot mode conversion is initiated, the device will enable analog section, perform a single conversion, then return back to standby mode. The most important is the internal oscillator needs a few ms time to startup and stabilization. After a one-shot conversion is completed, the EOC will active-low to interrupt external controller toaccess conversion data. The register data can be read several times if EOC keeps in low without cleared. Please do not read the register data when EOC in high state.

- Standby mode

In standby mode, most of the analog circuit is disabled with the linear regulator is active only. It consumes lower current consumption in standby mode but quickly response to the next data conversion. It could settle the analog signal into a stable stage in a short period oftime to initiate a updated data acquisition.

- Power-down mode

The AFE will stay into power-down mode by set the PWDN bit in register. It will disable all the enable signals of analog section. The maximum 1uA current will reduce thepower consumption of the devices and last a longer usage life by battery operation.

➢ ADC Digital Data Output

The oversampling sigma-delta modulator could be configured into unipolar or bipolar input,the digital data output is a binary with 2'complement format. The differential input voltage with 0V will output 0x000000, and a full-scale input voltage results in a code of 0xFFFFF.

➢ Multiplexer Connection Network

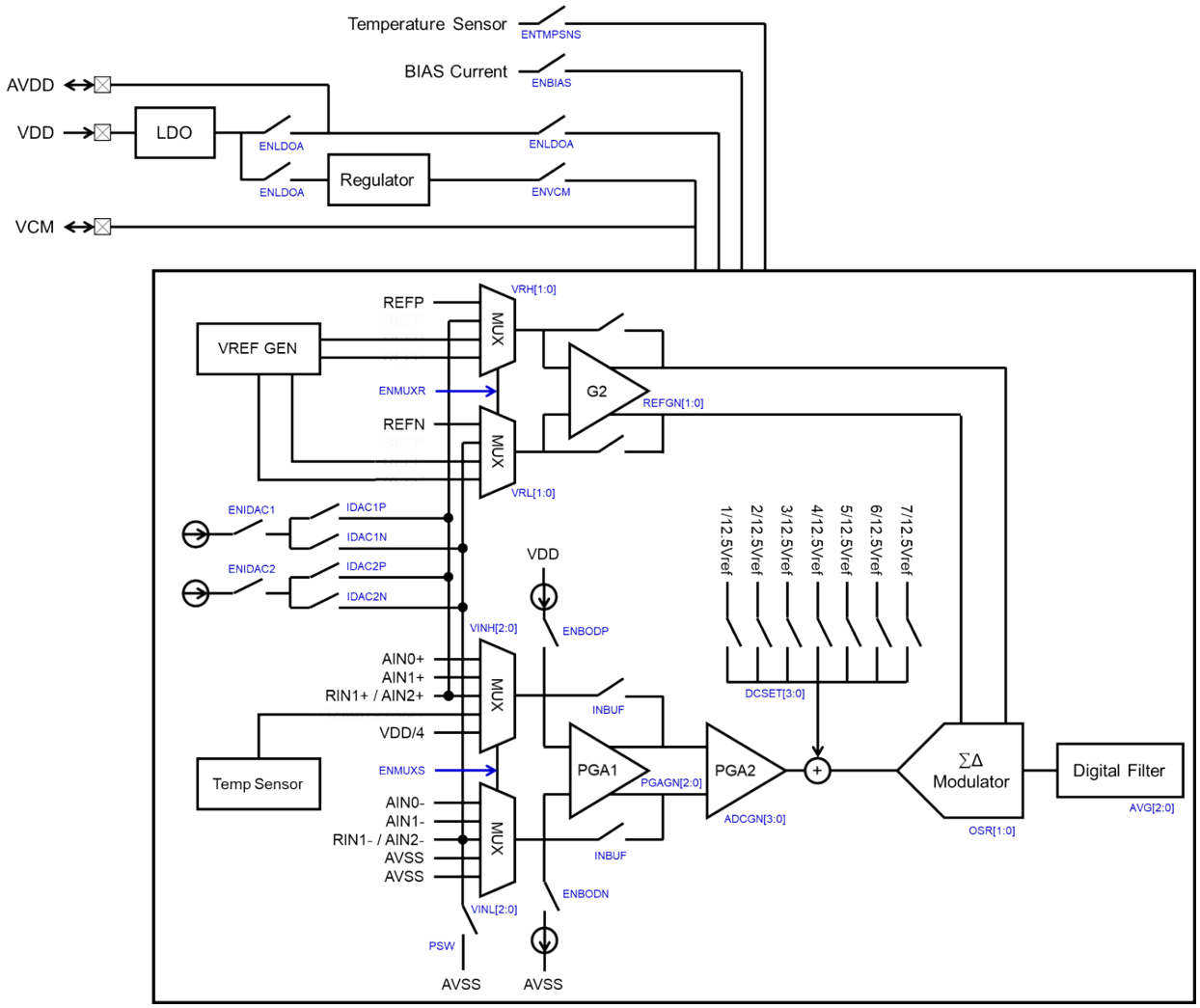
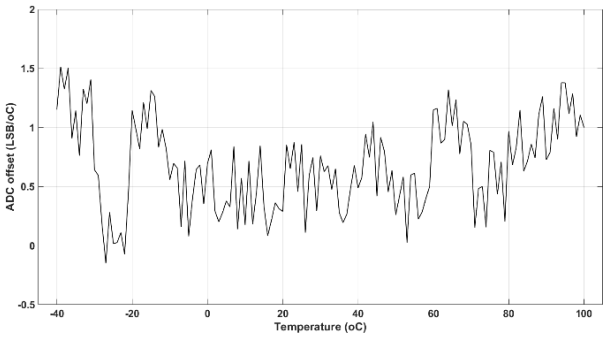
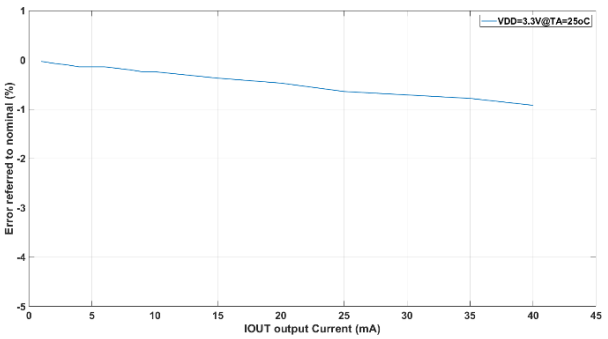


Figure 13. Multiplexer diagram of AFE

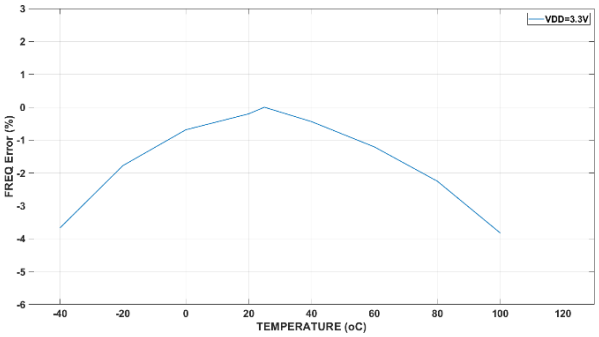
➢ Performance Characteristics



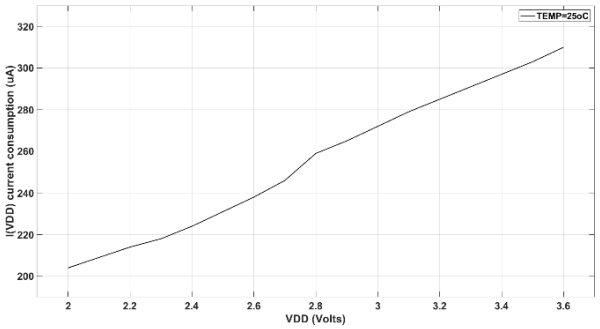
ADC offset vs. Temperature



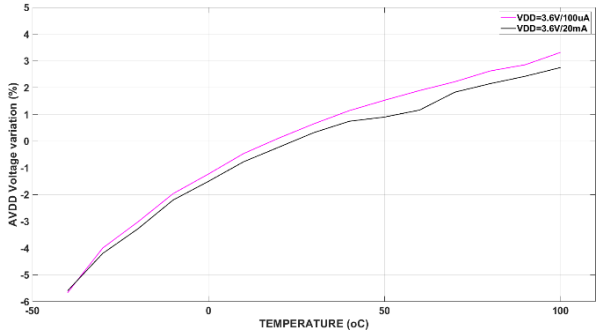
AVDD variation vs. Load current



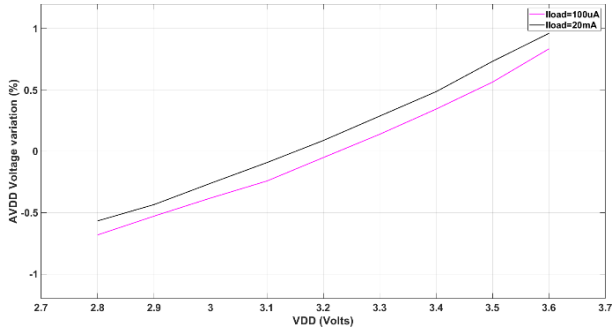
RC oscillator frequency vs. Temperature



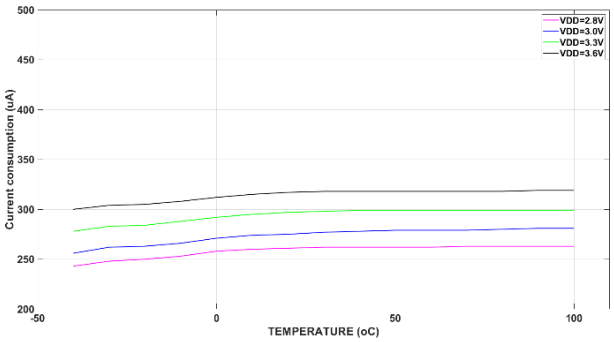
Current consumption vs. Supply voltage



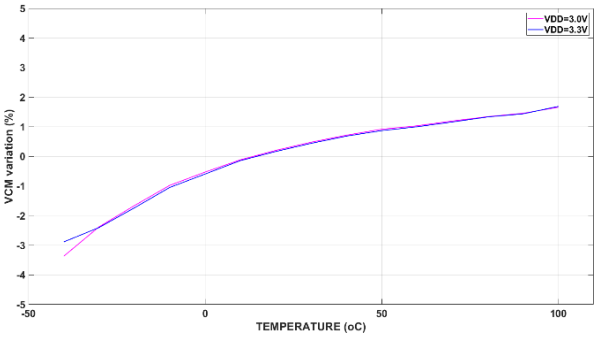
AVDD variation vs. Temperature



AVDD variation vs. Supply voltage



Current consumption vs. Temperature



VCM variation vs. Temperature

➢ Noise and Resolution

There are 2 kinds of noise terminologies where one is rms noise, another is peak-to-peaknoise. The rms noise could derive into effective number of bits (ENOB) and peak-to-peaknoise express into noise-free resolution for various output data rates. Of configuring the gain and oversampling ratio settings, designer could tradeoff the output data rate and resolution. The AFE is a differential, bipolar analog input sigma-delta converter with24 bits 2's complement digital output. The most-significant bit of digital output data standsfor sign-bit to indicate the analog input signal polarity.

It is important to note that the effective number of bits is calculated using the rms noise,where the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak noise is measured by histogram which represents the resolution for whichthere is no flicker code output.

The data shown in the effective resolution table represent typical ADC performance at roomtemperature. The noise-free bits are the peak-to-peak output of the ADC data, the effectivenumber of bits (ENOB) are the standard deviation computation of the ADC data. The outputdata are acquired with input shorted, based on consecutive ADC readings for a period of 1024 data points. Because of the statistical nature of noise, repeated noise measurementsmay yield higher or lower noise performance results.

There are 2 measurement methodologies in the following tables. One measurement byusing internal bandgap reference voltage, another measurement by external ratiometricreference voltage input. Because of the noise variation cancellation by ratiometric measurement, the effective resolution will raise up to 1-bit more than internal reference.

ADC data measurement by PGA enabled, Noise-Free resolution (effective resolution) at T_A =25℃ and internal 1.2V Reference

	OSR							
PGAGN	512	1024	2048	4096	8192	16384	32768	65536
x1	13.8(16.6)	14.27(17.1)	14.86(17.57)	15.49(18.04)	16.15(18.52)	16.63(18.97)	17.25(19.51)	18.22(20.17)
x2	13.51(16.19)	13.92(16.69)	14.47(17.18)	15.1(17.67)	15.64(18.22)	16.57(18.82)	17.05(19.35)	17.79(20.11)
x4	13.77(16.45)	14.39(16.97)	14.71(17.47)	15.21(17.95)	15.46(18.36)	16.17(18.78)	16.65(19.23)	17.48(19.65)
x8	13.74(16.59)	14.37(17.07)	14.84(17.55)	15.32(18)	15.92(18.51)	16.43(19.04)	16.99(19.5)	17.48(19.8)
x16	13.56(16.34)	14.2(16.82)	14.69(17.28)	15.33(17.76)	15.75(18.24)	16.25(18.62)	16.8(19.12)	17.56(19.78)
x32	12.82(15.63)	13.42(16.14)	13.87(16.66)	14.58(17.15)	15.11(17.56)	15.66(17.95)	16.09(18.38)	16.53(18.84)
x64	12.18(15.01)	12.59(15.49)	13.46(15.99)	13.85(16.45)	14.53(16.91)	14.92(17.37)	15.57(17.7)	15.88(17.93)
x128	11.51(14.2)	12.21(14.7)	12.54(15.21)	13.02(15.72)	13.71(16.26)	14.23(16.8)	14.98(17.21)	15.81(17.8)

ADC data measurement by PGA enabled, Noise-Free resolution (effective resolution) at T_A =25℃ and external ratiometric measurement

	OSR							
PGAGN	512	1024	2048	4096	8192	16384	32768	65536
x1	14.39(17.27)	15.21(17.77)	15.85(18.27)	16.29(18.74)	16.69(19.26)	17.3(19.76)	18(20.41)	18.79(21.12)
x2	14.33(17.18)	14.95(17.67)	15.5(18.18)	16.19(18.73)	16.77(19.27)	17.42(19.84)	18.17(20.44)	18.87(21.13)
x4	14.04(17.01)	14.64(17.49)	15.31(18.02)	15.88(18.55)	16.71(19.12)	17.26(19.68)	17.85(20.23)	18.45(20.78)
x8	14.17(16.84)	14.62(17.32)	15.34(17.83)	15.81(18.38)	16.4(18.91)	16.99(19.37)	17.62(19.73)	17.89(20.11)
x16	13.2(15.9)	13.52(16.39)	14.09(16.87)	14.9(17.39)	15.54(17.98)	16.23(18.7)	16.92(19.51)	17.48(20.01)
x32	13.73(16.47)	14.24(16.94)	14.78(17.42)	15.36(17.91)	16.03(18.46)	16.57(19)	17.13(19.36)	17.66(19.83)
x64	12.56(15.2)	12.9(15.65)	13.5(16.14)	14.11(16.64)	14.76(17.15)	15.2(17.75)	15.87(18.33)	16.64(18.93)
x128	11.76(14.36)	12.21(14.85)	12.67(15.37)	13.27(15.87)	13.84(16.31)	14.41(16.8)	14.86(17.17)	15.48(17.7)

ADC data measurement by PGA disabled, Noise-Free resolution (effective resolution) at T_A =25℃ and internal 1.2V Reference

	OSR							
ADCGN	512	1024	2048	4096	8192	16384	32768	65536
x1	14(16.65)	14.31(17.14)	14.93(17.66)	15.62(18.2)	16.24(18.76)	16.84(19.34)	17.49(19.94)	18.33(20.51)
x2	13.82(16.67)	14.32(17.18)	14.98(17.68)	15.45(18.11)	16.09(18.56)	16.66(19.06)	17.15(19.54)	18.02(20.21)
x4	13.82(16.67)	14.32(17.18)	14.98(17.68)	15.45(18.11)	16.09(18.56)	16.66(19.06)	17.15(19.54)	18.02(20.21)
x8	13.58(16.39)	14.04(16.89)	14.77(17.4)	15.1(17.89)	15.82(18.37)	16.6(18.87)	17.14(19.35)	17.77(20)
x16	13.8(16.52)	14.49(17.04)	14.9(17.57)	15.38(18.09)	15.93(18.54)	16.6(18.93)	16.99(19.25)	17.56(19.46)

ADC data measurement by PGA disabled, Noise-Free resolution (effective resolution) at T_A =25℃ and external ratiometric measurement

	OSR							
ADCGN	512	1024	2048	4096	8192	16384	32768	65536
x1	14.6(17.3)	15.06(17.82)	15.59(18.35)	16.25(18.88)	16.88(19.41)	17.31(19.97)	18.07(20.56)	18.71(21.16)
x2	14.73(17.32)	15.09(17.82)	15.54(18.33)	16.26(18.9)	16.89(19.41)	17.29(19.87)	17.91(20.37)	18.45(20.75)
x4	14.39(17.18)	15.03(17.68)	15.66(18.23)	16.12(18.82)	16.86(19.42)	17.4(19.9)	18.25(20.41)	18.51(20.69)
x8	14.19(17.08)	14.86(17.6)	15.45(18.12)	16.03(18.64)	16.63(19.14)	17.23(19.66)	17.91(20.21)	18.45(20.58)
x16	13.99(16.73)	14.51(17.25)	14.83(17.73)	15.46(18.27)	16.14(18.81)	16.78(19.36)	17.48(19.97)	18.17(20.61)

➢ Register Description

- Raw Data Register

Without post-calibration, the output data of sigma-delta converter will have gain error and offset error from system offset and impedance mismatch. During wafer and packaged testing, AFE will manufacture in factory calibrated flow to remove the DC errors. TheRWADATA are testing only registers and it is useless for users.

Register	Address	R/W	Description	Default
DATA_RL	0x00	R	Low-byte of 24-bit sigma-delta converter raw data	0x00
DATA_RM	0x01	R	Medium-byte of 24-bit sigma-delta converter raw data	0x00
DATA_RH	0x02	R	High-byte of 24-bit sigma-delta raw data	0x00

Bits	Bit Name	Description
[7:0]	DATA_R	Low-byte of ADC raw data
[15:8]		Medium-byte of ADC raw data
[23:16]		High-byte of ADCraw data

- ADC Data Register

It is a ADC data output after gain error and offset error cancellation. User could read the 3bytes ADC data registers from ADCDATA[23:0].

Register	Address	R/W	Description	Default
DATA_L	0x03	R	Low-byte of 24-bit sigma-delta converter data	0x00
DATA_M	0x04	R	Medium-byte of 24-bit sigma-delta converter data	0x00
DATA_H	0x05	R	High-byte of 24-bit sigma-delta data	0x00

Bits	Bit Name	Description
[7:0]	DATA	Low-byte of ADC data
[15:8]		Medium-byte of ADC data
[23:16]		High-byte of ADC data

- **Oversampling Ratio Register**

It is a ADC data output after gain error and offset error cancellation. User could read the 3bytes ADC data registers from ADCDATA[23:0].

Register	Offset	RW	Description	Default
OSR	0x18	R/W	OSR Register	0x00

Bits	Bit Name	Description
[7:4]	Reserved	—
[3:2]	OSR	**Oversampling ratio of data converter** 00：OSR = 512 01：OSR = 256 10：OSR= 128 11：OSR= 1024
[1:0]	AVG	—

- **ENCFG Register**

It is an analog front end fundamental block configuration. The register controls the sensordiagnostic excitation signals, voltage bias, current bias and LDO enabled.

Register	Address	R/W	Description	Default
ENCFG	0x19	R/W	Analog front-end configuration register	0x00

Bits	Bit Name	Description
[7:6]	Reserved	–
[5]	ENBODN	**Constant sink excitation current control** 0：Excitation sink current disabled 1： Excitation sink current enabled
[4]	ENBODP	**Constant source excitation current control** 0：Excitation source current disabled 1： Excitation source current enabled
[3]	ENPDET	**Power supply monitoring function control** 0：Power supply monitoring disabled 1： Power supply monitoring enabled
[2]	ENVCM	**VCM function configuration** 0：Common-mode voltage generator disabled 1：Common-mode voltage generator enabled
[1]	ENLDO	**LDO circuit configuration** 0：Voltage regulator disabled 1：Voltage regulator enabled
[0]	ENBIAS	**Current bias control** 0： Current bias circuit disabled1： Current bias circuit enabled

- **Analog Input Multiplexer Register**

It is a ADC data output after gain error and offset error cancellation. User could read the 3bytes ADC data registers from ADCDATA[23:0].

Register	Offset	RW	Description	Default
SIGMUX	0x1A	R/W	Analog input multiplexer register	0x00

Bits	Bit Name	Description
[7:3]	Reserved	—
[2:1]	INCH	**Analog input multiplexer configuration** 00： Differential analog input signals go-through 01： Differential signals connect to positive terminal input 10： Differential signals connect to negative terminal input1： Differential analog input signals crossover
[0]	Reserved	—

- **Input Signal Multiplexer Register**

The 3 channels differential analog input signal could be configured individually by 4 bits inSIGCFG register. The VRL controls the negative terminal input signals and VRH controls the positive terminal input signals.

Register	Offset	RW	Description	Default
SIGCFG	0x1B	R/W	Input signal multiplexer register	0x00

Bits	Bit Name	Description
[7]	ENMUX	Multiplexer control 0：input multiplexer disabled. All the input switches are disconnected from I/O pins to internal circuits 1：Multiplexer control active
[5:3]	VRL	**Inverting terminal signal path configuration** 000：Channel 1 001：Channel 2 010：Channel 3 011： Temperature measurement100 ~ 111：Reserved
[2:0]	VRH	**Non-inverting terminal signal path configuration** 000：Channel 1 001：Channel 2 010：Channel 3 011： Temperature measurement100 ~ 111：Reserved

- **Reference Voltage Input Multiplexer Register**

It is a ADC data output after gain error and offset error cancellation. User could read the 3bytes ADC data registers from ADCDATA[23:0].

Register	Offset	RW	Description	Default
REFCFG	0x1C	R/W	Reference voltage multiplexer register	0x00

Bits	Bit Name	Description
[7:4]	Reserved	—
[3:2]	VRL[1:0]	**Inverting terminal of analog differential input** 00： Channel 0, connecting to reference I/O pins, RIN0-01： Channel 1, connecting to reference I/O pins, RIN1-10： Channel 2, connecting to analog ground, 0V 11：Channel 3, connecting to low-side of TEMP reference voltage
[1:0]	VRH[1:0]	**Noninverting terminal of analog differential input** 00： Channel 0, connecting to analog I/O pins, RIN0+ 01：Channel 1, connecting to analog I/O pins, RIN1+ 10：Channel 2, connecting to internal 1.2V reference voltage 11：Channel 3, connecting to high-side of TEMP reference voltage

- **IDAC Configuration Register**

It is an IDAC output channel configuration. The IDAC1 and IDAC2 switches individually to CH2 noninverting terminal and CH2 inverting terminal. User could allocate the IDAC outputin dedicated channel by the register.

Register	Address	R/W	Description	Default
IDACCFG	0x1D	R/W	IDAC output channel configuration register	0x00

Bits	Bit Name	Description
[7:6]	Reserved	—
[5]	PSW	**Sensor switch (Connects to inverting input of CH2)** 0：Sensor switch dis-connected 1：Sensor switch connects to VSS
[4]	Reserved	–
[3]	DAC2N	**IDAC2 switch2 control** 0：IDAC2 switch disconnects from inverting terminal of analog input 1：IDAC2 switch connects to inverting terminal of analog input
[2]	DAC1N	**IDAC1 switch2 control** 0：IDAC1 switch disconnects to inverting terminal of analog input 1：IDAC1 switch connects to inverting terminal of analog input
[1]	DAC2P	**IDAC2 switch1 control** 0：IDAC2 switch disconnects to noninverting terminal of analog input 1：IDAC2 switch connects to noninverting terminal of analog input
[0]	DAC1P	**IDAC1 switch1 control** 0：IDAC1 switch disconnects to noninverting terminal of analog input 1：IDAC1 switch connects to noninverting terminal of analog input

- **PGACFG Register**

PGACFG configures the PGA amplifier and reference voltage buffer circuits. The buffer configuration register controls the enable and disable of analog input buffer, reference inputbuffer and programmable gain amplifier.

Register	Address	R/W	Description	Default
PGACFG	0x1E	R/W	1st gain stage amplification configuration	0x00

Bits	Bit Name	Description
[7]	Reserved	—
[6]	VRBUF	**Reference voltage input buffer control** 0：Reference voltage input without buffer 1：Reference voltage input with buffer
[5]	ENPGACH	**PGA and analog input buffer chopper enable** 0：Disable 1：Enable
[4]	INBUF	**PGA and analog input buffer enable** 0：Disable 1：Enable
[3]	Reserved	—
[2:0]	PGAGN	**1st stage gain factor configuration** 000：x1 001：x2 010：x4 011：x8 100：x16 101：x32 110：x64 111：x128

- **ADC Configuration Register**

The ADC configuration register program the data converter operation scaling.

Register	Address	R/W	Description	Default
ADCCFG	0x1F	R/W	ADC configuration registoer	0x00

Bits	Bit Name	Description
[7]	ENADC	**ADC conversion enable** 0：Disable 1：Enable
[6]	ENADCCH	**ADC conversion chopper enable** 0：Disable 1：Enable
[5:4]	VRGN	**Reference input voltage gain configuration** 00：x1 01：x1/2 10：x3/4 11：x1/4
[3:0]	ADCGN	**2nd stage gain factor configuration** 0000：x1 0001：x2 0010：x3 0011：x4 0100：x5 0101：x6 0110：x7 0111：x8 1000：x9 1001：x10 1010：x11 1011：x12 1100：x13 1101：x14 1110：x15 1111：x16

- **ADC DCSET Register**

The ADC DCSET register program the analog input offset voltage and reference voltagegain of data converter.

Register	Address	R/W	Description	Default
DCSET	0x20	R/W	DC input offset register	0x00

Bits	Bit Name	Description
[7:3]	Reserved	—
[2:0]	DCSET	**PGA and analog input buffer chopper enable** 000：Normal 001：1/12xVREF input dc offset 010：2/12xVREF input dc offset 011：3/12xVREF input dc offset 100：4/12xVREF input dc offset 101：5/12xVREF input dc offset 110：6/12xVREF input dc offset 111：7/12VREF input dc offset

- **VBGCFG Register**

It is an analog input amplifier gain stage configuration. The PGAGN[2:0] sets the gain of theinstrumentation amplifier. The ADCGN[3:0] configures the 2nd gain stage amplifier.

Register	Address	R/W	Description	Default
CONF	0x21	R/W	Reference voltage and T sensor configuration register	0x00

Bits	Bit Name	Description
[7:3]	Reserved	—
[2]	ENDEM	**DEM enable control** 0：Disable 1： Enable
[1]	ENSNSCH	**Temperature sensor chopper enabled** 0：Disable 1：Enable
[0]	ENTMPSNS	**Temperature sensor enabled** 0：Disable 1：Enable

- **IDAC1 Register**

IDAC1 constant output current control register.

Register	Address	R/W	Description	Default
IDAC1	0x22	R/W	IDAC1 constant source current control register	0x00

Bits	Bit Name	Description
[7]	ENIDAC1	**IDAC1 enable control** 0：IDAC1 disabled 1：IDAC1 enabled
[6:0]	IDAC1	**IDAC1 constant output current control** 00000：0 00001：10uA 00010：25uA …. 10000：800uA …. 111111：1600uA

- **IDAC2 Register**

IDAC2 constant output current control register.

Register	Address	R/W	Description	Default
IDAC2	0x23	R/W	IDAC2 constant source current control register	0x00

Bits	Bit Name	Description
[7]	ENIDAC2	**IDAC2 enable control** 0：IDAC2 disabled 1：IDAC2 enabled
[6:0]	IDAC2	**IDAC2 constant output current control** 00000：0 00001：10uA 00010：25uA …. 10000：800uA …. 111111：1600uA

- **System Clock Register**

The SYSCLK register configures the data converter clock and system clock enabled.

Register	Address	R/W	Description	Default
SYSCLK	0x24	R/W	System clock configuration register	0x00

Bits	Bit Name	Description
[7]	Reserved	—
[6:4]	CLKDIV	**System clock to ADC clock divider** 000：ADC clock is master clock 001：divide-by-2 010：divide-by-4 011：divide-by-8 100：divide-by-16 101：divide-by-32 110：reserved 111：reserved
[3:1]	Reserved	—
0	ENHSRC	**System clock enabled** 0：disabled 1： enabled

- **INTSTAT Register**

Interruption state indication register to indicate the chip reset status.

Register	Address	R/W	Description	Default
INSTAT	0x25	R/W	Interrupt flag and EOC polarity register	0x00

Bits	Bit Name	Description
[7]	INTF	**Interrupt flag** 0：Converter is under conversion 1：DATA is ready to be read
[6]	SNSL	**Sensor signal Lo-level Interrupt** 0： Sensor signal above low-level threshold1： Sensor signal below low-level threshold
[5]	SNSH	**Sensor signal Hi-level Interrupt** 0： Sensor signal below high-level threshold1： Sensor signal above low-level threshold
[6:2]	Reserved	—

[1]	POL	**EOC polarity control** 0：EOC pin open-drain output with active 0 1：EOC pin open-drain output with active 1
[0]	INTEN	**Interrupt output enable** 0：Disable interrupt function 1：Enable interrupt function

- **Register Summary**

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
DATA_R	0x00	R	DATA_R[7:0]								0x00
	0x01	R	DATA_R[15:8]								0x00
	0x02	R	DATA_R[23:16]								0x00
DATA	0x03	R	DATA[7:0]								
	0x04	R	DATA[15:8]								
	0x05	R	DATA[23:16]								
OSR	0x18	R/W	–	–	–	OSR[1:0]		–	–	–	0x00
ENCFG	0x19	R/W	–	–	ENBODN	ENBODP	EMPDET	ENVCM	ENLDO	ENBIAS	0x00
SIGMUX	0x1A	R/W	–	–	–	–	–	INCH1	INCH0	–	0x00
SIGCFG	0x1B	R/W	ENMUX	–	VIL[2:0]			VIH[2:0]			0x00
REFCFG	0x1C	R/W	–	–	–	–	VRL[1:0]		VRH[1:0]		0x00
IDACCFG	0x1D	R/W	–	–	PSW	–	DAC2N	DAC1N	DAC2P	DAC1P	0x00
PGACFG	0x1E	R/W	–	VRBUF	ENPGACH	INBUF	–	PGAGN[2:0]			0x00
ADCCFG	0x1F	R/W	ENADC	ENADCCH	VRGN[1:0]		ADCGN[3:0]				0x00
DCSET	0X20	R/W	–	–	–	–	–	DCSET[2:0]			0x00
VBGCFG	0x21	R/W	–	–	–	–	–	ENDEM	ENSNSCH	ENVBG	0x00
IDAC1	0x22	R/W	ENIDAC1	IDAC1[6:0]							0x00
IDAC2	0x23	R/W	ENIDAC2	IDAC2[6:0]							0x00
SYSCLK	0x24	R/W	–	CLKDIV[2:0]			–	–	–	ENHSRC	0x01

➢ Layout Note and Grounding Guidelines

The AFE have 2 set of power supplies. One voltage (AVDD) supplies power to analog circuit with external filtering capacitor to immune the system noise, and another DVDD provides power to digital circuit which could protect and isolate the digital switchingnoise from interference the analog circuits and minimizing coupling between analog powerand digital power sections. Decoupling capacitors are important when AFE operatesin high resolution data conversion. The AVDD pin is referenced to AVSS pin with dual decoupling capacitor. Decouple AVDD with a 1.5uF capacitor in parallel with a 0.1uF capacitor to AVSS. The higher capacitance decoupling capacitor could use as a power supply tank and lower-order capacitor to high-frequency noise filtering. Referring to AVDDpower lines, the digital power lines DVDD pin is reference to DVSS pin as the same function and connection with AVDD and AVSS pins.The power lines are necessary to use as wide trace as possible to have lower impedance path to reduce the voltage drop and glitches on power lines.

The analog signal inputs and reference voltage input are differential and referred to common-mode voltage. There is a common-mode voltage filtering capacitor pin to filtering out the high-frequency noises. Because of differential input signals, the high common-moderejection of the AFE removes common-mode noise on the analog input signals. The analog ground plane should pave under AFE to ensure that the noisy signal will not couple into the device. Designer should avoid to routing digital signals under the device or running in parallel in sensitive signals because these traces will couple noise onto the device or analog and reference signals.

The sigma-delta modulator architectures implement oversampling and using noise shapingtechniques to move the low-frequency noise forward higher frequency band. The digital filter after modulator removes the noise from the analog and reference inputs. The notch frequency of digital filter is configurable adapting to different applications which immune to noise interference than conventional Nyquist rate data converters. Because of high resolution and low noise levels from AFE, care must be taken regarding grounding placement and layout floorplan.

The ground and power traces around AFE should be separated on PCB which is sensitive to any switching noise. With large ground planes with multi-through holes and shorter return path to reduce the ground impedance could minimize the disturbance voltage.Also, the shielding technique could protect the sensitive analog input and reference input signals from noisy environment. Digital interface clock and data signals are fast switching traces, using ground shield to prevent radiating noise to other sections of the PCB. Please be noted that never run digital signals near the analog and reference input signals.
Double-sided board with large ground plane is preferred to have the best performance.

The layout engineer must ensure that the paths for all return currents are as close aspossible to the paths the currents took to reach their destinations.

● 32-bit ARM® Cortex™-M0+ MCU

➢ Core with Embedded Flash and SRAM

The ARM ® Cortex™-M0+ is a new processor of ARM company, it provides a reliable platform for MCU to achieve high performance and low power consumption, and integrates rich IO and advanced interrupt control system.

The FE82160 embedded 64/32KB Flash memory for storing user application code and data. The core can operate up to 24Mhz, Flash does not need wait cycles.

The FE82160 embeds 4KB of SRAM memory.

➢ CRC Calculation Unit

The CRC calculation unit uses a fixed polynomial generator (according to the polynomial F(x) = X16 + X12 + X5 + 1 given in ISO/IEC13239). used to generate CRC codes for 32-bit data. In many applications technology is used to verify the integrity of data transmission and storage, it provides a means to verify storage errors in flash memory, calculate the signature of the software in real time, and compare the signatures generated during software execution.

➢ Nested Vectored Interrupt Controller (NVIC)

The FE82160 embeds a nested vectored interrupt controller (NVIC), capable of real-time control and interrupt processing.

- Up to 32 interrupt requests (IRQ)Input
- 4 interrupt priority levels
- Provide low-latency interrupt handling.
- The entry address of the interrupt vector leads directly to the core.
- Tightly coupled NVIC interface.
- Early processing of interrupts.
- Handle late-arriving higher-level interrupts.

➢ System Reset

The FE82160 has 9 reset sources, each reset source can trigger the system reset which reset most of the registers, the program counter will point to the reset address (0x0000 0000)

- power-on reset (POR) and power-down reset (PDR)
- External Reset Pin reset
- Independent watchdog reset
- Window watchdog reset
- Software reset
- Low voltage Detect(LVD)Reset
- Lockout Reset
- CPURST Reset
- MCURST Reset

➢ Clock

- 4M~24MHz external high-speed crystal oscillator (HSE)
- 32.768KHz external low-speed crystal oscillator (LSE)
- 4M~24MHz internal high-speed clock (HSI)
- 32.768KHz/38.4KHz internal low speed clock (LSI)

Internal RC Frequency deviation over full voltage and full temperature range<±2.5%.
System clock selection is performed on startup; however, the internal high-speed oscillator is selected as default CPU clock on reset.

➢ Power supply supervisors (POR/BOR/LVD)

The FE82160 integrates power-on reset (POR) and power-down reset (BOR) detection circuits, which are always on to ensure proper operation above a threshold of 2.5V. If the power supply is lower than the threshold VPOR/VBOR, the system is always in reset state, without the need for an external reset circuit. The product also integrates a programmable voltage detector (LVD) for monitoring power supply voltage. Can generate interrupt or reset according to rising/falling edge. With hardware delay circuit and configurable software antishock function.

➢ Voltage regulator (LDO)

The voltage regulator powers the internal circuitry and the VCAP capacitor is connected externally.

➢ Power mode

The FE82160 supports 3 working modes：

- Run mode: The CPU core and peripheral modules continue to operate.
- Sleep mode: In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Deep-sleep mode: The CPU core is halt, the main clock is turned off, and the low-power modules continue to operate.

In sleep mode, the core clock is turned off, and other peripherals can still operate, and the core can be woken up through an interrupt. In deep sleep mode, the main clock is turned off, and most modules stop operate. The system operates on the built-in 38.4KHz/32.768KHz low-speed clock, which can be interrupted by RTC, AWK interrupt or external interrupt to wake up the chip device. In the normal operate mode, you can choose to work in frequency division mode or turn off the clock of some unused peripherals to achieve flexible switching between power consumption and performance.

➢ Real Time Clock (RTC)

The real-time clock provides a set of continuous counting counters, which can be configured by software to provide clock calendar functions, and can also provide warning interrupts and periodic interrupts.

➢ Timers and Watchdogs

The FE82160 product includes 1 advanced timer,1 general purpose timer,1 programmable counter,2basic timer,1 low power timer,1 window watchdog,1 stand-alone watchdog and 1 systick (SysTick)Timer.

➢ Advanced Timer（TIM1）

Advanced control timer (TIM1) can be seen as a three-phase PWM generator assigned to 6 channels, It has a complementary PWM output with dead-time insertion and can also be used as a complete general-purpose timer. Four independent channels can be used for:

- Input capture
- Output comparison
- Generate PWM (edge or center aligned)
- Single-shot pulse output TIM1 the same function as TIM2 timer when configured as 16-bit general-purpose timer. It has full modulation capability (0~100%) when configured as 16-bit PWM generator

In debug mode, the timers can be frozen and the PWM outputs disabled, cutting off the power switches controlled by these outputs. Most functions of the advanced timer are the same as the general timer, and the same internal structure, so it can work together with the TIM timer through the timer link function to provide synchronization or event link.

➢ General purpose timer (TIM2)

The FE82160 has a 16-bit autoload up/down counter, a 16-bit prescaler and 4 independent channels, each channel can be used for input capture, output compare,PWM and single-pulse mode output, they canalso work with advanced control timers through the timer link function, providing Synchronization or event chaining functionality. In debug mode, the counter can be frozen and any general purpose timer can be used to generate PWM outputs.

➢ Programmable Counter Array (PCA)

PCA (Programmable Counter Array) supports up to five 16-bit capture/comparison modules. The timing/counters can be used as a general-purpose clock counting/event counters for capture/comparison functions. Each channel of the PCA can be independently programmed to provide input capture/output compare or pulse width modulation.

➢ Low Power Timer (LPTIM)

The low power timers are 16-bit selectable. After the system clock is turned off, it can still be clocked by LSI or LSE, and the system can be woken up in low power mode by interrupt.

➢ Basic timer (TIM10/11)

The basic timer consists of 2 16/32 bit selectable timers TIM10/11. TIM10/11 have exactly the same function, they are all synchronous timer, you can choose to work in heavy load mode or non-heavy load mode. TIM10/11 can count external pulses or implement system timer.

➢ Independent Watchdog (IWDG)

The independent watchdog is a 20-bit down counter. It is clocked by an internal independent LSI; since the internal LSI is independent of the main clock, it can operate in shutdown and standby modes. It can be used either as a watchdog to reset the device if the CPU runs away, or as a free-running timer to provide time-out management for the application. In debug mode, the counters can be frozen.

➢ System Watchdog (WWDG)

The system window watchdog is based on a 8-bit down-counter, supporting a 20-bit prescaler, which is driven by the APB clock (PCLK) provides the action clock. It can be used as a watchdog to reset the device in case of system problems, it has an early warning interrupt function, and the counters can be frozen in debug mode.

➢ SysTick timer (SysTick)

The systick timer is dedicated to real-time operating systems, but can also be used as a standard down counter. It has the following properties:

- 24-bit down counter
- Auto-reload function
- Generate a maskable system interrupt when the counter counts to 0
- Programmable clock source (HCLK or HCLK/4)

➢ I2C Bus

I²C bus interfaces can operate in multimaster and slave modes. They can support standard, fast and high speed modes, the maximum data transmission speed can reach 1Mbps.

➢ Universal Asynchronous Transceiver (UART1/UART2)

The FE82160 has 2 Universal Asynchronous Transceivers for asynchronous communication.

➢ Low Power Universal Asynchronous Transceiver (LPUART)

The FE82160 has 1 Universal Asynchronous Transceiver that can work in low power mode, providing asynchronous communication.

➢ Serial Peripheral Interface (SPI)

The SPI is capable of communicating at rates up to 12Mb/s in full-duplex and simplex communication modes, master and slave modes.

➢ General purpose input and output (GPIO)

Each GPIO can be software configured as a push-pull or open-drain output, as an input with or without pull-up/pull-down, or as an alternate peripheral function. Each port is controlled by an independent control register bit. Supports edge-triggered interrupts and level-triggered interrupts, can wake up MCU from various low power consumption modes to work mode, support Schmitt trigger input filtering function. The output drive capability is configurable, and the maximum drive current is 12mA. Generic IO supports external asynchronous interrupts.

➢ Analog to Digital Converter (ADC)

The sampling rate of a 12-bit sequential approximation ADC can reach 1Msps when operating under a 16MHz ADC clock. Power supply can be selected as reference voltage. The 20 Pin package contains 7 external channels, and the 32 Pin package contains 16 external channels. Can achieve single, scan, cycle conversion. Automatically converts on a selected set of analog inputs in scan/loop mode.

- Input voltage range:0 to VCC
- Conversion cycles:16/20 clock cycles
- Support trigger ADC from external terminals, internal TIM1,TIM2,TIM10/11, voltage comparator, etc
- End of Conversion (EOC)Interrupt

➢ Voltage Comparator (VCMP)

Total 3 configurable positive/negative external input channels;1 internal bandgap reference voltage (FE82160F8 = 2.5V, FE82160K8 = 1.57V). VCMP output available for timers TIM1, TIM10/11, LPTIM and PCA Capture, Gating, External Count usage. Asynchronous interrupt can be generated according to rising/falling edge, wake up MCU from low power mode.

➢ Buzzer (BEEP)

A 1/2/4KHz BEEP signal can be generated on the BEEP pin, which is used to drive the external buzzer. 2 basic timers TIM10/11 and 1 LPTIM can function as multiplexed outputs to provide programmable clock source for buzzers Frequency, can support complementary output.

➢ Automatic wake-up timer (AWK)

AWK is used to provide an internal wake-up time reference when MCU enters low power mode. The time base is clocked by the internal low speed RC oscillator clock (LSI) or by the prescaled HSE crystal clock.

➢ Clock Trim/Monitoring Module (CLKTRIM)

The FE82160 embeds clock calibration circuit, can be used to calibrate the internal RC clock throughthe external precise crystal oscillator clock, or use the internal RC clock to detect whether the external crystal oscillator clock works fine.

➢ Unique ID (UID)

The FE82160 are shipped with a unique 16 byte device identification number.(0x180000F0-0x180000FF)

➢ Embedded Debug System

The embedded debugging solution provides a full-featured real-time debugger, which cooperates with standard mature Keil/IAR and other debugging and development software.
Supports 4 hard breakpoints and multiple soft breakpoints.

➢ Embedded Debug (DBG)

An encrypted embedded debugging solution that provides a full-featured real-time debugger.

Absolute Maximum Rating

- **AFE**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage	VDD	-0.3	4.0	V
V_{IN}	Input pin voltage	AINx+, AINx-, RINx+, RINx-, VCM	-0.3	4.0	V
V_{IO}	Digital I/O ports	EOC, SDA, SCL	-0.3	4.0	V
T_A	Operating ambient temperature range		-40	85	°C
T_{stg}	Storage temperature range		-55	150	°C
ESD	Human Body Model	AINx+,AINx-,RIN0+,RIN0-SDA,SCL,EOC	±2000		V
		AVDD, VCM	±1000		
	Charged Device Model		±500		

*Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

- **MCU**

Symbol	Paramete	Min	Typ	Max	Unit
VDD	voltage	2.5		4.0	V
VIO	pin voltage	-0.3		VDD+0.3	V
Tstorage	Storage temperature	-40	25	150	°C
Toperation	Operating temperature	-40	25	85	°C
fCPU	CPU Operating frequency	32.768K	4M	24M	Hz
VESD, HBM		8			KV
TESD, CDM		2			KV
LU	TA = +85 °C conforming to JESD78A	±300mA			

[1] Temperature test -40°C tests only in laboratory and Production Quality Qualification
[2] Frequency Test：CP test at 24MHz

Recommended Operating Condition

- **AFE**

Symbol	Description	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VDD	System power supply	VDD to VSS	2.7	3.3	3.6	V
ANALOG INPUTS						
V_{AINx}	Absolute input voltage	PGA enabled	Note(1)			
		PGA disabled	AVSS-0.3	—	AVDD+0.3	V
V_{IN}	Differential input voltage	$V_{IN} = V_{AINP} - V_{AINN}$	—	$\pm V_{REF}$/Gain	—	V
REFERENCE INPUTS						
V_{RINX}	Differential reference voltage	$V_{REF} = V_{REFP} - V_{REFN}$	0.3	—	AVDD-AVSS	V
V_{REFP}	Positive reference voltage		V_{REFN} + 0.3	—	AVDD	V
V_{REFN}	Negative reference voltage		AVSS	—	V_{REFP} - 0.3	V
DIGITAL INPUTS/OUTPUTS						
	GPIO ports	SDA, SCL, EOC	VSS	—	VDD	V
OPERATION TEMPERATURE						
T_A	Operating ambient temperature		-40	—	85	℃

Note (1) ：VAINX+ > AVSS + 0.3 + Vin x (Gain-1)/2 VAINX - AVDD - 0.3 - Vin x (Gain-1)/2

- **MCU**

Parameter	Symbol	Min	Typical	Max	reference
Voltage	VDD	2.7	3.6	V	
VCAP Capacitance	C_s	0.47	2.2	μF	1.0μF
Operating temperature	T_{OP}	-40	85	°C	

[1] Recommended working conditions are the conditions to ensure the normal operation of the chip device. All specification values for electrical characteristics are guaranteed within the range of recommended operating conditions. Use outside this condition may affect product reliability

[2] Our company does not make any guarantees for the use of items, conditions of use, or logical combinations that are not described in this data sheet

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