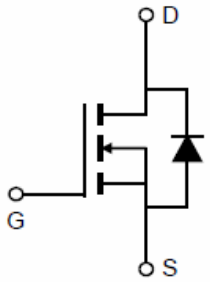
Features

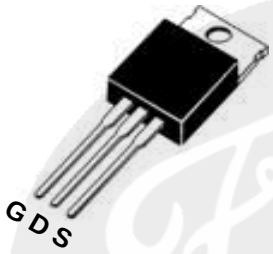
- Uses split-gate technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product
- Qualified according to JEDEC criteria

VDS	98V
$R_{DS(on)@VGS=10V}$	5.2mΩ
I_D	140A

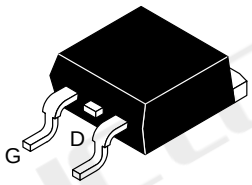
Application

- Motor Drivers
- UPS (Uninterruptible Power Supplies)
- DC/DC converter
- General purpose applications





TO-220AB



TO-263

Order Information

Part No.	Package	Marking	Shipping	Qty
FIR140N098PG	TO-220AB	FIR140N098P	Reel	800 PCS
FIR140N098RG	TO-263	FIR140N098R	Tube	1000 PCS

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	98	V
Continuous drain current T_C = 25°C T_C = 100°C	I_D	140 100	A
Pulsed drain current T_C = 25°C, t_p limited by T_{jmax}	$I_{D\ pulse}$	480	
Avalanche energy, single pulse	E_{AS}	689	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation T_C = 25°C	P_{tot}	200	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	℃

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal resistance, junction – case. Max	R_{thJC}	0.62	℃/W
Thermal resistance, junction – ambient. Max	R_{thJA}	62.0	

Electrical Characteristic, at Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Test Condition	Value			Unit
			min.	typ.	max.	
Static Characteristic						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA		98		V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA T_j=25°C	2.5		4.0	
Zero gate voltage drain current	I_{DSS}	V_{IS}=80V,V_{GS}=0V T_j=25°C T_A=125°C	- -	0.05 -	1 5	μA
Gate-source leakage current	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=50A, T_j=25°C T_j=125°C	- -	5.2 -	- -	mΩ
Transconductance	g_{fs}	V_{DS}=5V,I_D=50A	-	84.2	-	S
Dynamic Characteristic						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=40V, f=1MHz	-	3900	-	pF
Output Capacitance	C_{oss}		-	1100	-	
Reverse Transfer Capacitance	C_{rss}		-	35	-	
Gate Total Charge	Q_G	V_{GS}=10V, V_{DS}=40V, I_D=50A, f=1MHz	-	75.0	-	nC
Gate-Source charge	Q_{gs}		-	15.0	-	
Gate-Drain charge	Q_{gd}		-	13.0	-	
Turn-on delay time	$t_{d(on)}$	T_j=25°C, V_{GS}=10V, V_{DS}=40V, R_L=3Ω	-	20.1	-	ns
Rise time	t_r		-	38.9	-	
Turn-off delay time	$t_{d(off)}$		-	45.1	-	
Fall time	t_f		-	22.8	-	
Gate resistance	R_G	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	3.3	-	Ω
Body Diode Characteristic						
Body Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_{SD}=50A	-	0.95	1.4	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=20A, dI/dt=500A/μs		60		ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=20A, dI/dt=50A/μs		52		nC

Typical Performance Characteristics

Figure 1. Typ. Output Characteristics (Tj=25℃)

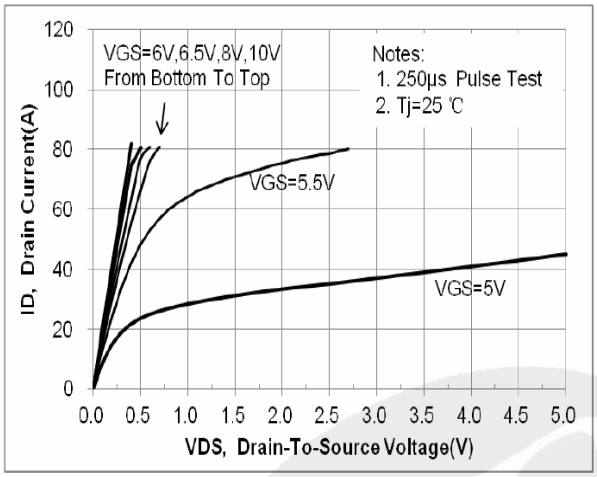


Figure 2. Transfer Characteristics (Junction Temperature)

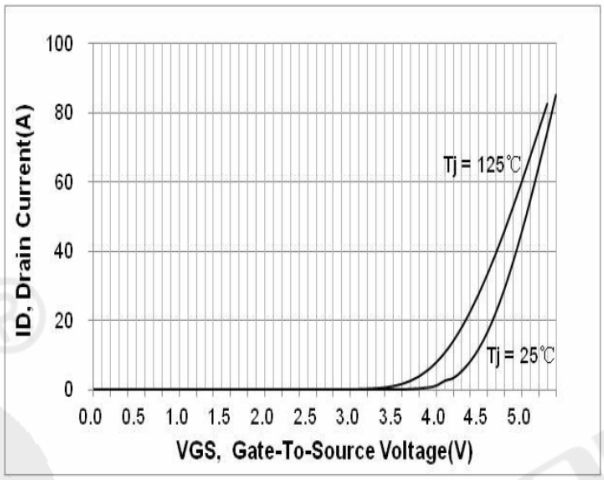


Figure 3. On-Resistance vs. Drain Current and Gate Voltage Figure

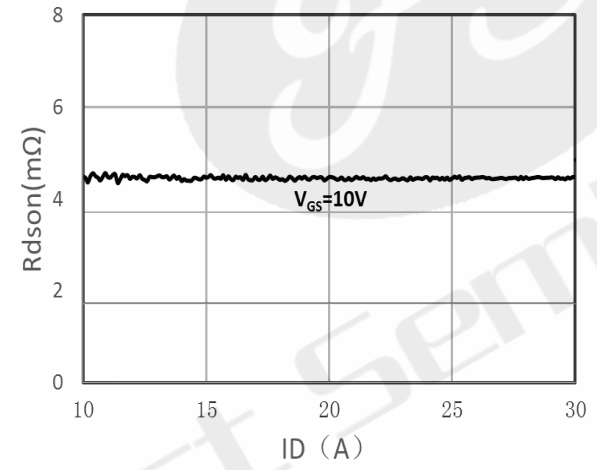


Figure 4. On-Resistance vs. Junction Temperature

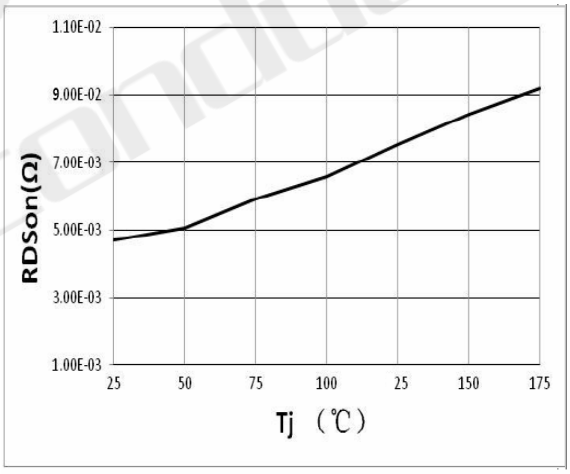


Figure 5. On-Resistance vs. Gate-Source Voltage (Junction Temperature)

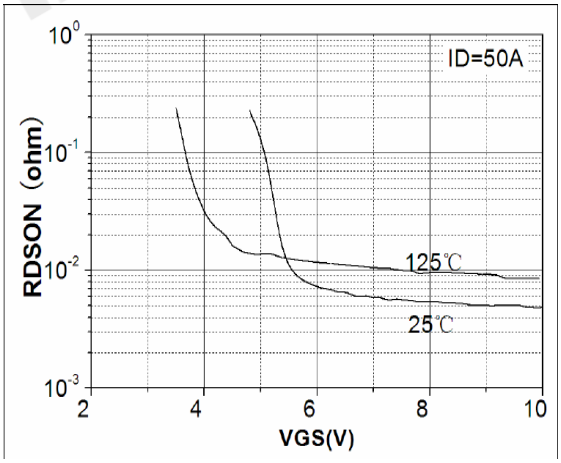


Figure 6. Body-Diode Characteristics (Junction Temperature)

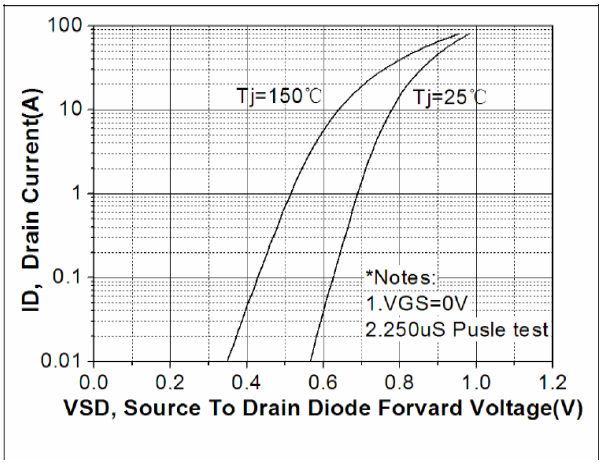


Figure 7. Gate-Charge Characteristics

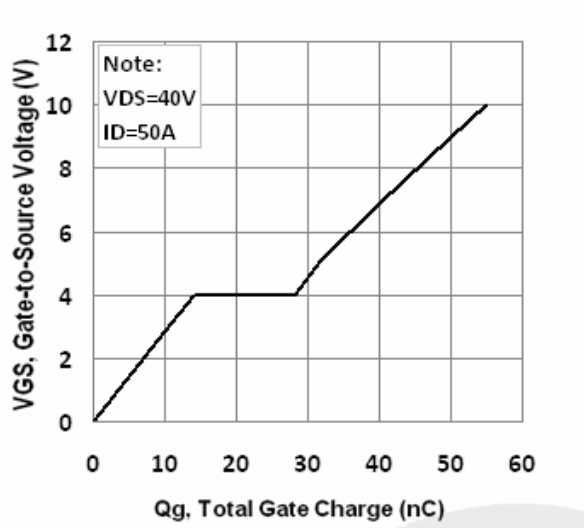


Figure 8. Capacitance Characteristics

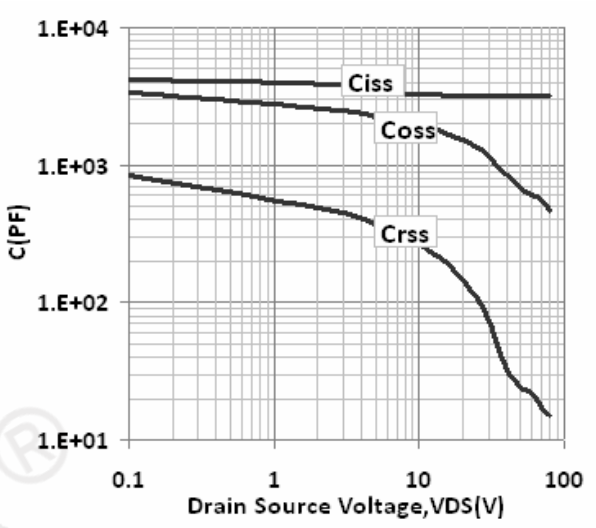


Figure 9: Normalized Maximum Transient Thermal Impedance (R_{thJC})

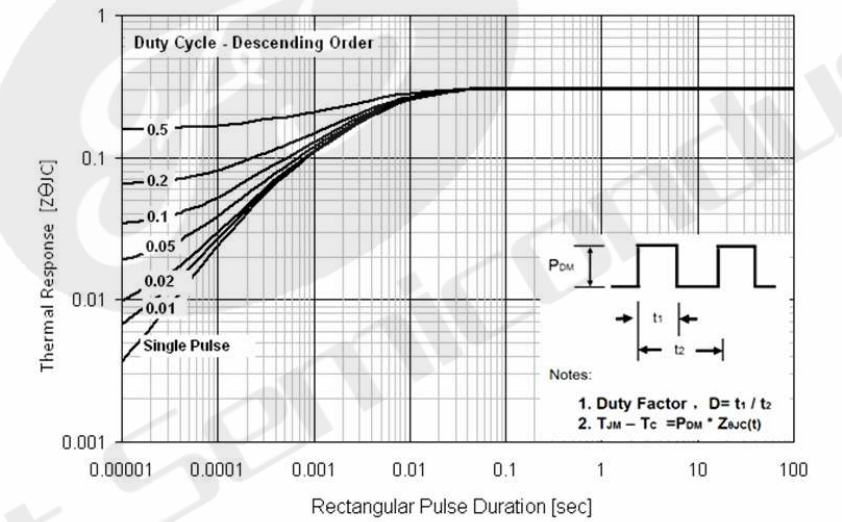
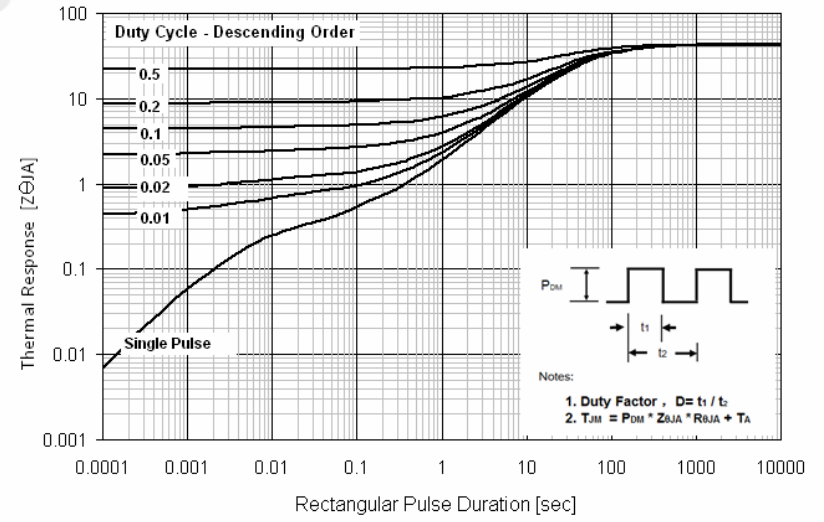
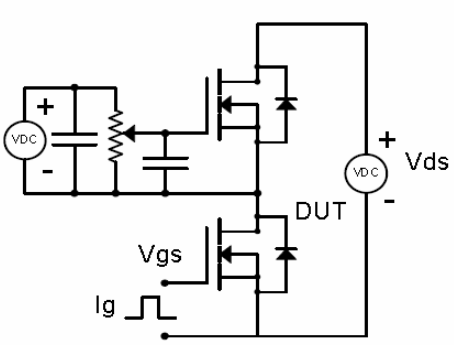


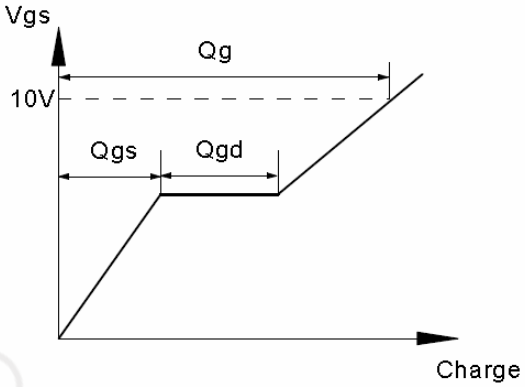
Figure 10: Normalized Maximum Transient Thermal Impedance (R_{thJA})



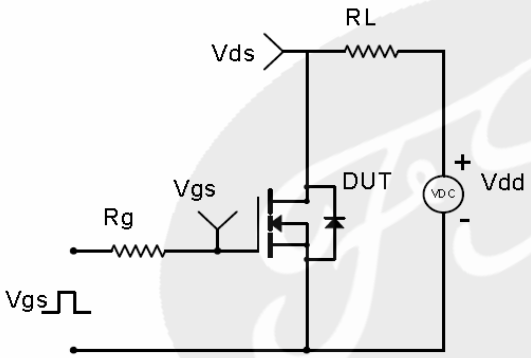
Test Circuit & Waveform

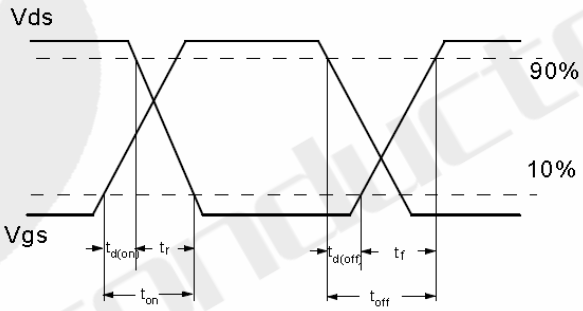
Gate Charge Test Circuit & Waveform



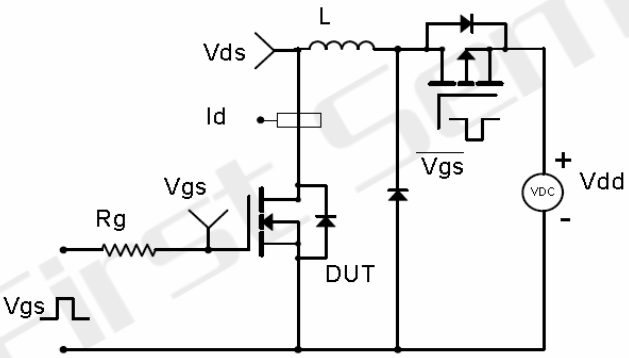


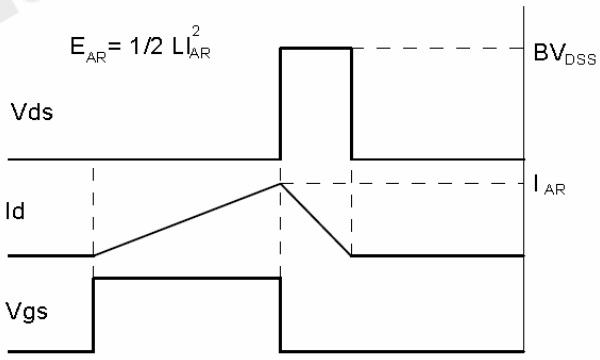
Resistive Switching Test Circuit & Waveforms



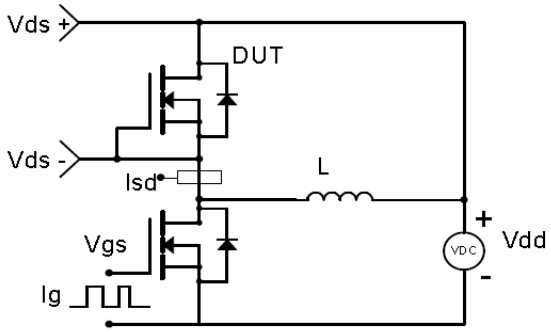


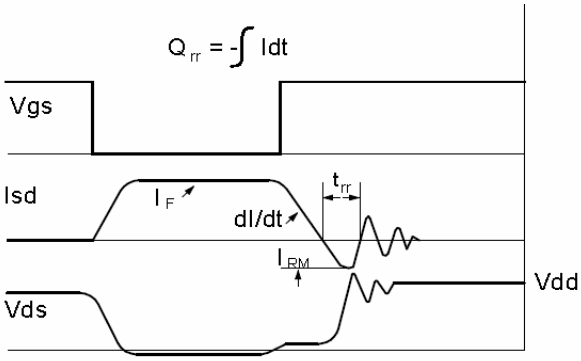
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



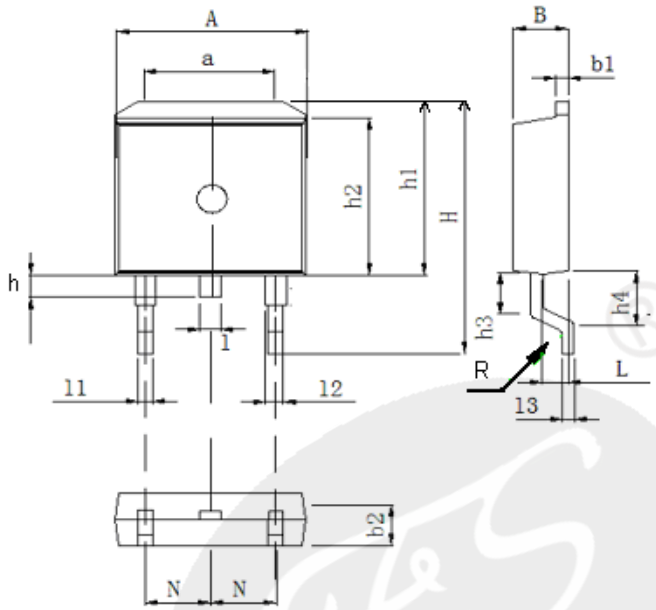


Diode Recovery Test Circuit & Waveforms



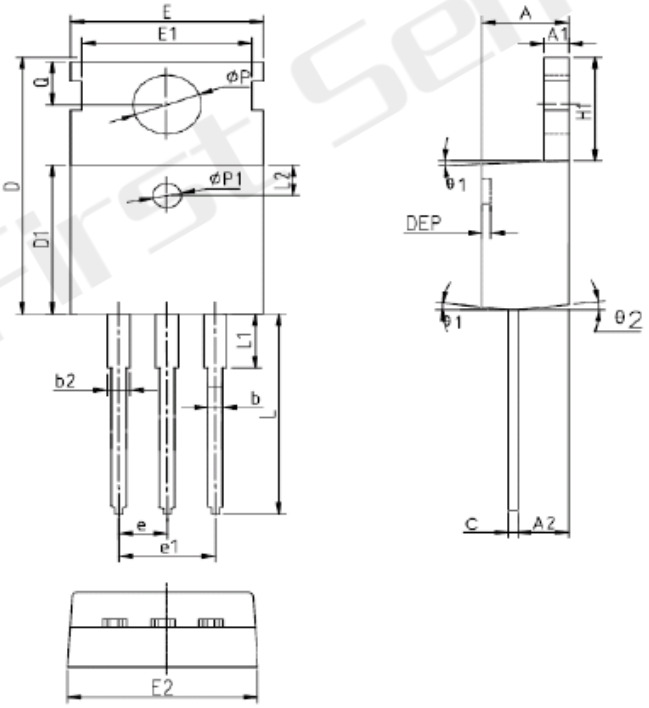


TO-263 Package Outline



DIM	MILLIMETERS
A	9.8±0.2
a	7.4±0.2
B	4.5±0.2
b1	1.3±0.05
b2	2.4±0.2
H	15.5±0.3
h	1.54±0.2
h1	10.5±0.2
h2	9.2±0.1
h3	1.54±0.2
h4	2.7±0.2
L	2.4±0.2
l	1.3±0.1
l1	0.8±0.1
l2	1.3±0.1
l3	0.5±0.1
N	2.45

TO-220 Package Outline



SYMBOL	MM		
	MIN	NOM	MAX
A	4.40	4.57	4.70
A1	1.27	1.30	1.33
A2	2.35	2.40	2.50
b	0.77	-	0.90
b2	1.23	-	1.36
C	0.48	0.50	0.52
D	15.40	15.60	15.80
D1	9.00	9.10	9.20
DEP	0.05	0.10	0.20
E	9.70	9.90	10.10
E1	-	8.70	-
E2	9.80	10.00	10.20
Øp1	1.40	1.50	1.60
e	2.54BSC		
e1	5.08BSC		
H1	6.40	6.50	6.60
L	12.75	-	13.17
L1	-	-	3.95
L2	2.50REF.		
Øp	3.57	3.60	3.63
Q	2.73	2.80	2.87
θ1	5°	7°	9°
θ2	1°	3°	5°

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	