



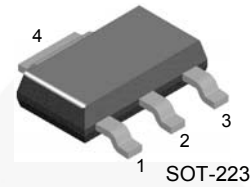
October 2014

FJT44

NPN Epitaxial Silicon Transistor

Features

- High-Voltage Transistor



1. Base 2,4. Collector 3. Emitter

Ordering Information

Part Number	Marking	Package	Packing Method, Size
FJT44TF	FJT44	SOT-223 4L	Tape and Reel, 4000 pcs
FJT44KTF	FJT44	SOT-223 4L	Tape and Reel, 2500 pcs

Absolute Maximum Ratings^{(1),(2)}

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	500	V
V_{CEO}	Collector-Emitter Voltage	400	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current	300	mA
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Notes:

1. These ratings are based on a maximum junction temperature of 150°C .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

Thermal Characteristics⁽³⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Max.	Unit
P_D	Power Dissipation, $T_C = 25^\circ\text{C}$	2	W
	Derate Above 25°C	16	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

Note:

3. Device is mounted on FR-4 PCB 36 mm × 18 mm × 1.5 mm; mounting pad for the collector lead minimum 6 cm².

Electrical Characteristics⁽⁴⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 100\ \mu\text{A}$, $I_E = 0$	500			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 1\ \text{mA}$, $I_B = 0$	400			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 100\ \mu\text{A}$, $I_C = 0$	6			V
I_{CBO}	Collector-Base Cut-Off Current	$V_{CB} = 400\ \text{V}$, $I_E = 0$			100	nA
I_{CES}	Collector-Emitter Cut-Off Current	$V_{CE} = 400\ \text{V}$, $V_{BE} = 0$			500	nA
I_{EBO}	Emitter-Base Cut-Off Current	$V_{EB} = 4\ \text{V}$, $I_C = 0$			100	nA
h_{FE}	DC Current Gain	$V_{CE} = 10\ \text{V}$, $I_C = 1\ \text{mA}$	40			
		$V_{CE} = 10\ \text{V}$, $I_C = 10\ \text{mA}$	50		200	
		$V_{CE} = 10\ \text{V}$, $I_C = 50\ \text{mA}$	45			
		$V_{CE} = 10\ \text{V}$, $I_C = 100\ \text{mA}$	40			
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 1\ \text{mA}$, $I_B = 0.1\ \text{mA}$			0.40	V
		$I_C = 10\ \text{mA}$, $I_B = 1\ \text{mA}$			0.50	
		$I_C = 50\ \text{mA}$, $I_B = 5\ \text{mA}$			0.75	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 10\ \text{mA}$, $I_B = 1\ \text{mA}$			0.75	V
C_{obo}	Output Capacitance	$V_{CB} = 20\ \text{V}$, $I_E = 0$, $f = 1.0\ \text{MHz}$			7	pF

Note:

4. Pulse test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2.0\%$

Typical Performance Characteristics

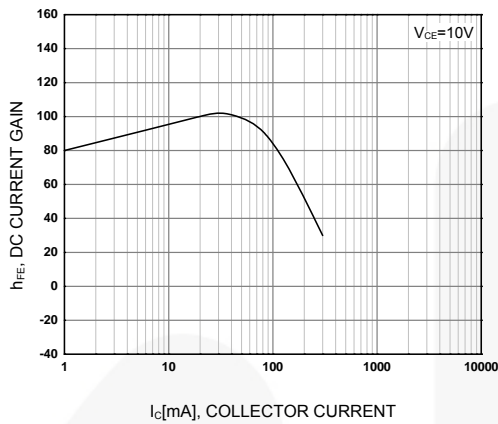


Figure 1. DC Current Gain

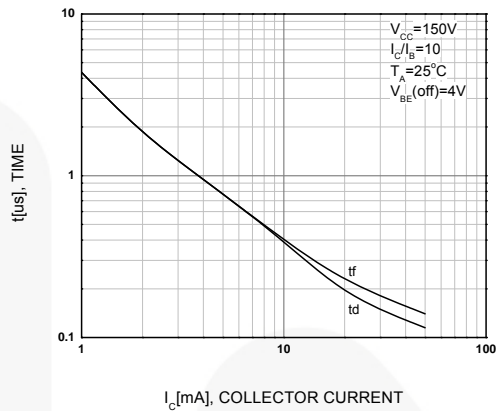


Figure 2. Turn-On Switching Times

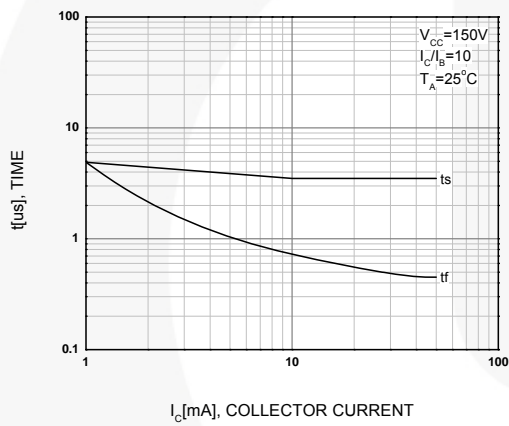


Figure 3. Turn-Off Switching Times

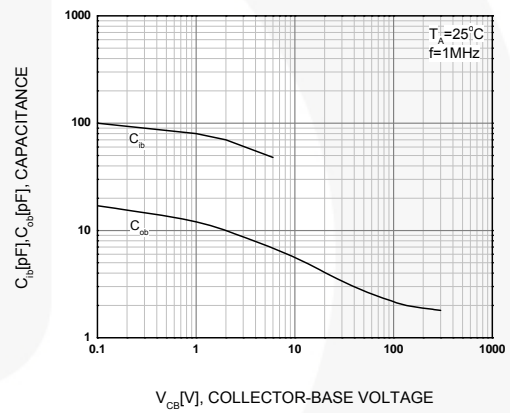


Figure 4. Capacitance

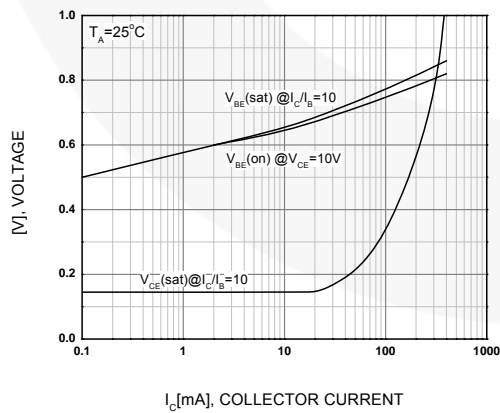


Figure 5. On Voltage

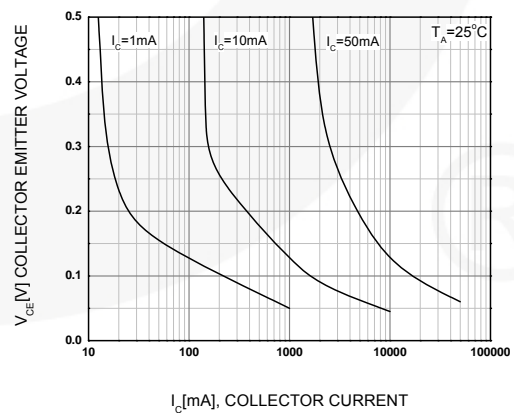


Figure 6. Collector Saturation Region

Typical Performance Characteristics (Continued)

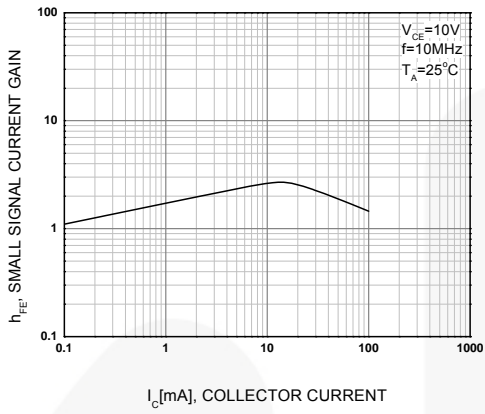


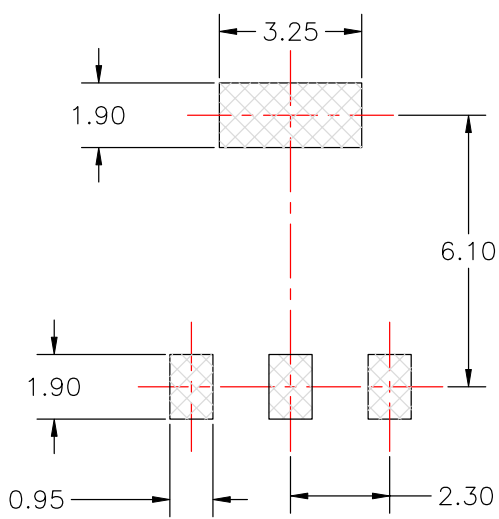
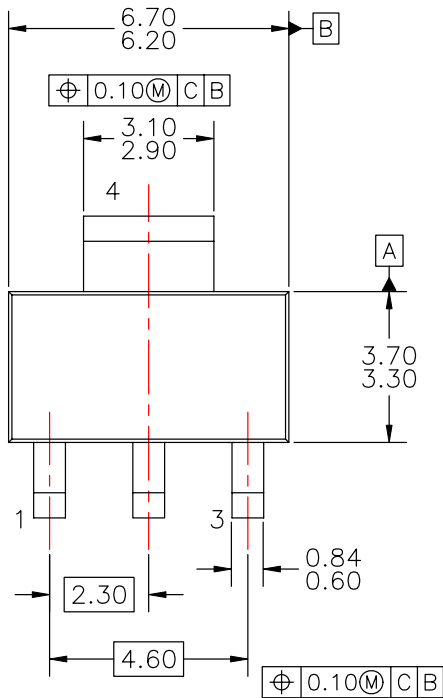
Figure 7. High Frequency Current Gain



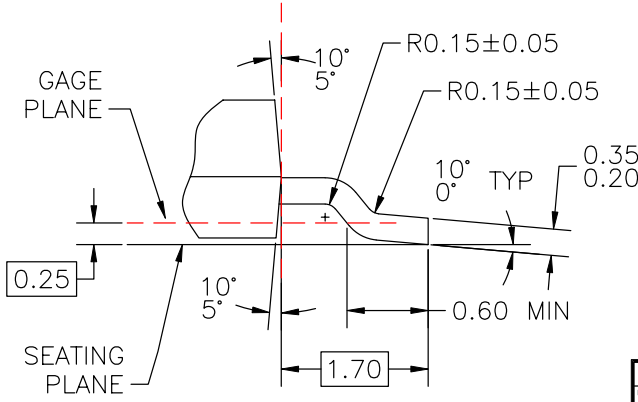
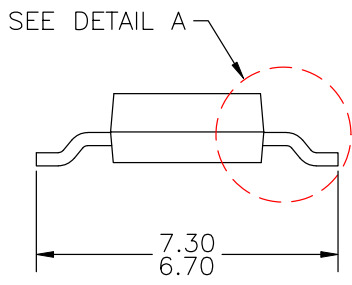
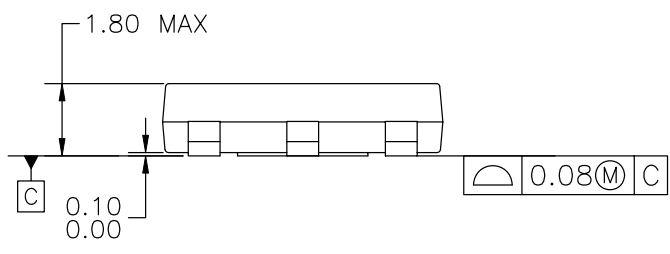
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APPROVED
July-14-2008

REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 ±0.03 TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.8 ±0.05 TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 ±0.03 TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 ±0.33 TO 3.3; CHG BODY LN FR 6.53 ±0.33 TO 6.3; CHG TOTAL PKG WID FR 6.94 ±0.33 TO 7.3; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE: 2:1






- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING BASED ON JEDEC REGISTRATION TO-261, VARIATION AA.
 - B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - C) ALL DIMENSIONS ARE IN MILLIMETERS.
 - D) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - E) LANDPATTERN NAME: SOT230P700X180-4BN
 - F) DRAWING FILENAME: MKT-MA04AREV2

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™
DRAWN: J.U. COMPARATIVO JR.	26FEB2008	
CHECKED: L.Z. STA CRUZ		
APPROVED: M.R. GESTOLE		
G.S. BAJE		MOLDED PACKAGE SOT-223, 4 LEAD
		SCALE: 1:1
		SIZE: A3
		DRAWING NUMBER: MKT-MA04A
		REV: 2
		FORMERLY: N/A
		SHEET: 1 OF 1



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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