

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

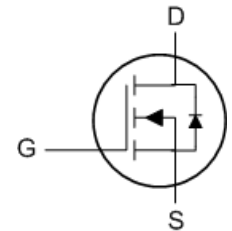
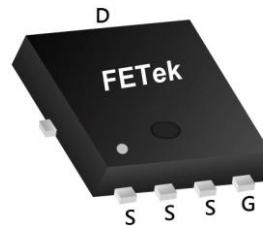
Product Summary


BVDSS	RDSON	ID
80V	6.5mΩ	122A

Description

The FKBA8024A is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKBA8024A meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PRPAK5X6 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	80	V
V_{GS}	Gate-Source Voltage	±20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	122	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	78.6	A
I_{DM}	Pulsed Drain Current ²	300	A
EAS	Single Pulse Avalanche Energy ³	246.4	mJ
I_{AS}	Avalanche Current	70.2	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	156	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	0.8	°C/W

**Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	80	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.059	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	---	---	6.5	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2	---	4	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.6	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=64V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=64V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	50	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.4	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=64V, V_{GS}=10V, I_D=30A$	---	83.7	---	nC
Q_{gs}	Gate-Source Charge		---	28.6	---	
Q_{gd}	Gate-Drain Charge		---	29.3	---	
$T_d(on)$	Turn-On Delay Time	$V_{DD}=40V, V_{GS}=10V, R_G=3.3\Omega, I_D=30A$	---	38.1	---	ns
T_r	Rise Time		---	73.3	---	
$T_d(off)$	Turn-Off Delay Time		---	51.6	---	
T_f	Fall Time		---	26.1	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	5580	---	μF
C_{oss}	Output Capacitance		---	571	---	
C_{rss}	Reverse Transfer Capacitance		---	278	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	122	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	300	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=30A, di/dt=100A/\mu\text{s}, T_J=25^\circ\text{C}$	---	26.7	---	nS
Q_{rr}	Reverse Recovery Charge		---	27.9	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=70.2A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 90A.

Typical Characteristics

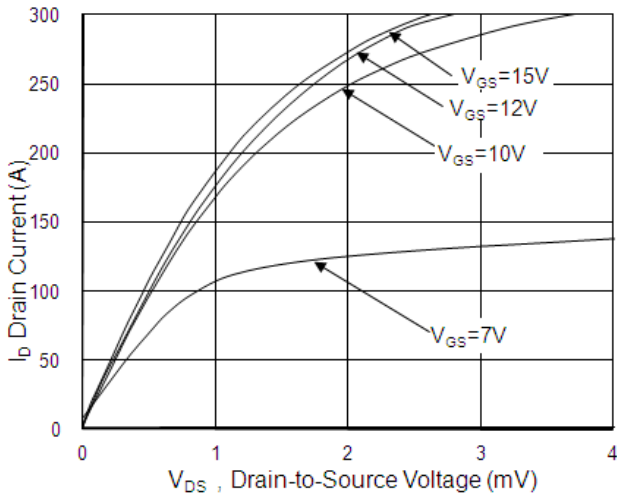


Fig.1 Typical Output Characteristics

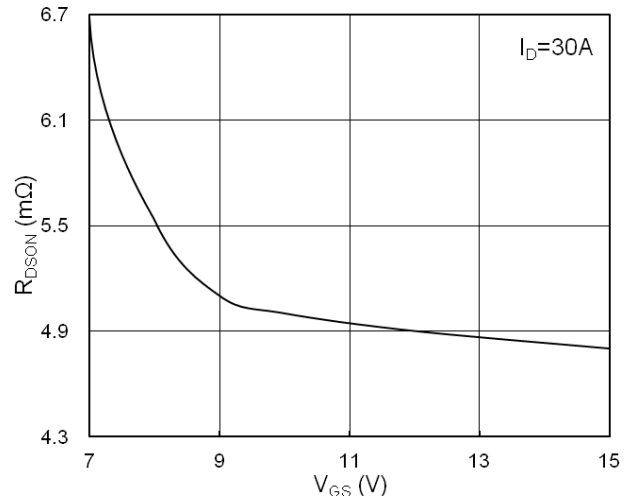


Fig.2 On-Resistance v.s Gate-Source

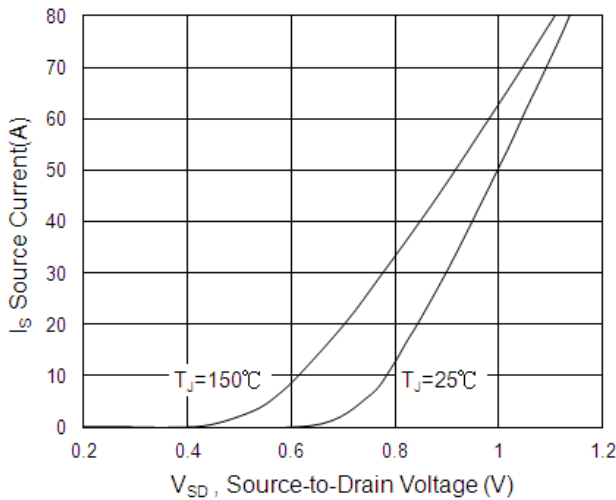


Fig.3 Forward Characteristics of Reverse

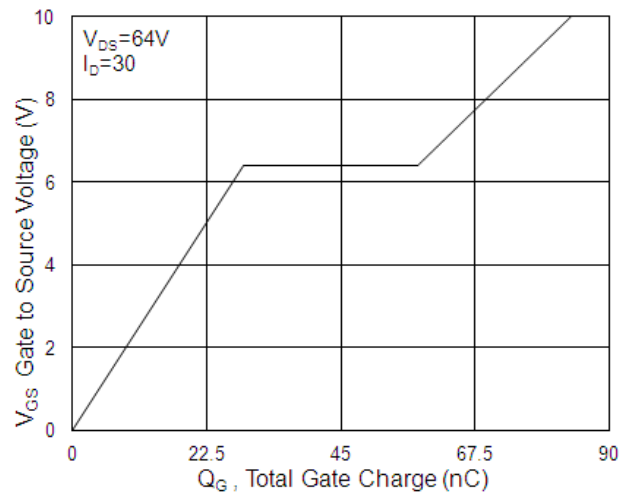


Fig.4 Gate-Charge Characteristics

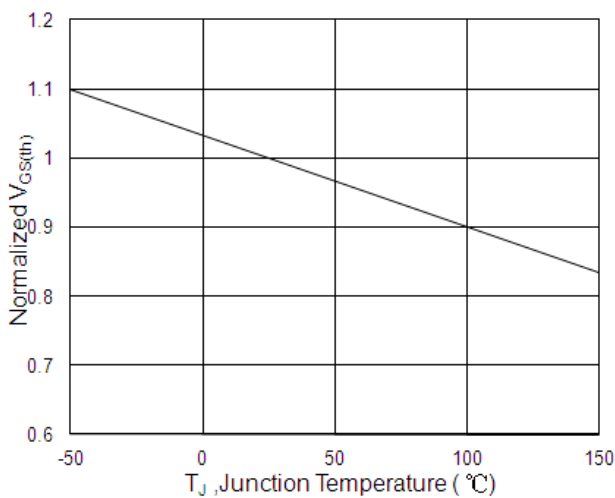


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

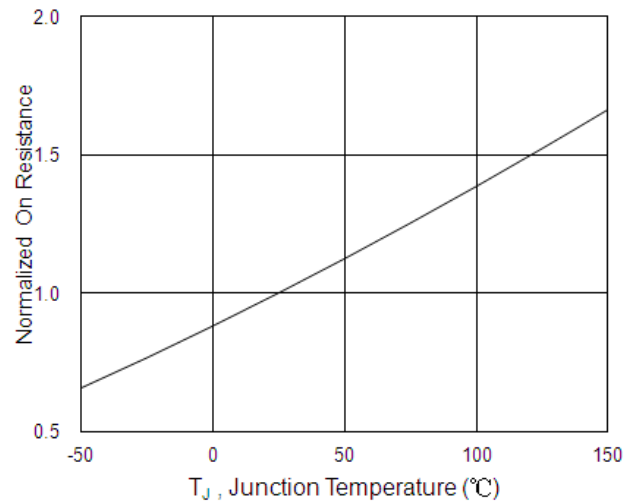


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

N-Ch 80V Fast Switching MOSFETs

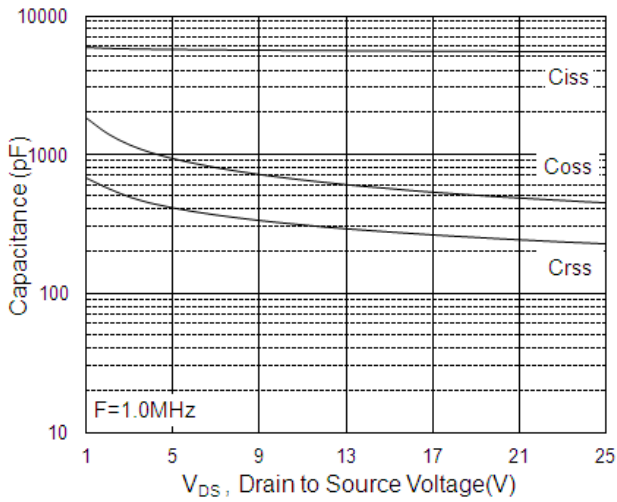


Fig.7 Capacitance

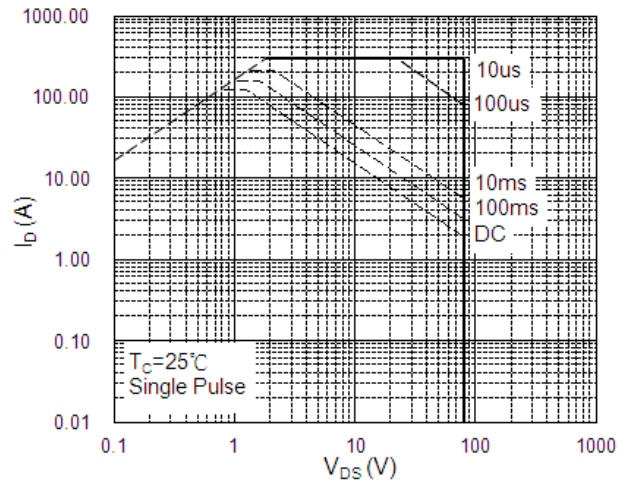


Fig.8 Safe Operating Area

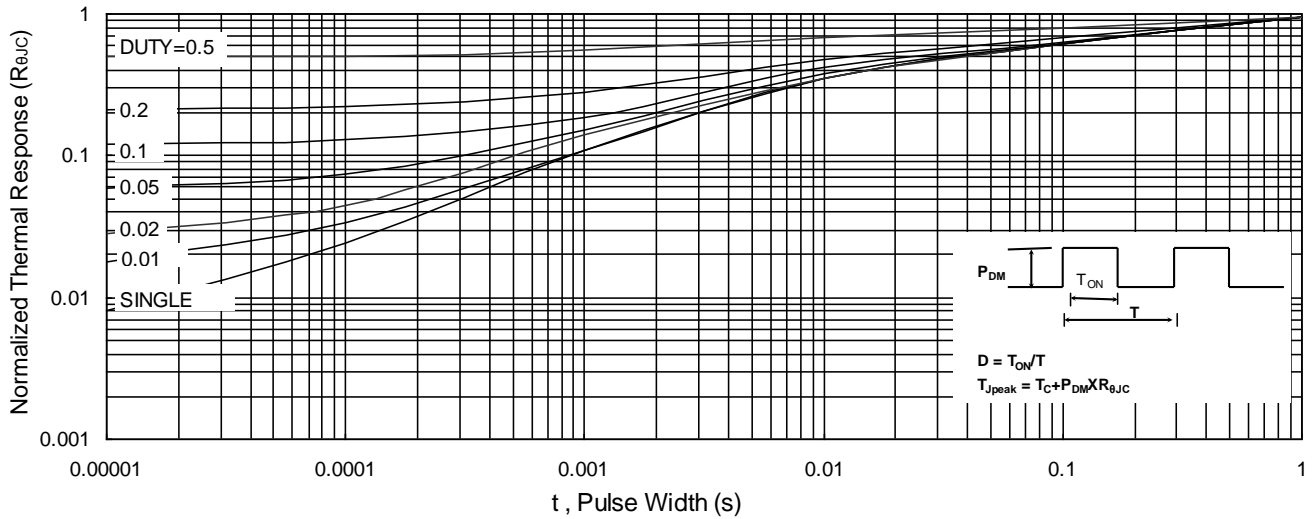


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform

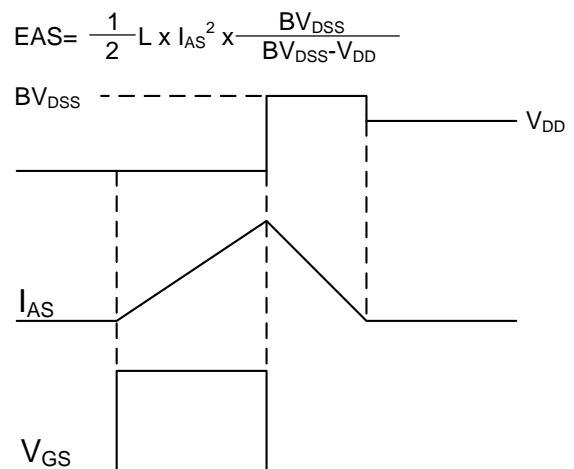


Fig.11 Unclamped Inductive Switching Waveform