


Features

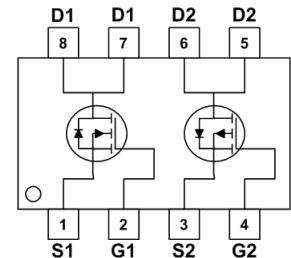
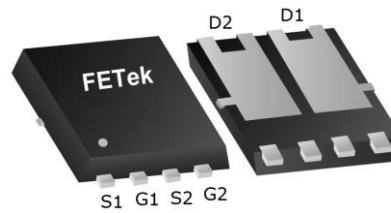
- Advanced Trench MOS Technology
- 100% EAS Guaranteed
- Reliable and Rugged
- Green Device Available

Product Summary

BVDSS	RDSON	ID
100V	100mΩ	6.0A
-100V	220mΩ	-4.1A

Applications

- Power Management.
- DC Motor Control.

PRPAK3X3 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	100	-100	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.0	-4.1	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.8	-2.6	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	2.6	-1.8	A
$I_D@T_A=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	1.6	-1.1	A
I_{DM}	Pulsed Drain Current ²	20	-20	A
EAS	Single Pulse Avalanche Energy ³	25	49	mJ
I_{AS}	Avalanche Current	10	-14	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	7.8	7.8	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	1.5	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	16	$^\circ C/W$

**N-Channel Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=4A$	---	---	100	m Ω
		$V_{GS}=4.5V, I_D=3A$	---	---	125	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.7	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	μA
		$V_{DS}=80V, V_{GS}=0V, T_J=85^\circ C$	---	---	30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	3.5	---	Ω
Q_g	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V, I_D=2A$	---	15	---	nC
Q_{gs}	Gate-Source Charge		---	3.2	---	
Q_{gd}	Gate-Drain Charge		---	2.6	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, V_{GS}=10V, R_G=3.3\Omega, I_D=1A$	---	8	---	ns
T_r	Rise Time		---	12	---	
$T_{d(off)}$	Turn-Off Delay Time		---	20	---	
T_f	Fall Time		---	6	---	
C_{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1MHz$	---	987	---	pF
C_{oss}	Output Capacitance		---	38	---	
C_{rss}	Reverse Transfer Capacitance		---	26	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ C$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.5mH, I_{AS}=10A$
- 4.The power dissipation is limited by 150 $^\circ C$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-100	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-3A$	---	---	220	m Ω
		$V_{GS}=-4.5V, I_D=-2A$	---	---	255	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	---	-2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-80V, V_{GS}=0V, T_J=85^\circ\text{C}$	---	---	-30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	13	---	Ω
Q_g	Total Gate Charge (-10V)	$V_{DS}=-50V, V_{GS}=-10V, I_D=-2A$	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	3.4	---	
Q_{gd}	Gate-Drain Charge		---	2.9	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-30V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-1A$	---	9	---	ns
T_r	Rise Time		---	6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	39	---	
T_f	Fall Time		---	33	---	
C_{iss}	Input Capacitance	$V_{DS}=-30V, V_{GS}=0V, f=1\text{MHz}$	---	1228	---	pF
C_{oss}	Output Capacitance		---	41	---	
C_{rss}	Reverse Transfer Capacitance		---	29	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	4.1	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.5\text{mH}, I_{AS}=-14A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

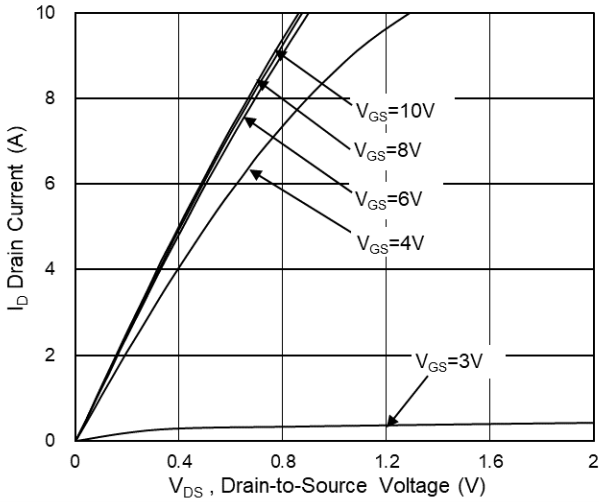


Fig.1 Typical Output Characteristics

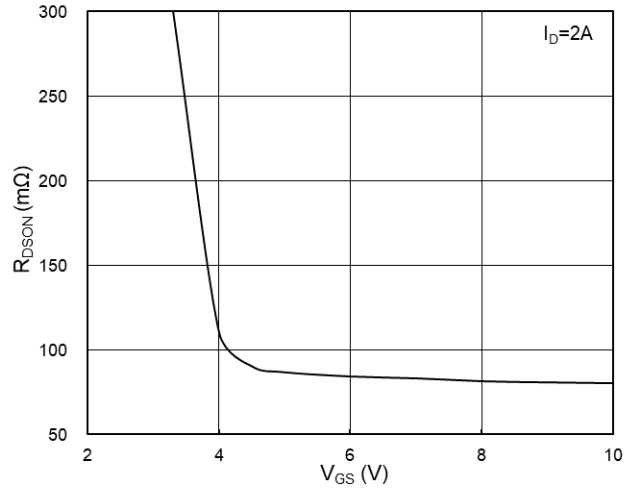


Fig.2 On-Resistance vs G-S Voltage

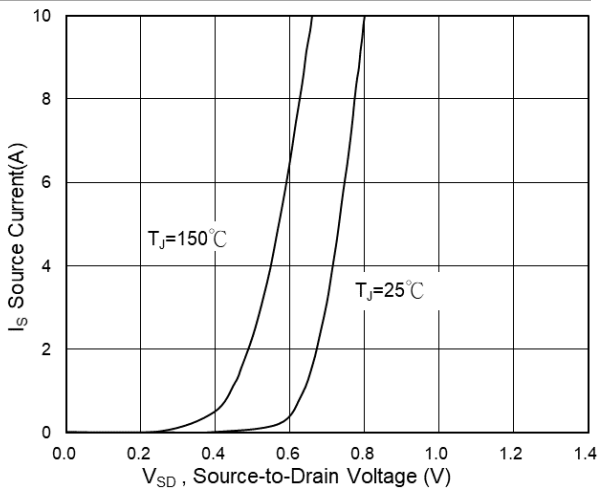


Fig.3 Source Drain Forward Characteristics

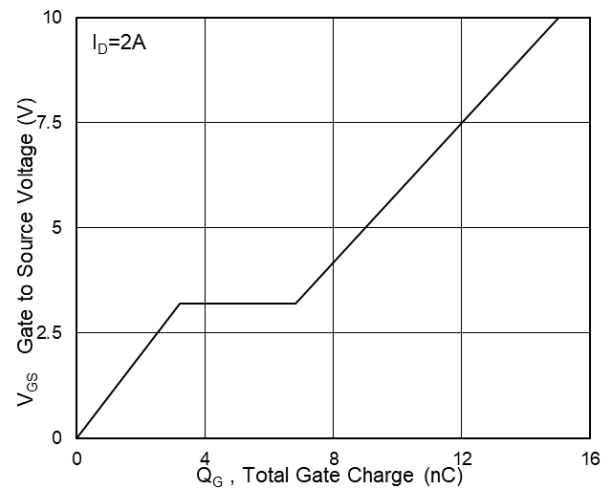


Fig.4 Gate-Charge Characteristics

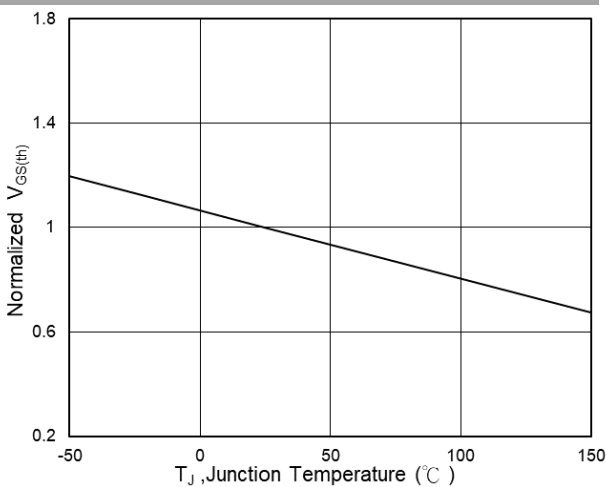


Fig.5 Normalized $V_{GS(th)}$ vs T_J

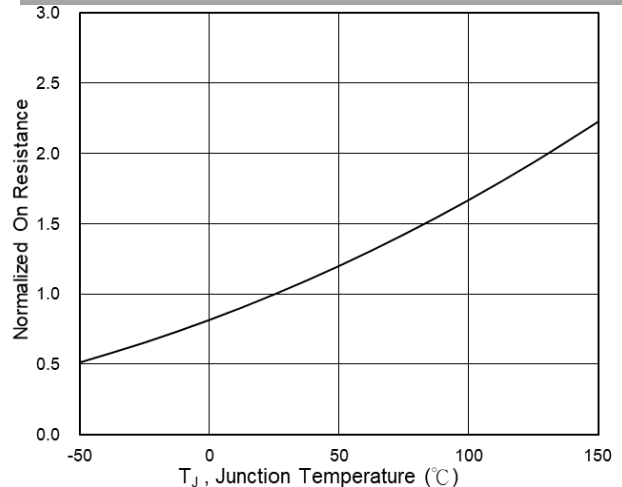


Fig.6 Normalized $R_{DS(on)}$ vs T_J

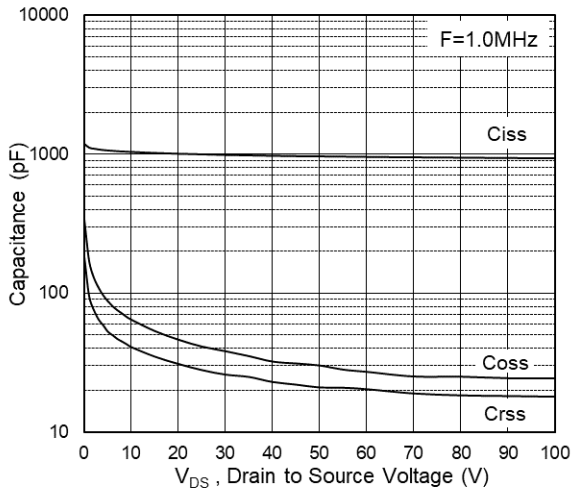


Fig.7 Capacitance

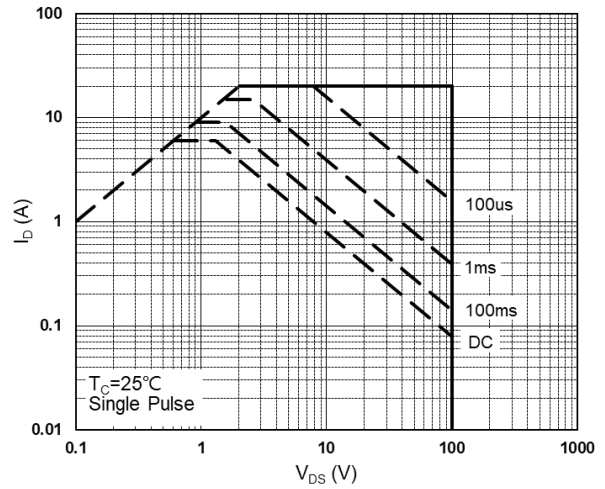


Fig.8 Safe Operating Area

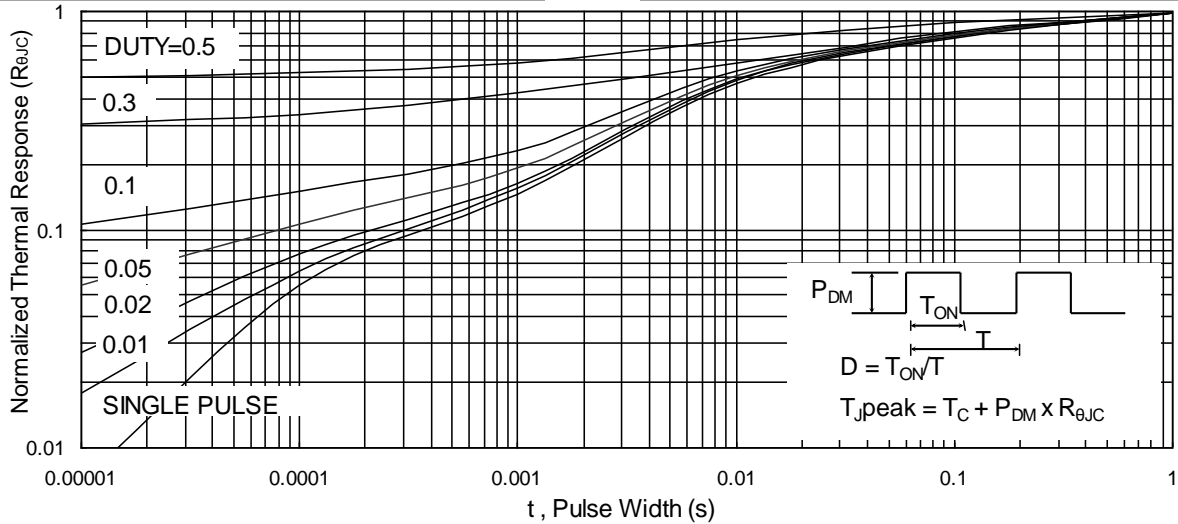


Fig.9 Normalized Maximum Transient Thermal Impedance

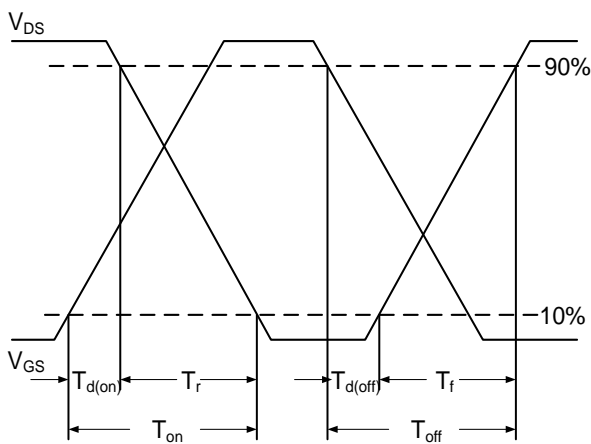


Fig.10 Switching Time Waveform

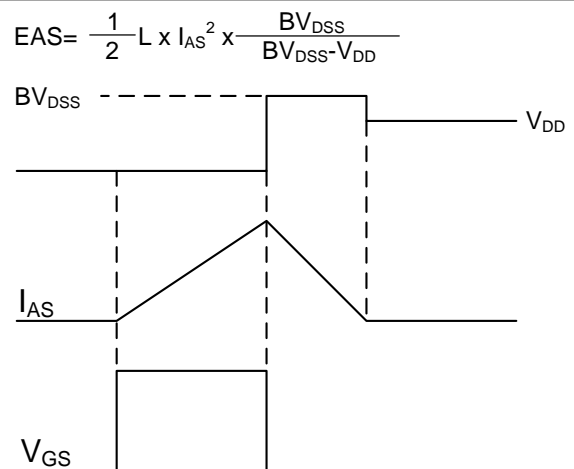


Fig.11 Unclamped Inductive Waveform

P-Channel Typical Characteristics

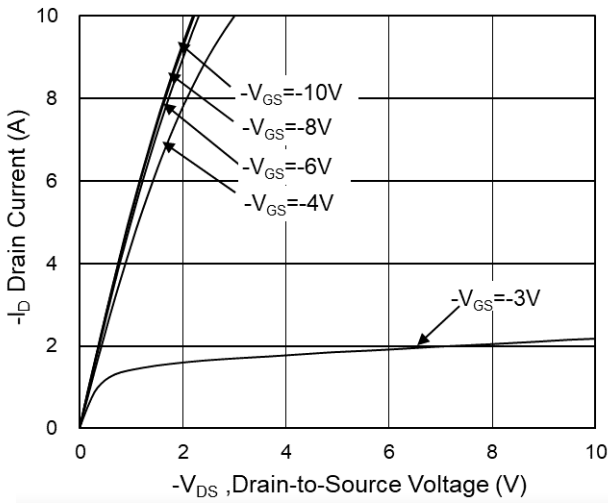


Fig.1 Typical Output Characteristics

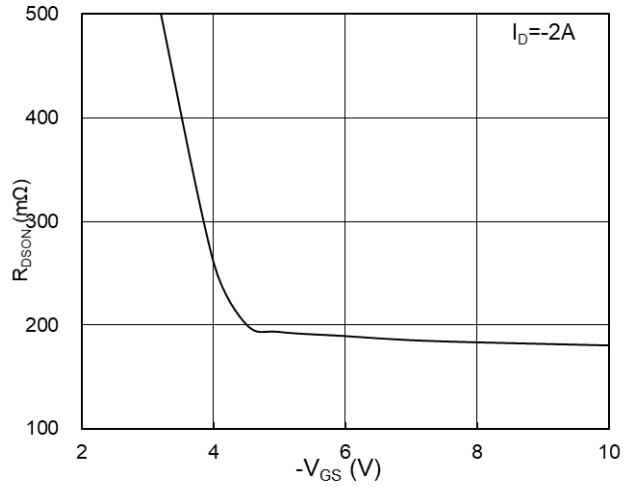


Fig.2 On-Resistance vs G-S Voltage

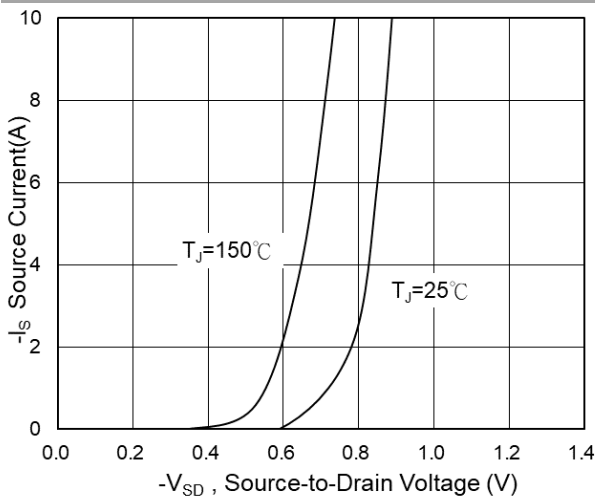


Fig.3 Source Drain Forward Characteristics

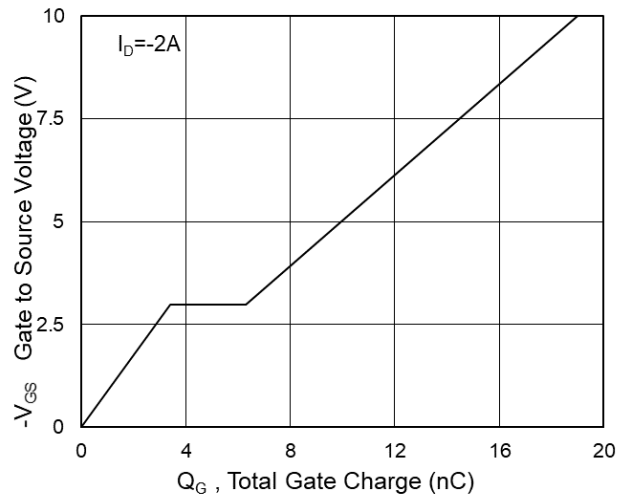


Fig.4 Gate-Charge Characteristics

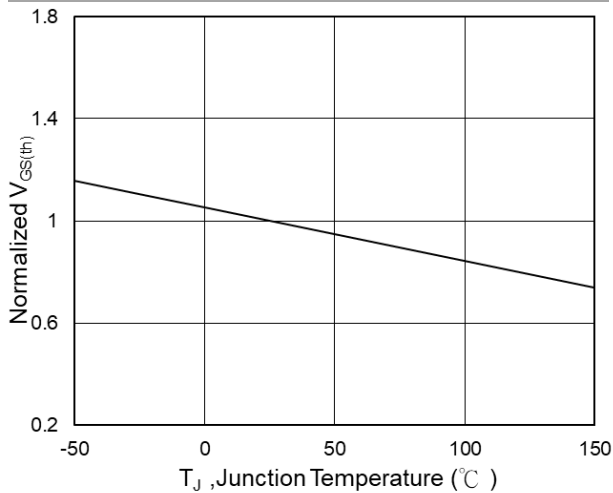


Fig.5 Normalized $V_{GS(th)}$ vs T_J

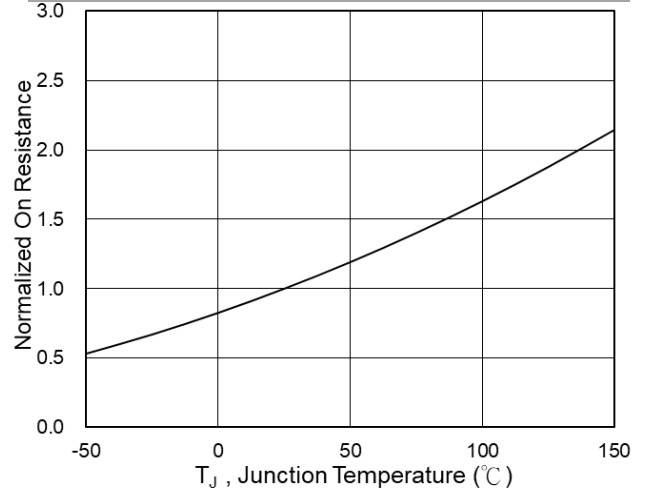


Fig.6 Normalized $R_{DS(on)}$ vs T_J

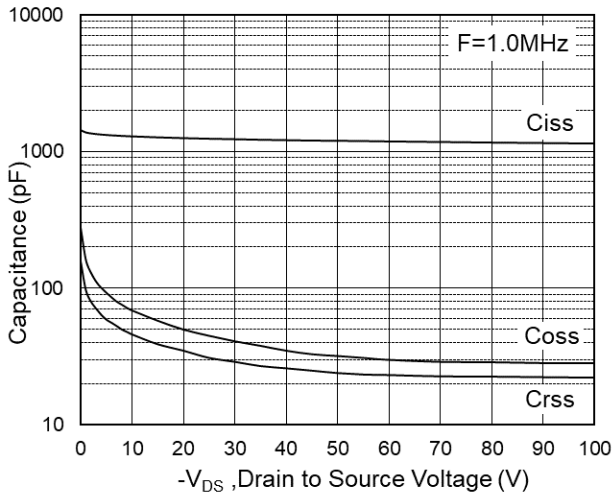


Fig.7 Capacitance

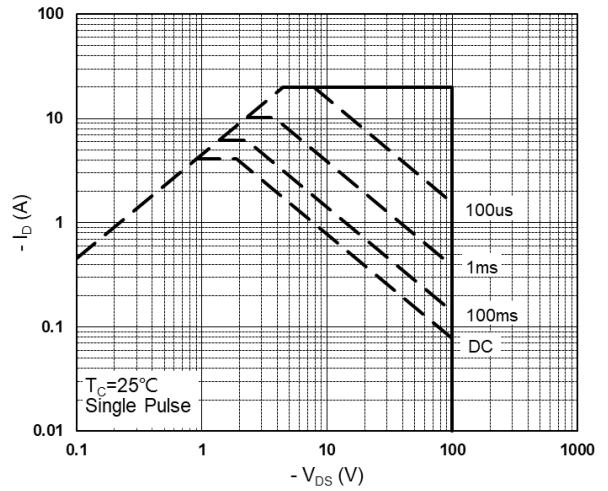


Fig.8 Safe Operating Area

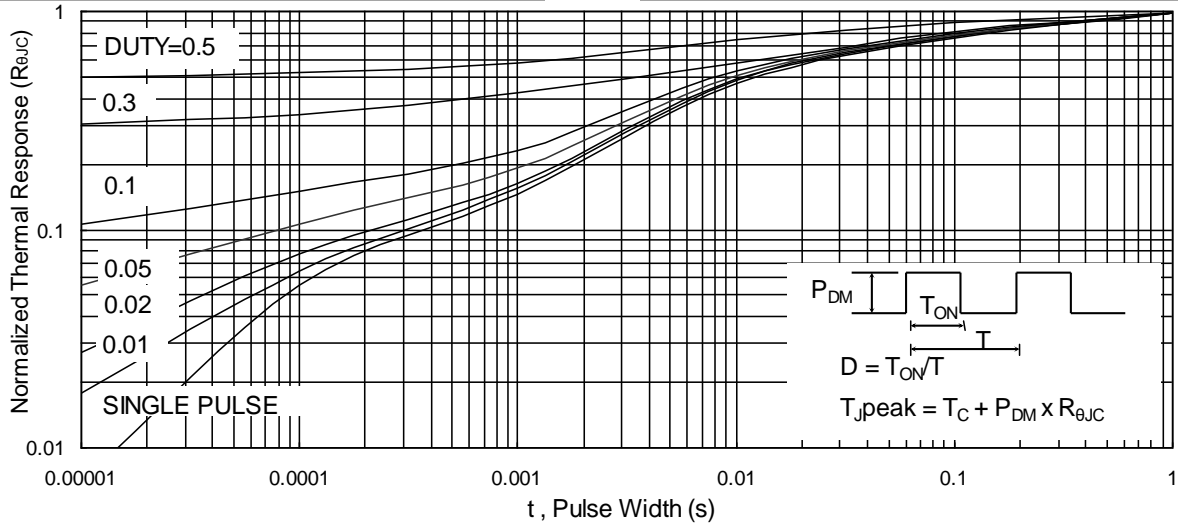


Fig.9 Normalized Maximum Transient Thermal Impedance

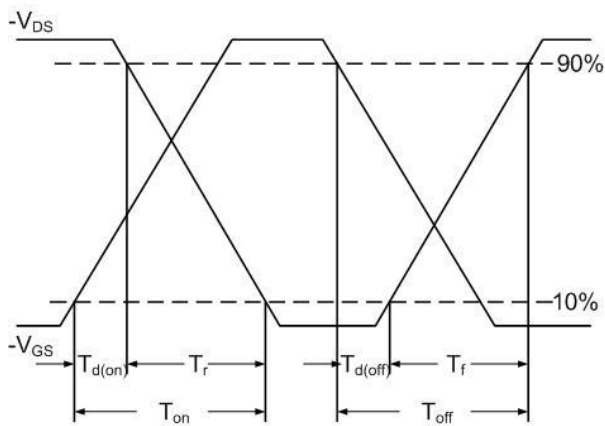


Fig.10 Switching Time Waveform

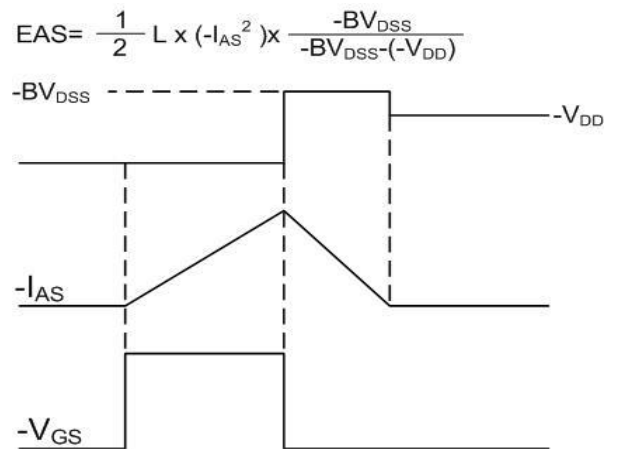


Fig.11 Unclamped Inductive Waveform