

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

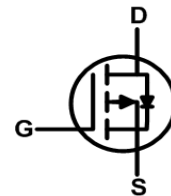
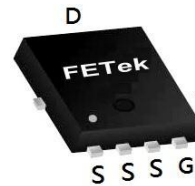
**Product Summary**


BVDSS	RDSON	ID
-30V	8.7mΩ	-50A

**Description**

The FKBB3115 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKBB3115 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

**PRPAK3X3 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-50	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-32	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-200	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	125	mJ
$I_{AS}$	Avalanche Current	-50	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	38	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	65	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	2.3	$^\circ C/W$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-30A$	---	7.3	8.7	m $\Omega$
		$V_{GS}=-4.5V, I_D=-15A$	---	11	13.5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	---	-2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	$\mu A$
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-30A$	---	25	---	S
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-15A$	---	30	---	nC
$Q_{gs}$	Gate-Source Charge		---	10	---	
$Q_{gd}$	Gate-Drain Charge		---	10.4	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega$ $I_D=-15A$	---	9.4	---	ns
$T_r$	Rise Time		---	10.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	117	---	
$T_f$	Fall Time		---	24	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	3448	---	pF
$C_{oss}$	Output Capacitance		---	508	---	
$C_{rss}$	Reverse Transfer Capacitance		---	421	---	

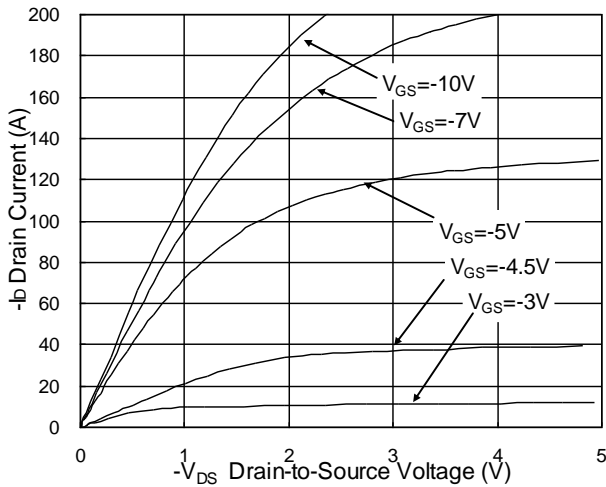
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	-50	A
$I_{SM}$	Pulsed Source Current <sup>2</sup>		---	---	-130	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V
$t_{rr}$	Reverse Recovery Time	$I_F=-15A, dI/dt=100A/\mu s$ ,	---	20	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	9.5	---	nC

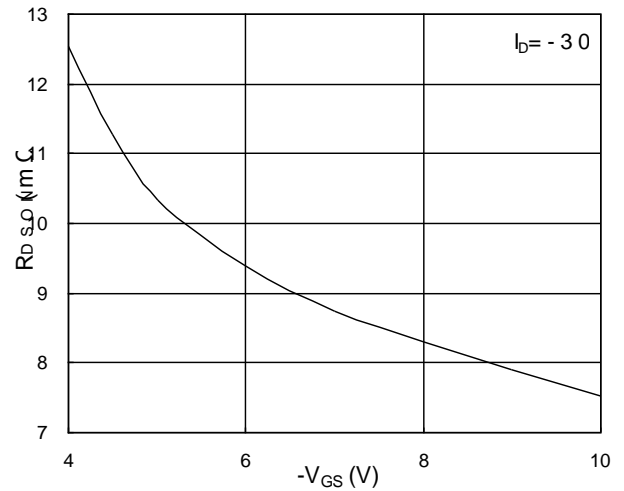
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-50A$
- 4.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  , in real applications , should be limited by total power dissipation.

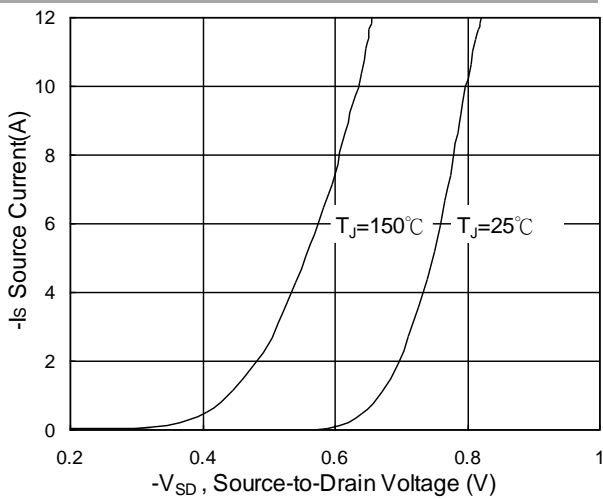
**Typical Characteristics**



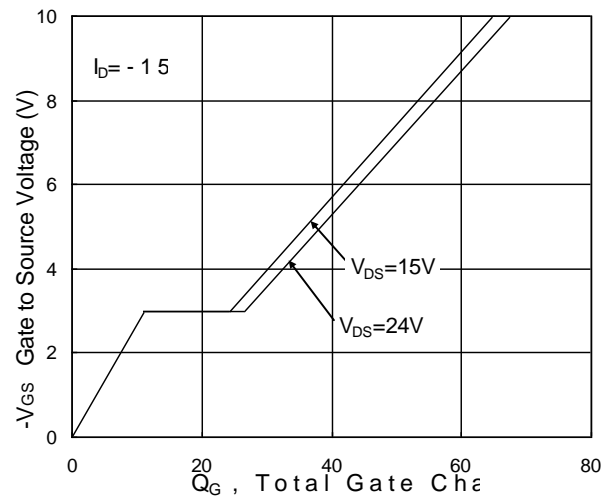
**Fig.1 Typical Output Characteristics**



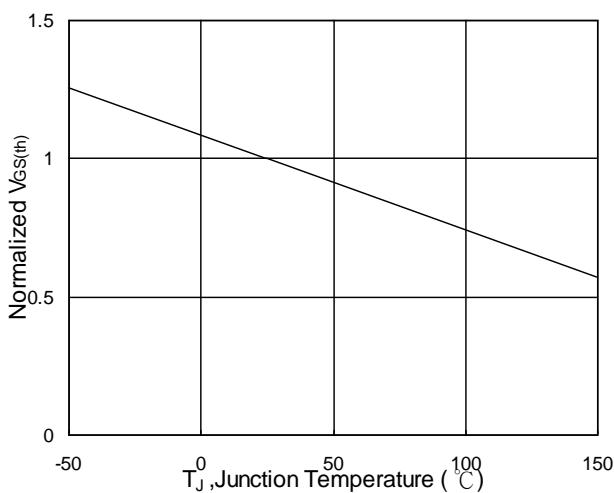
**Fig.2 On-Resistance v.s Gate-Source**



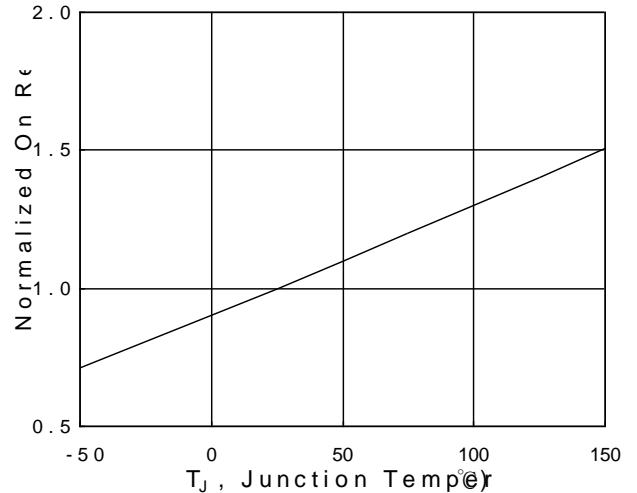
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized V<sub>GS(th)</sub> v.s T<sub>J</sub>**



**Fig.6 Normalized R<sub>DS(on)</sub> v.s T<sub>J</sub>**

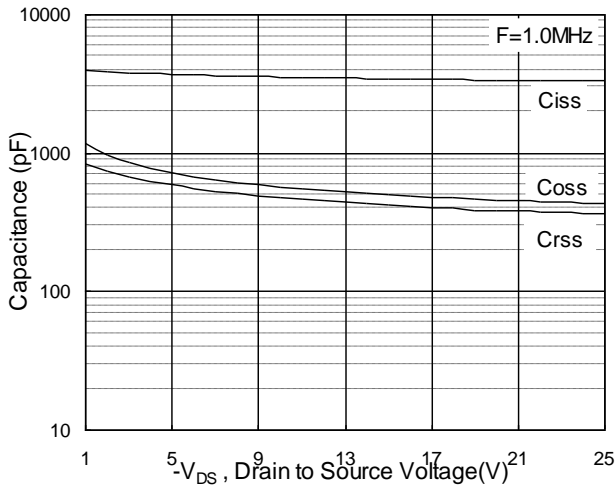


Fig.7 Capacitance

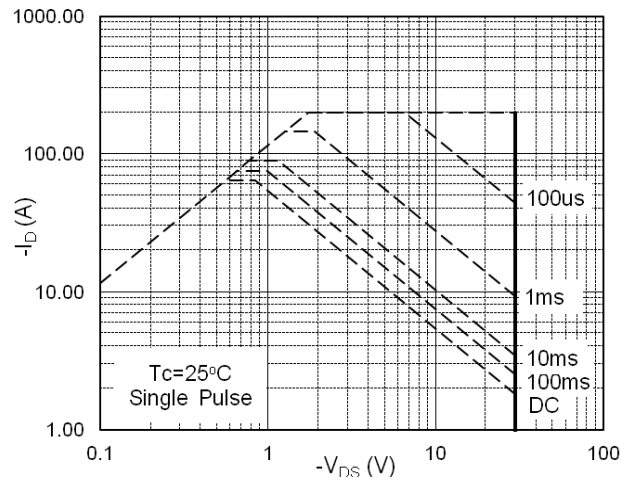


Fig.8 Safe Operating Area

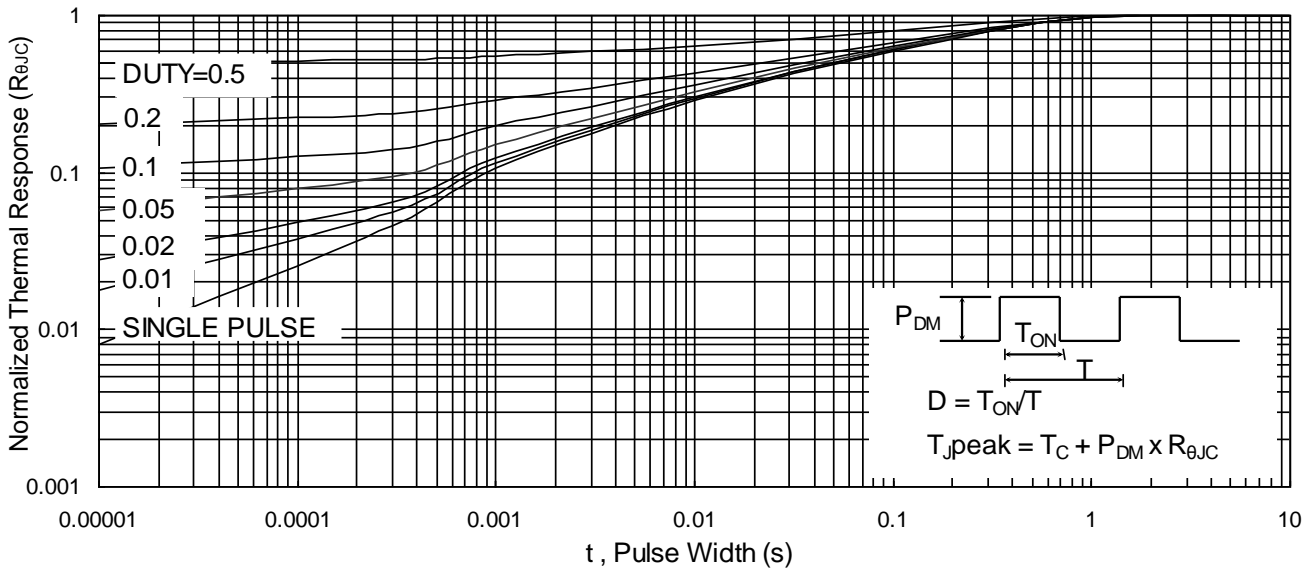


Fig.9 Normalized Maximum Transient Thermal Impedance

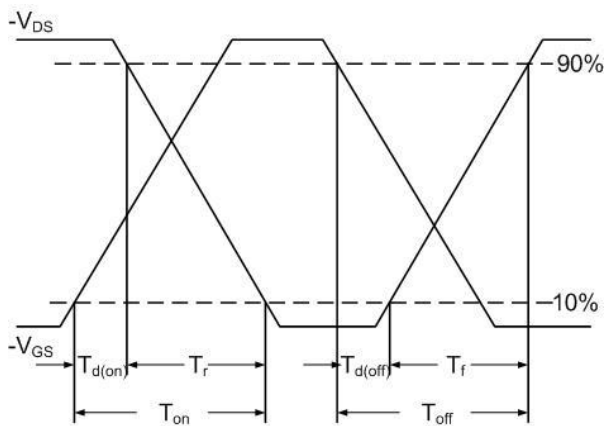


Fig.10 Switching Time Waveform

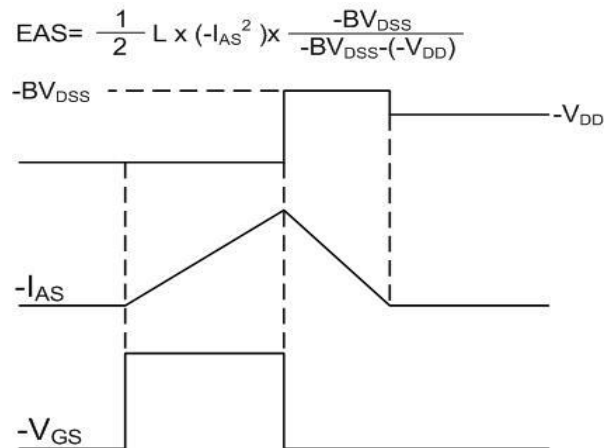


Fig.11 Unclamped Inductive Switching Waveform