

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

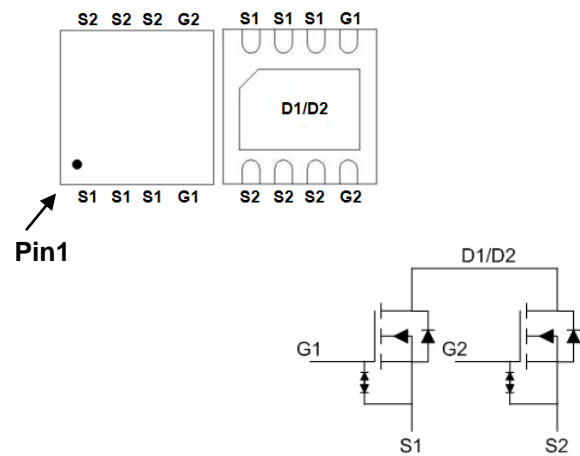
**Product Summary**


BVDSS	RDSON	ID
12V	5.2mΩ	56A

**General Description**

The FKCA1030 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The FKCA1030 meet the RoHS and Green Product requirement with full function reliability approved.

**DFN3x3 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	12	V
$V_{GS}$	Gate-Source Voltage	$\pm 8$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	56	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	35.6	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	19	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	15	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	100	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>1</sup>	31	W
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>1</sup>	3.6	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	35	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	4	$^\circ C/W$



**N-Channel Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	12	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A	---	4.2	5.2	mΩ
		V <sub>GS</sub> =3.9V, I <sub>D</sub> =3A	---	4.3	6.5	
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =3A	---	5	7	
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =3A	---	7	11	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	0.4	---	1.0	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =12V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =12V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±8V, V <sub>DS</sub> =0V	---	---	±10	uA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =3A	---	42	---	S
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =10V, I <sub>D</sub> =3A	---	38	---	nC
	Total Gate Charge (3.9V)		---	33	---	
Q <sub>gs</sub>	Gate-Source Charge		---	4.5	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	12	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =10V, V <sub>GS</sub> =4.5V, R <sub>G</sub> =6Ω I <sub>D</sub> =3A	---	22	---	ns
T <sub>r</sub>	Rise Time		---	41	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	77	---	
T <sub>f</sub>	Fall Time		---	21	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHz	---	3165	---	pF
C <sub>oss</sub>	Output Capacitance		---	380	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	325	---	

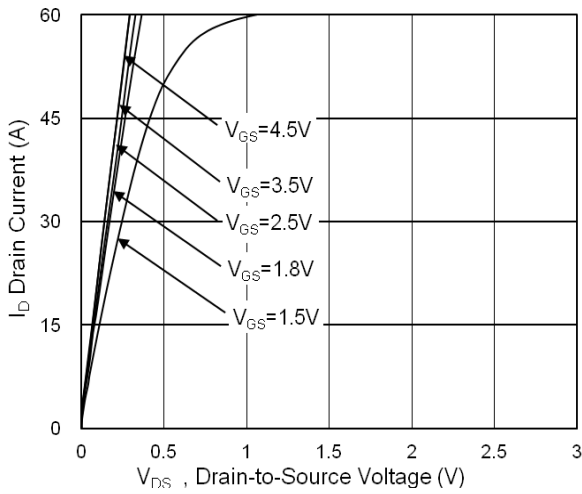
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	30	A
I <sub>SM</sub>	Pulsed Source Current <sup>2</sup>		---	---	100	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =3A, T <sub>J</sub> =25°C	---	---	1.2	V

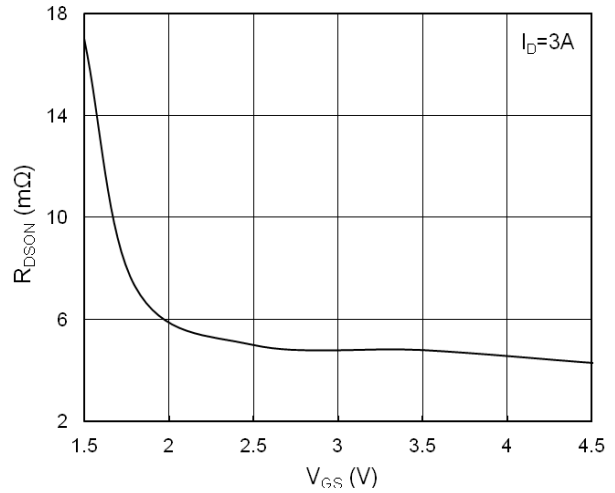
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper, t ≤10s.
- 2.The data tested by pulsed , pulse width ≤ 10us , duty cycle ≤ 1%

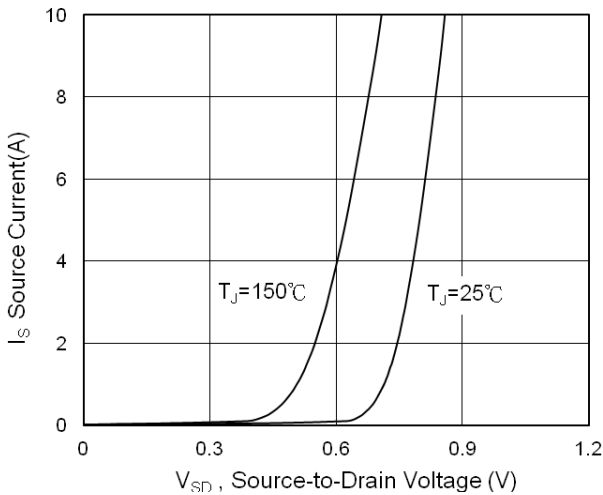
### Typical Characteristics



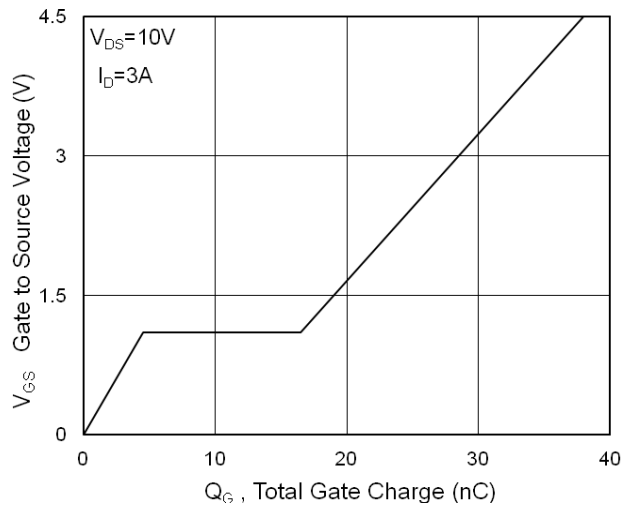
**Fig.1 Typical Output Characteristics**



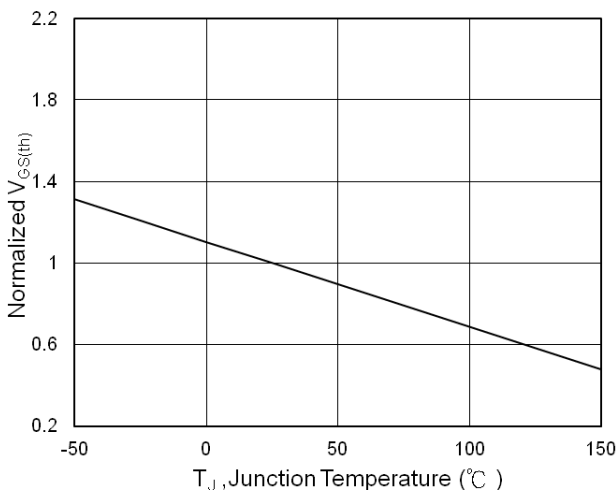
**Fig.2 On-Resistance vs. Gate-Source Voltage**



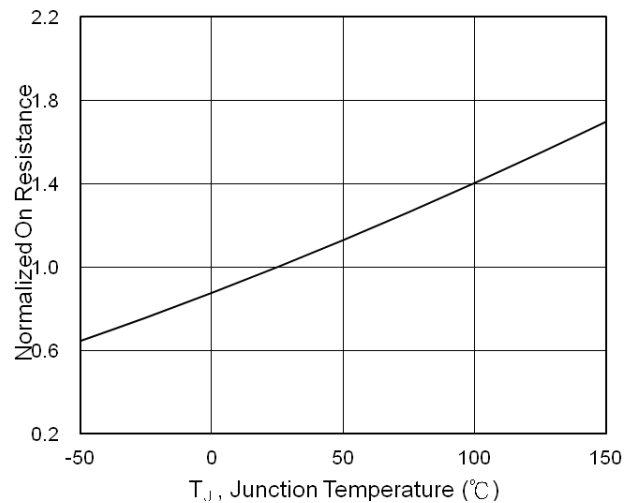
**Fig.3 Forward Characteristics of Reverse**



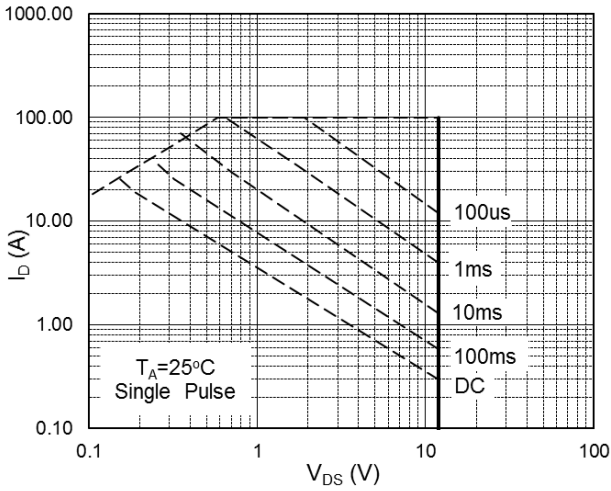
**Fig.4 Gate-Charge Characteristics**



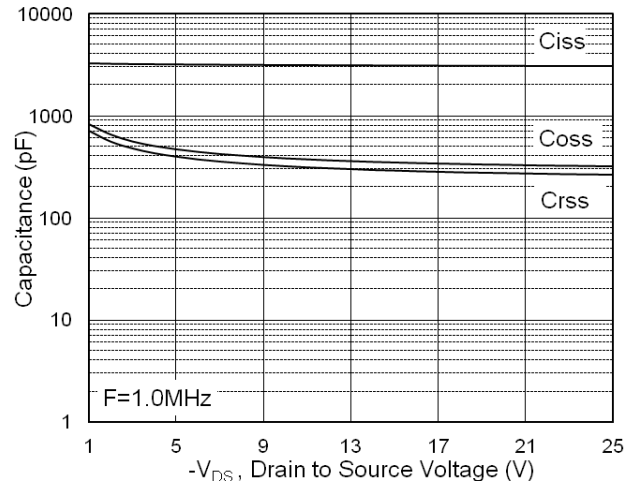
**Fig.5  $V_{GS(th)}$  vs.  $T_J$**



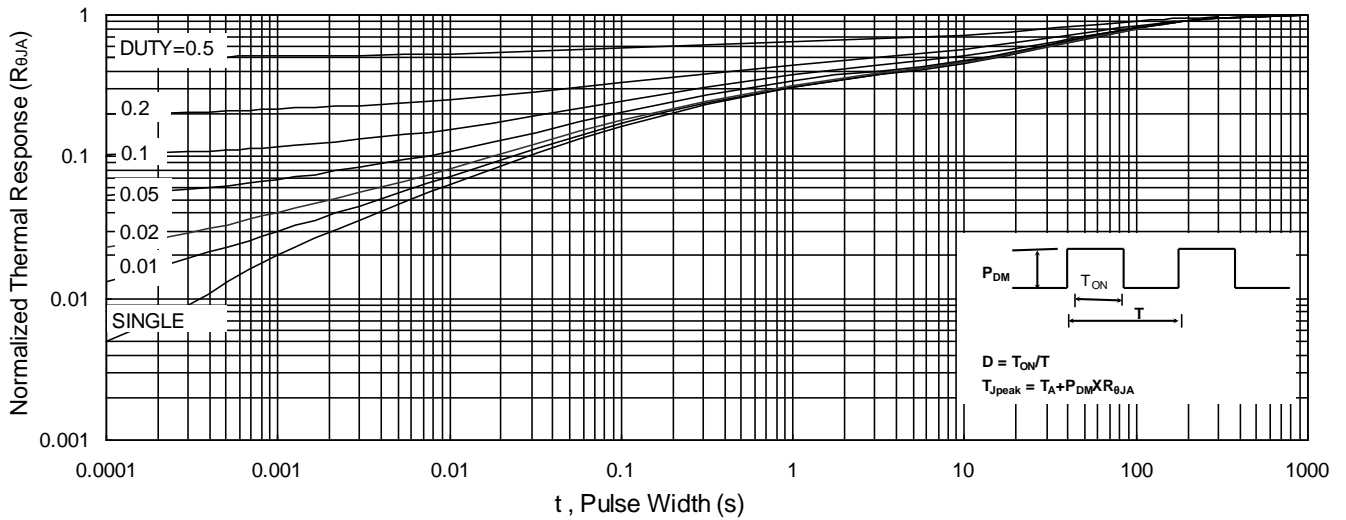
**Fig.6 Normalized  $R_{DSON}$  vs.  $T_J$**



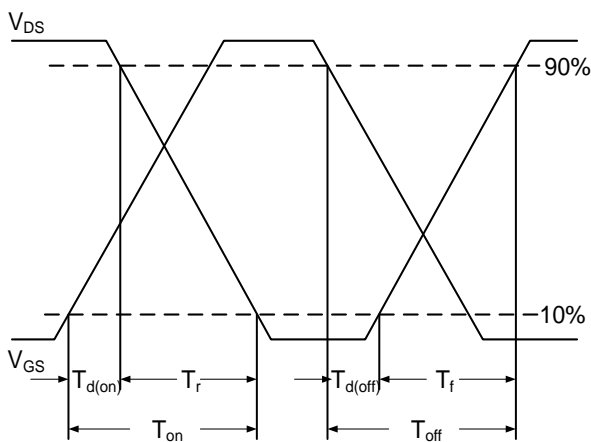
**Fig.7 Safe Operating Area**



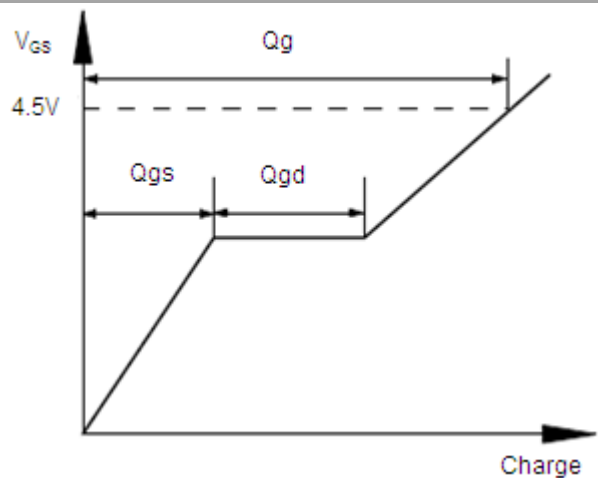
**Fig.8 Capacitance**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**