

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

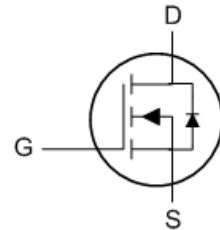
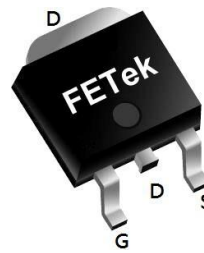
Product Summary


BVDSS	RDSON	ID
100V	66mΩ	14A

Description

The FKD0028 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKD0028 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	14	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	10	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	4	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3	A
I_{DM}	Pulsed Drain Current ²	25	A
EAS	Single Pulse Avalanche Energy ³	0.8	mJ
I_{AS}	Avalanche Current	4	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	30	W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	2.7	W
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 175	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	55	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	5	$^\circ C/W$

**Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=5A$	---	---	66	m Ω
		$V_{GS}=4.5V, I_D=3A$	---	---	85	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.5	---	2.9	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	10	μA
		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=5A$	---	14	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	3	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=50V, V_{GS}=10V, I_D=5A$	---	11.9	---	nC
Q_{gs}	Gate-Source Charge		---	2.6	---	
Q_{gd}	Gate-Drain Charge		---	1.7	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V, V_{GS}=10V, R_G=3\Omega, I_D=5A$	---	3.8	---	ns
T_r	Rise Time		---	25.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	16	---	
T_f	Fall Time		---	8.8	---	
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$	---	620	---	pF
C_{oss}	Output Capacitance		---	105	---	
C_{rss}	Reverse Transfer Capacitance		---	63	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	14	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	25	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=5A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	30	---	nS
Q_{rr}	Reverse Recovery Charge		---	37	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=4A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

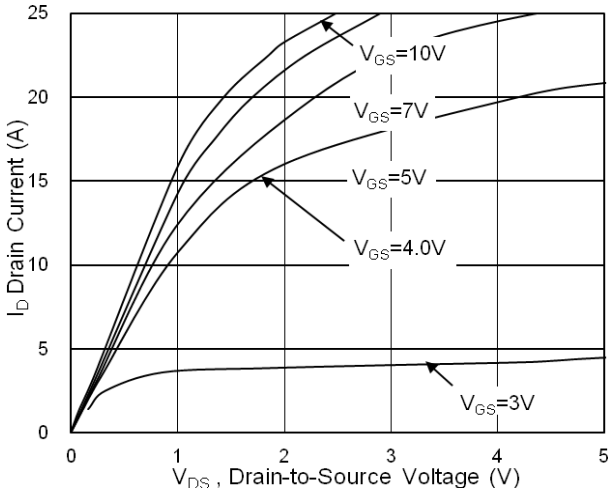


Fig.1 Typical Output Characteristics

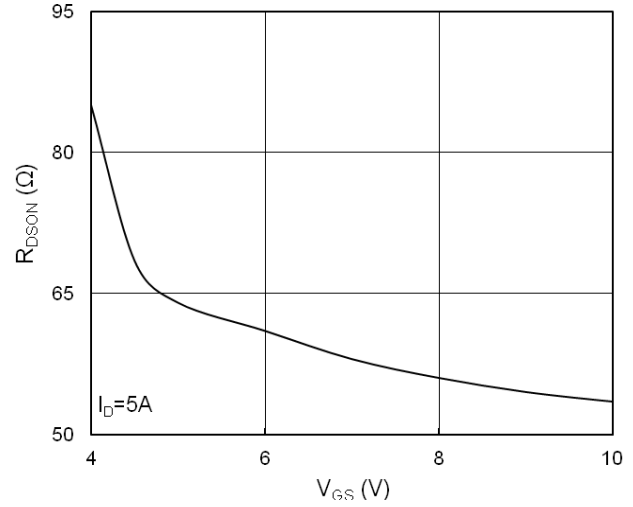


Fig.2 On-Resistance v.s Gate-Source

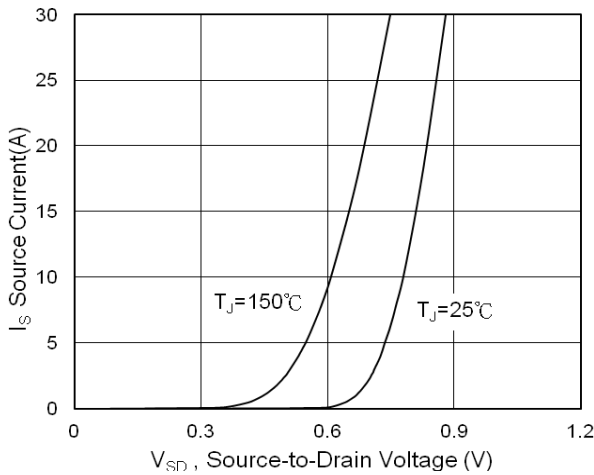


Fig.3 Forward Characteristics Of Reverse

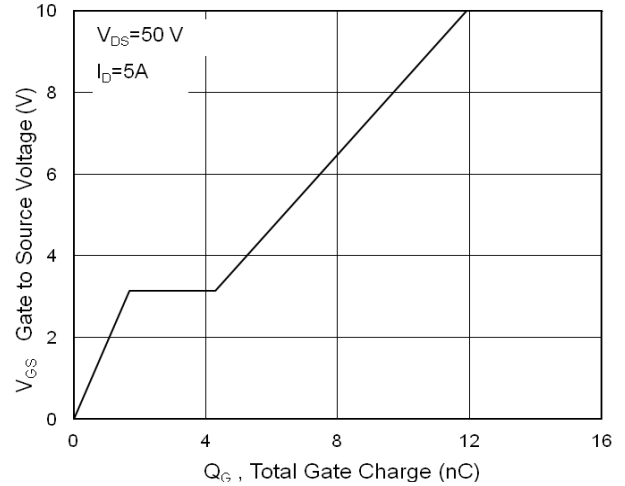


Fig.4 Gate-Charge Characteristics

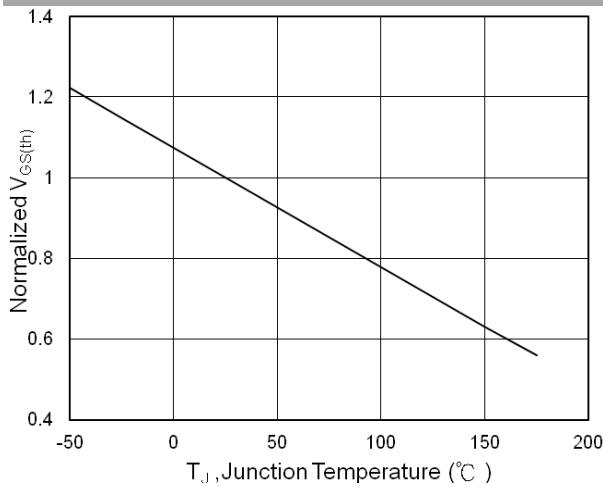


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

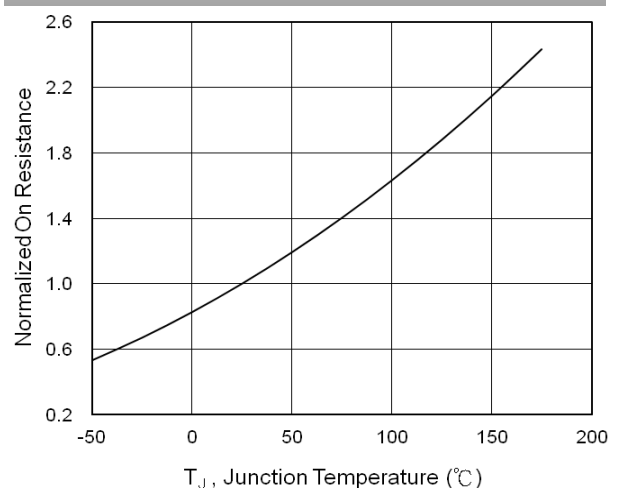


Fig.6 Normalized R_{DSON} v.s T_J

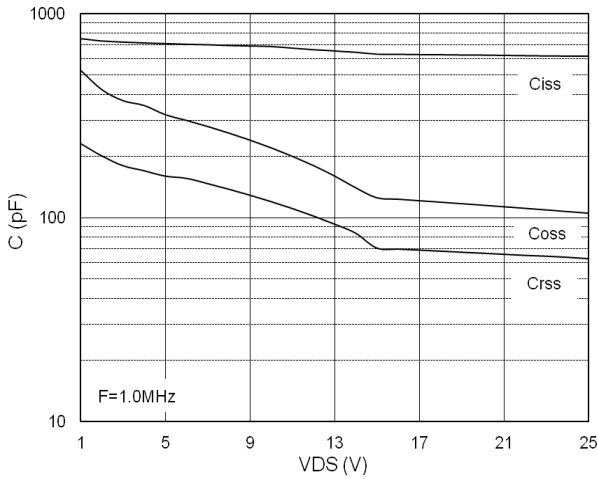


Fig.7 Capacitance

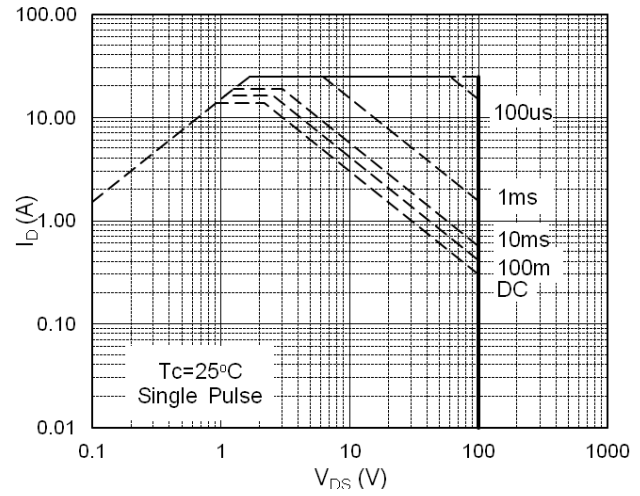


Fig.8 Safe Operating Area

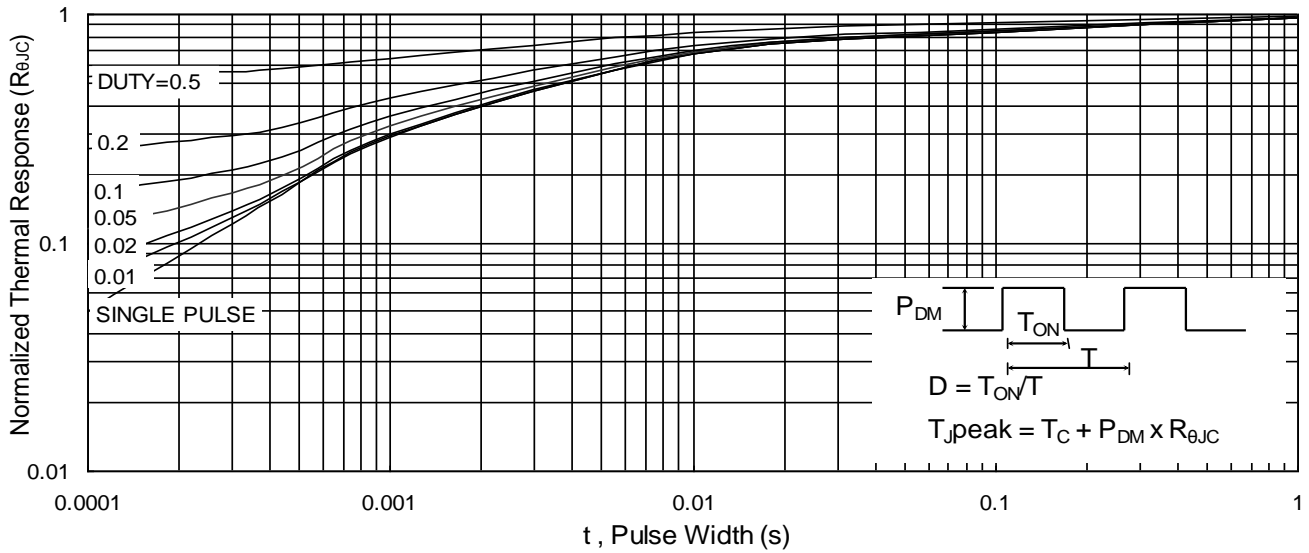


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform



Fig.11 Unclamped Inductive Switching Waveform