



- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

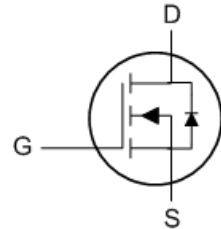
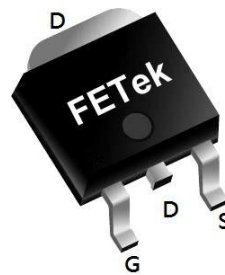
Product Summary

BVDSS	R _{DS(on)}	I _D
150V	88mΩ	20A

Description

The FKD20N15 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The FKD20N15 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	150	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	20	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	14	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	3	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	2.5	A
I _{DM}	Pulsed Drain Current ²	40	A
EAS	Single Pulse Avalanche Energy ³	53	mJ
I _{AS}	Avalanche Current	18	A
P _D @T _C =25°C	Total Power Dissipation ³	72.6	W
P _D @T _A =25°C	Total Power Dissipation ³	2.1	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	60	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.72	°C/W

**Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	150	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=10A$	---	---	88	m Ω
	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=10A$	---	---	100	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=120V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=120V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=10A$	---	33	---	S
Q_g	Total Gate Charge	$V_{DS}=75V, V_{GS}=4.5V, I_D=10A$	---	25.1	---	nC
Q_{gs}	Gate-Source Charge		---	6.8	---	
Q_{gd}	Gate-Drain Charge		---	12.6	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=75V, V_{GS}=10V, R_G=3.3\Omega, I_D=10A$	---	13	---	ns
T_r	Rise Time		---	8.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	25	---	
T_f	Fall Time		---	11	---	
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$	---	2285	---	pF
C_{oss}	Output Capacitance		---	110	---	
C_{rss}	Reverse Transfer Capacitance		---	83	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	20	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	40	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=10A, di/dt=100A/\mu s,$	---	37	---	nS
Q_{rr}	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	263	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.3mH, I_{AS}=18A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

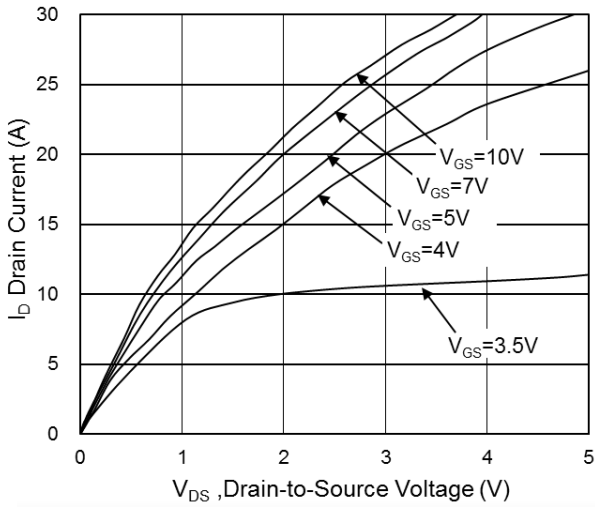


Fig.1 Typical Output Characteristics

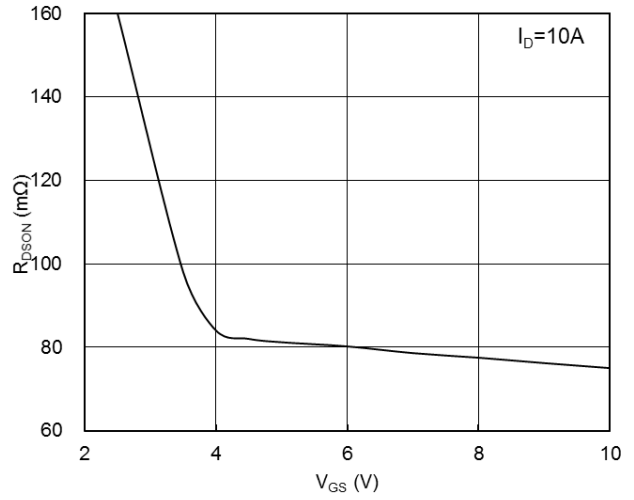


Fig.2 On-Resistance vs. Gate-Source Voltage

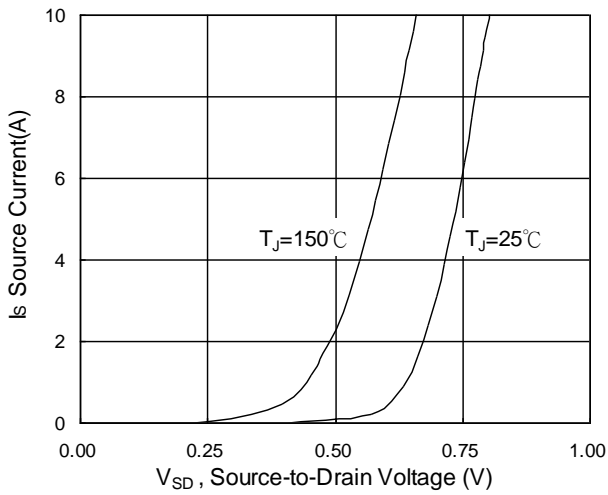


Fig.3 Forward Characteristics of Reverse

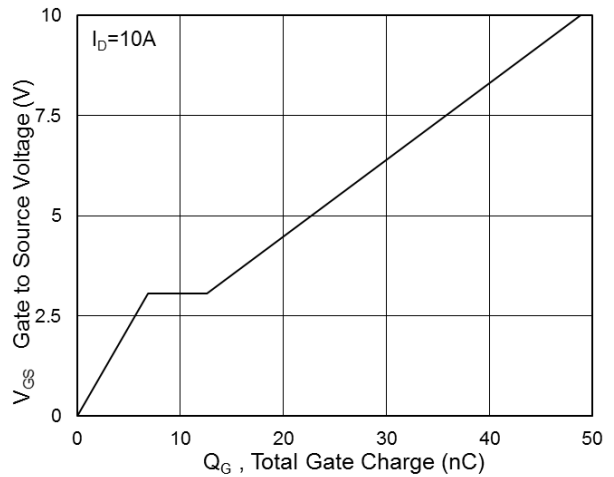


Fig.4 Gate-Charge Characteristics

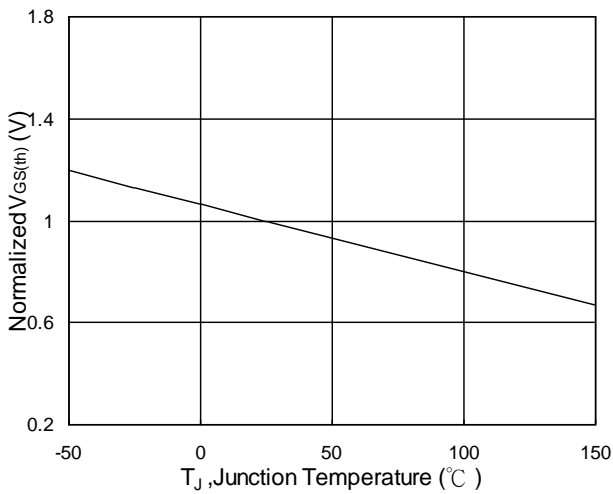


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

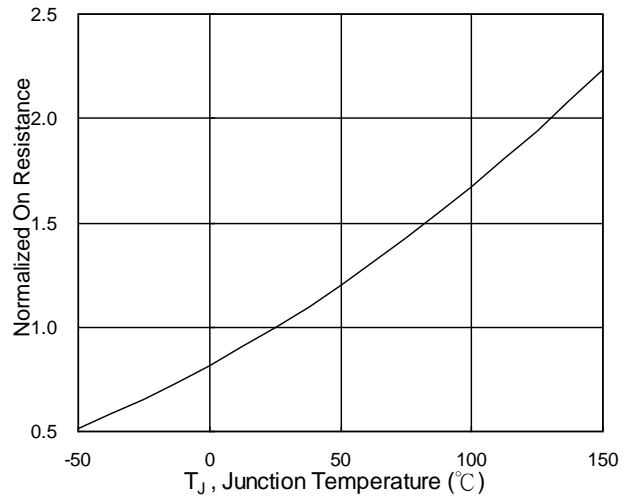


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

N-Ch 150V Fast Switching MOSFETs

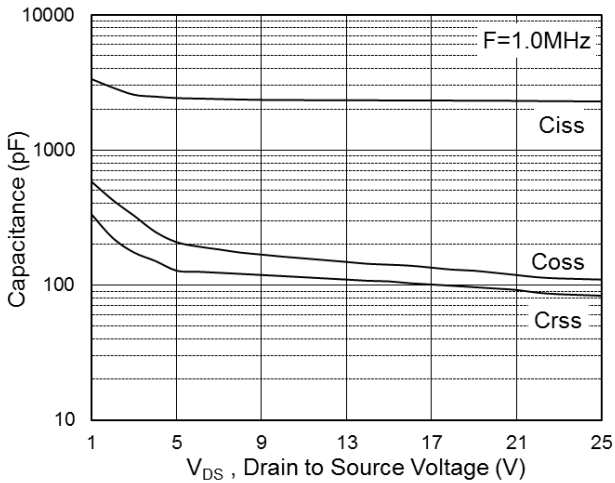


Fig.7 Capacitance

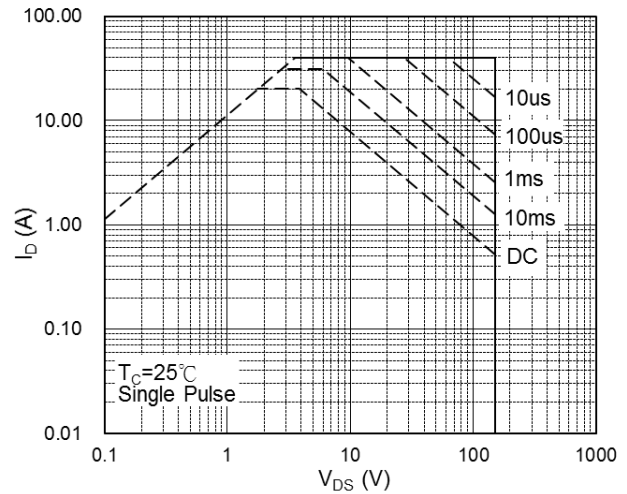


Fig.8 Safe Operating Area

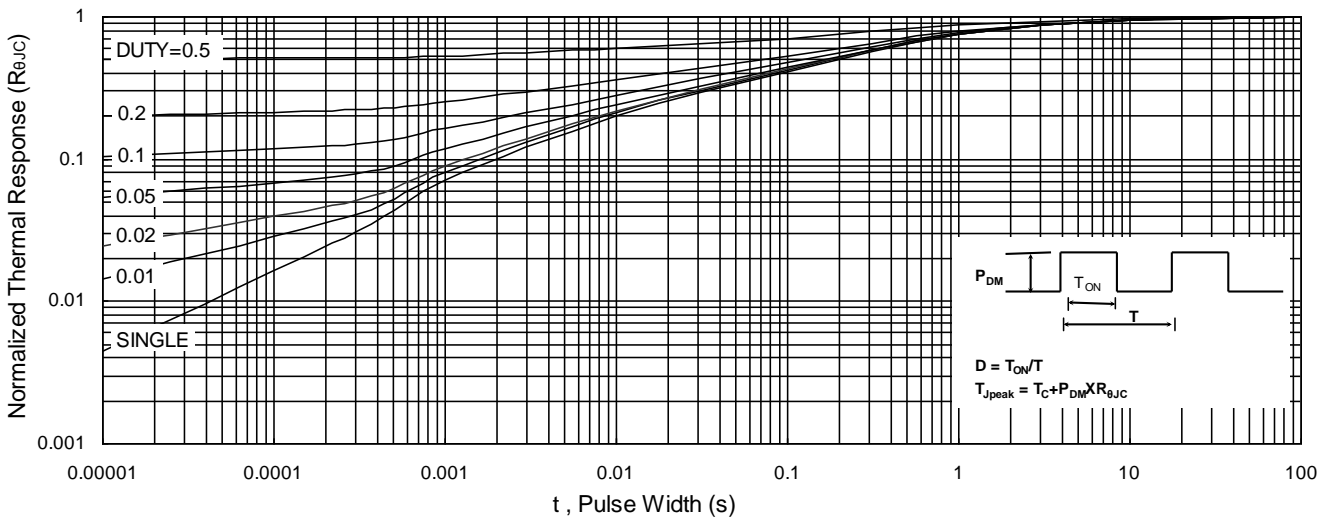


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform



Fig.11 Unclamped Inductive Switching Waveform