

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

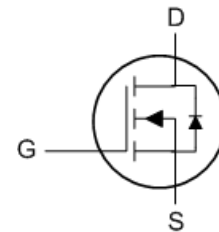
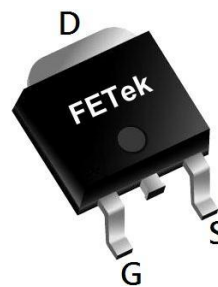
Product Summary


BVDSS	R _{DS(on)}	I _D
80V	100mΩ	11.8A

Description

The FKD8014 is the high cell density trenched N-ch MOSFETs, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The FKD8014 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	80	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	11.8	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	7.5	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	3	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	2.4	A
I _{DM}	Pulsed Drain Current ²	25	A
EAS	Single Pulse Avalanche Energy ³	15.5	mJ
I _{AS}	Avalanche Current	17.6	A
P _D @T _C =25°C	Total Power Dissipation ⁴	31.3	W
P _D @T _A =25°C	Total Power Dissipation ⁴	2.02	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	4	°C/W

**Electrical Characteristics (T_J=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	80	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.072	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =10A	---	---	100	mΩ
		V _{GS} =4.5V, I _D =8A	---	---	115	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	---	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4.7	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =64V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =64V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =10A	---	14.7	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.8	---	Ω
Q _g	Total Gate Charge (10V)	V _{DS} =64V, V _{GS} =10V, I _D =10A	---	18.6	---	nC
Q _{gs}	Gate-Source Charge		---	3.9	---	
Q _{gd}	Gate-Drain Charge		---	3.2	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =40V, V _{GS} =10V, R _G =3.3Ω, I _D =10A	---	5	---	ns
T _r	Rise Time		---	25	---	
T _{d(off)}	Turn-Off Delay Time		---	21	---	
T _f	Fall Time		---	7.6	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1090	---	pF
C _{oss}	Output Capacitance		---	60	---	
C _{rss}	Reverse Transfer Capacitance		---	41	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	11.8	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	25	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =10A, dI/dt=100A/μs, T _J =25°C	---	18.6	---	nS
Q _{rr}	Reverse Recovery Charge		---	17.7	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=17.6A
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

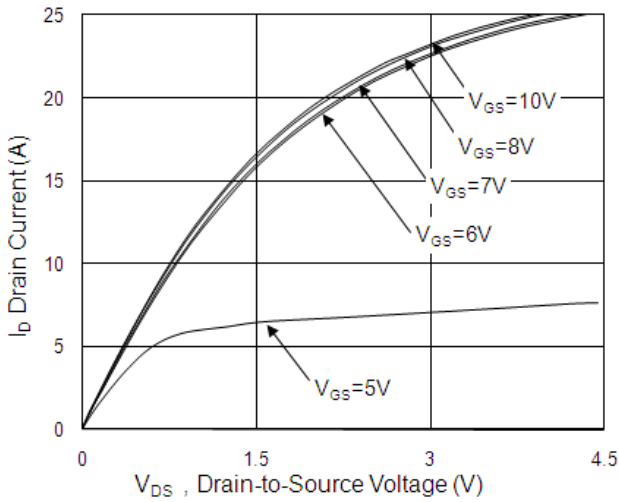


Fig.1 Typical Output Characteristics

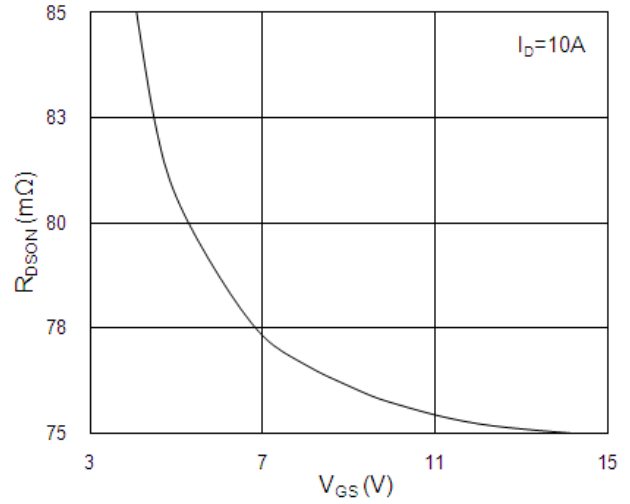


Fig.2 On-Resistance v.s Gate-Source

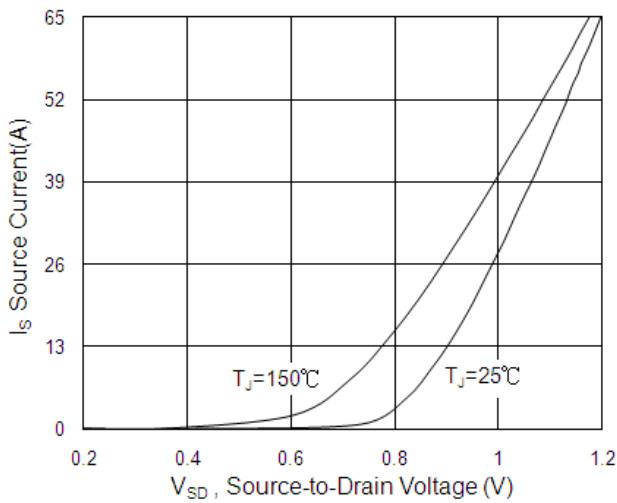


Fig.3 Forward Characteristics of Reverse

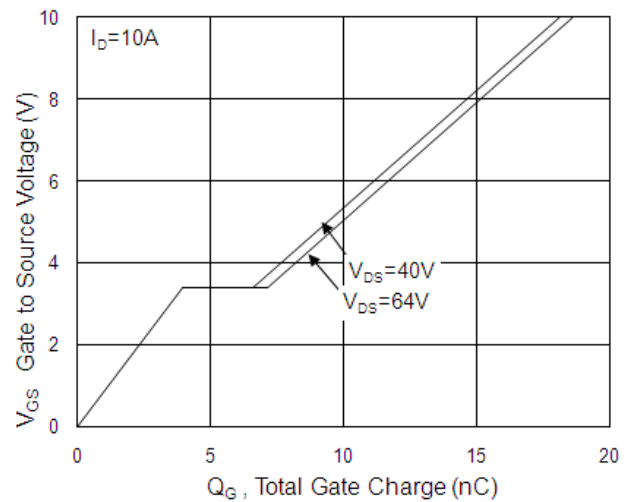


Fig.4 Gate-Charge Characteristics

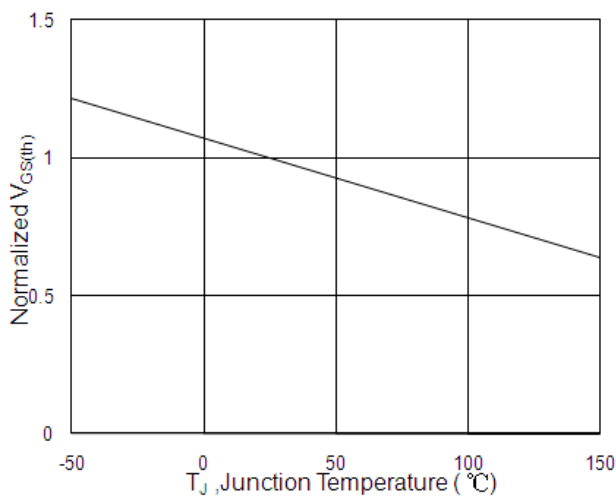


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

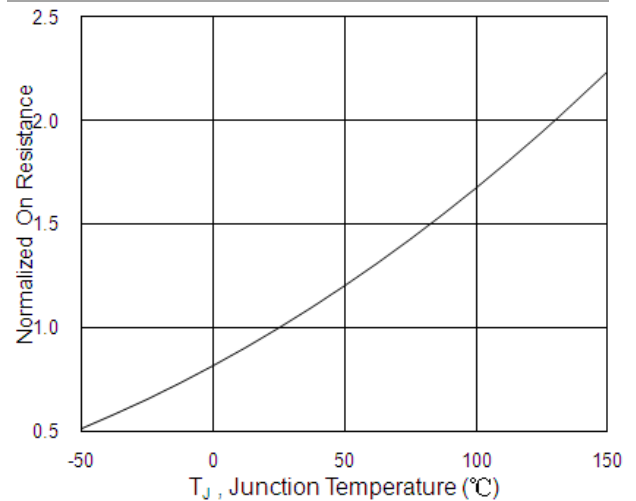


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

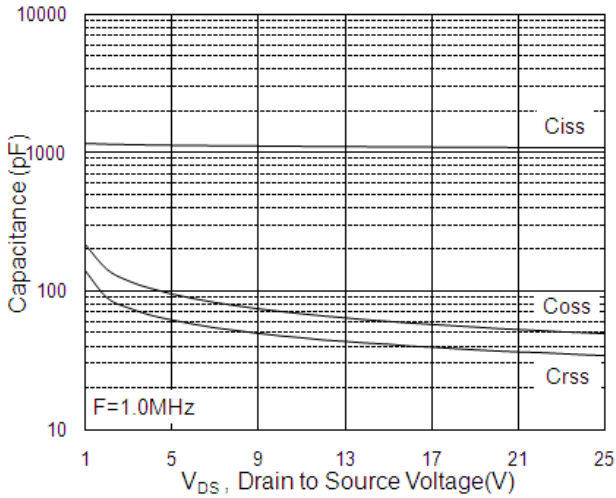


Fig.7 Capacitance

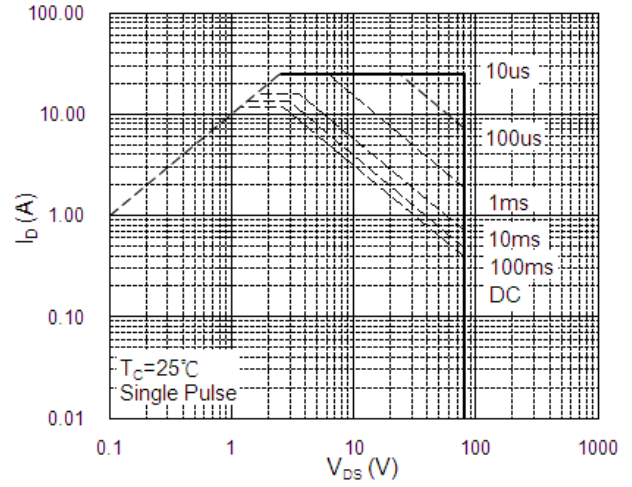


Fig.8 Safe Operating Area

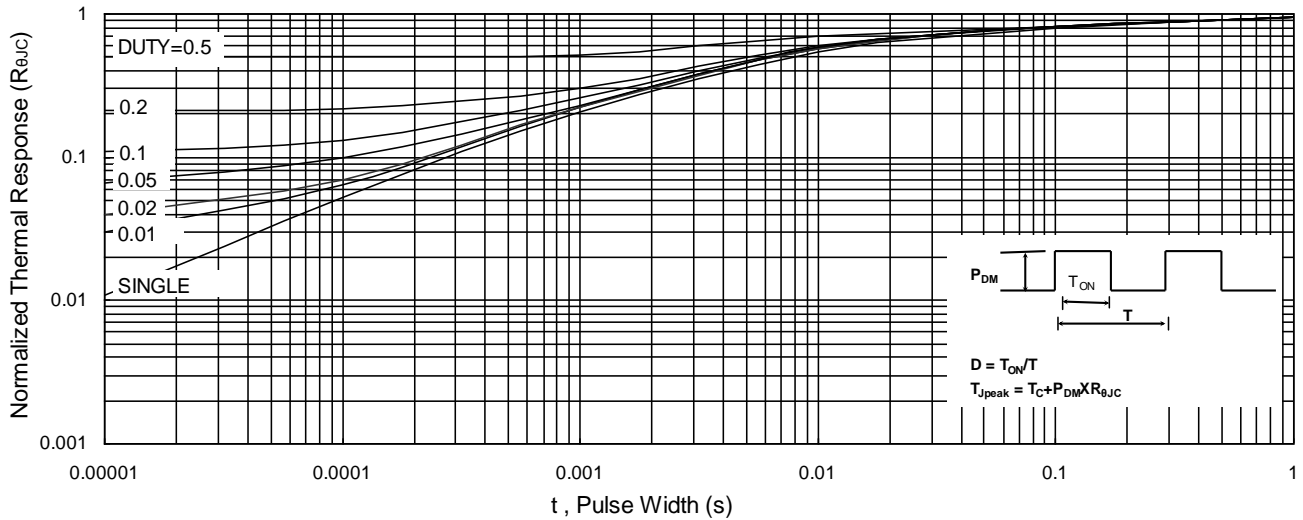


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform



Fig.11 Unclamped Inductive Switching Waveform