

- Green Device Available
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology

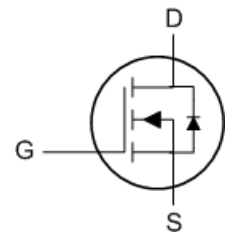
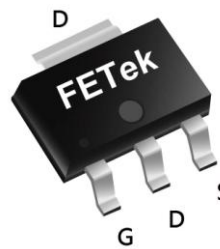
Product Summary


BVDSS	RDSON	ID
100V	47mΩ	6A

Description

The FKL0016 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKL0016 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

SOT223 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.7	A
I_{DM}	Pulsed Drain Current ²	24	A
EAS	Single Pulse Avalanche Energy ³	11.3	mJ
I_{AS}	Avalanche Current	15	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹ (Steady State)	---	70	$^\circ\text{C/W}$
	Thermal Resistance Junction-ambient ¹ ($t \leq 10s$)	---	35	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.098	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=5A$	---	---	47	m Ω
		$V_{GS}=4.5V, I_D=5A$	---	---	50	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.52	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	10	μA
		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=5A$	---	6.2	---	S
Q_g	Total Gate Charge (10V)	$V_{DS}=80V, V_{GS}=10V, I_D=5A$	---	60	---	nC
Q_{gs}	Gate-Source Charge		---	9.2	---	
Q_{gd}	Gate-Drain Charge		---	9.9	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=3A$	---	10.8	---	ns
T_r	Rise Time		---	27	---	
$T_{d(off)}$	Turn-Off Delay Time		---	56	---	
T_f	Fall Time		---	24	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	3848	---	pF
C_{oss}	Output Capacitance		---	137	---	
C_{riss}	Reverse Transfer Capacitance		---	82	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	6	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	24	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=5A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	25	---	nS
Q_{rr}	Reverse Recovery Charge		---	29	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=15A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

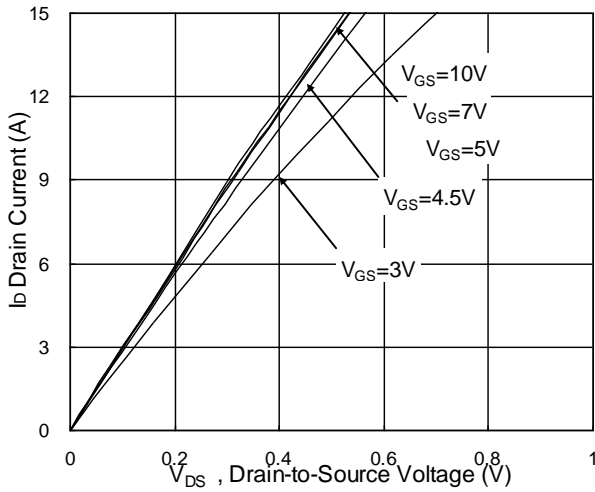


Fig.1 Typical Output Characteristics

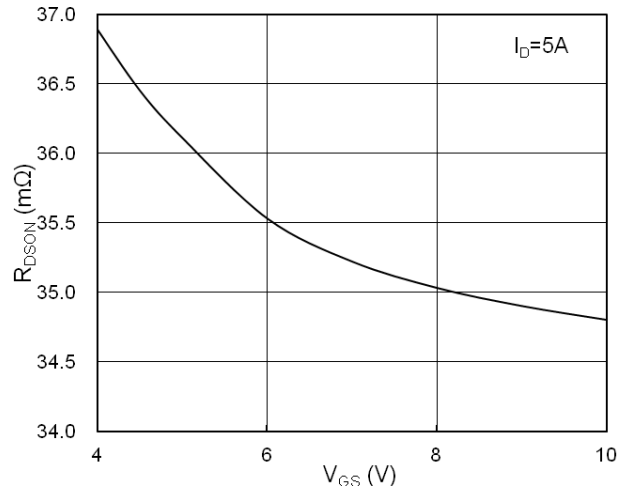


Fig.2 On-Resistance vs. Gate-Source

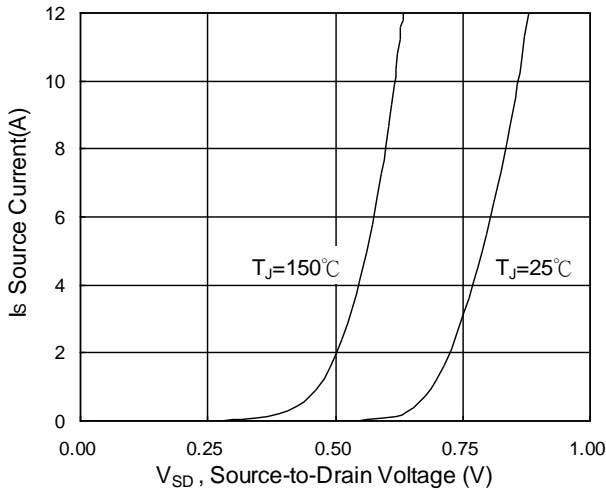


Fig.3 Forward Characteristics Of Reverse

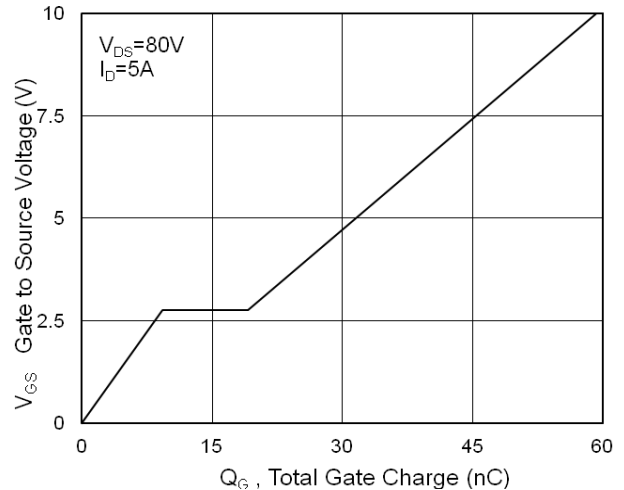


Fig.4 Gate-Charge Characteristics

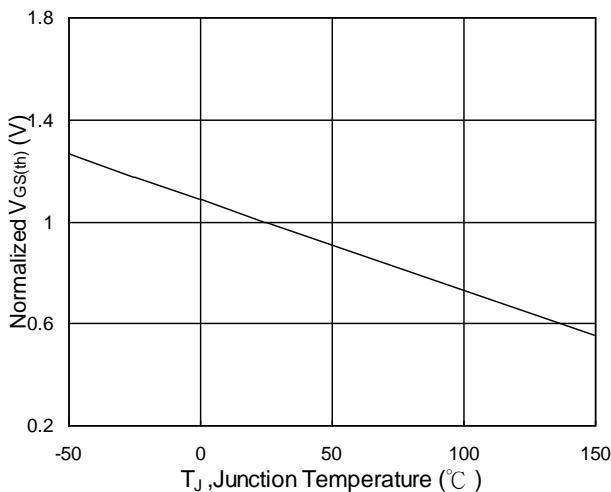


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

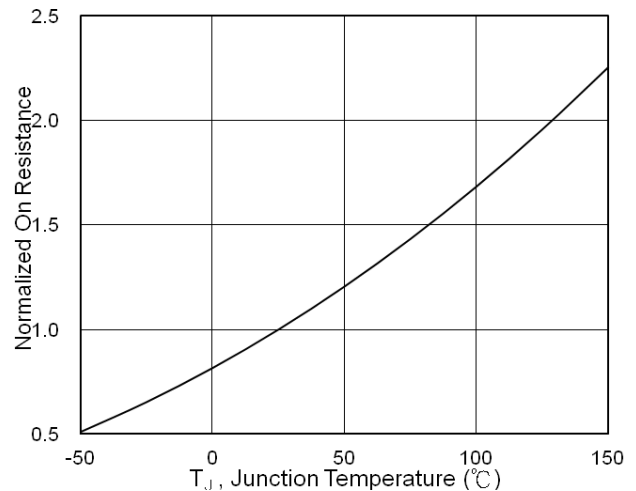


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

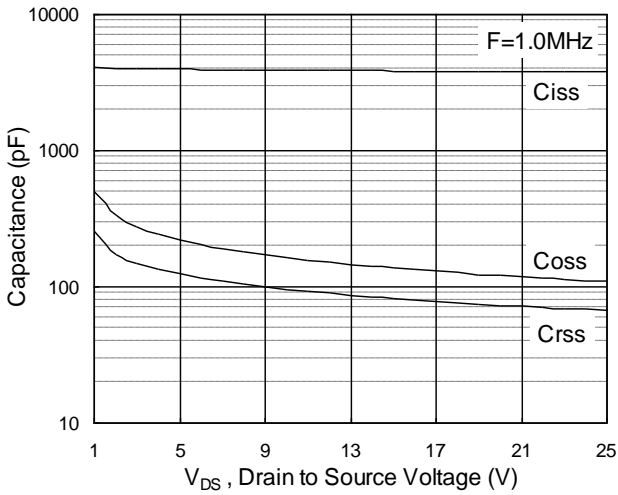


Fig.7 Capacitance

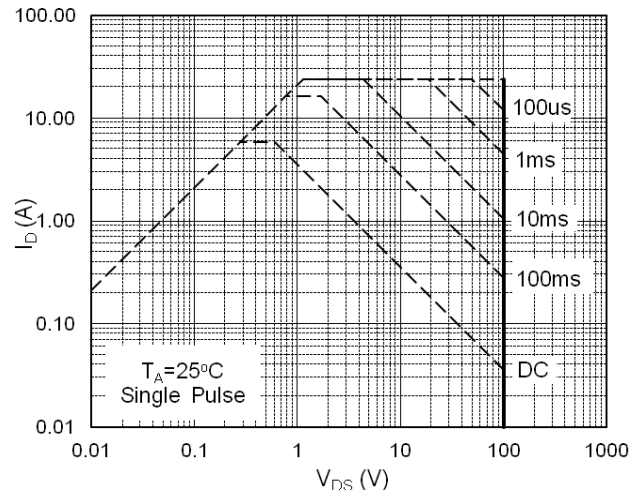


Fig.8 Safe Operating Area

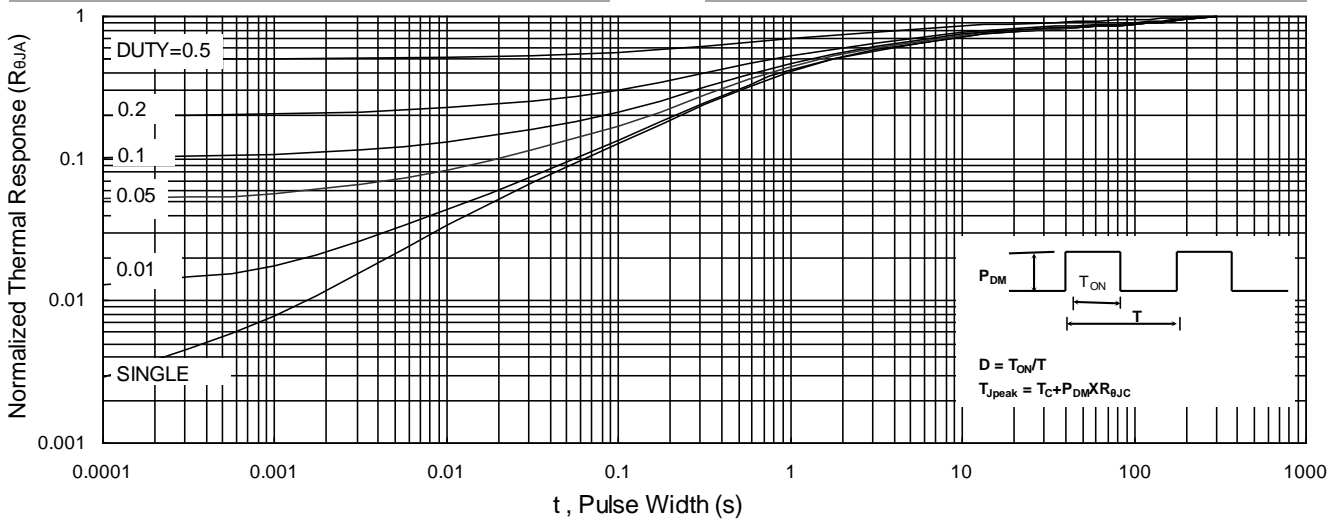


Fig.9 Normalized Maximum Transient Thermal Impedance

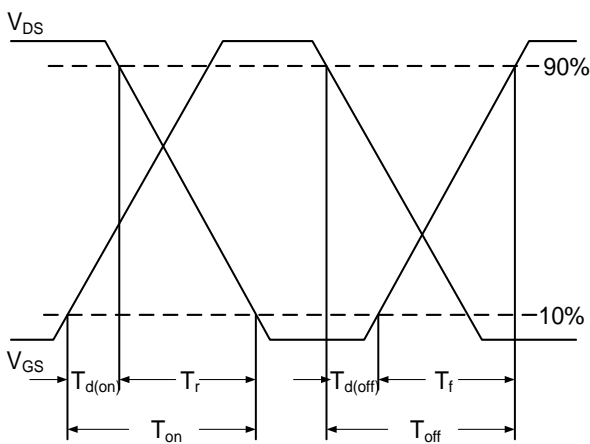


Fig.10 Switching Time Waveform

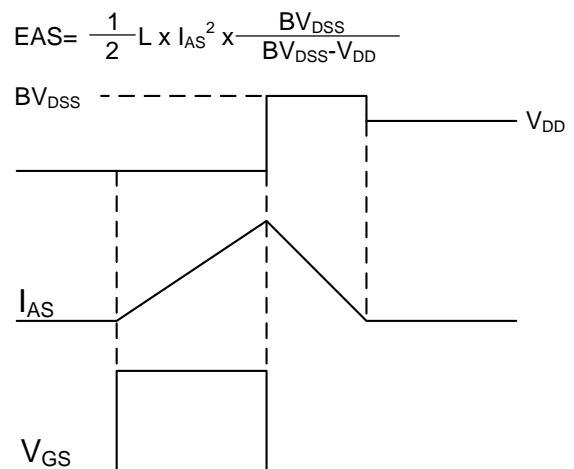


Fig.11 Unclamped Inductive Switching Waveform