



- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

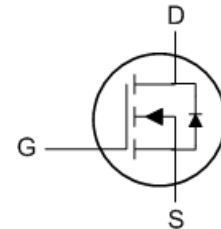
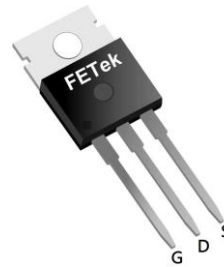
**Product Summary**

BVDSS	RDSON	ID
100V	152mΩ	11.8 A

**Description**

The FKP0014 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKP0014 meet the RoHS and Green Product requirement with full function reliability approved.

**TO220 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	11.8	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	7.4	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	24	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>3</sup>	52.1	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	2.4	$^\circ C/W$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	---	0.122	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=8A$	---	---	152	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=6A$	---	---	158	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.84	---	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	10	$\mu A$
		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	100	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=8A$	---	10.2	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2.3	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DS}=60V, V_{GS}=10V, I_D=8A$	---	25.5	---	nC
$Q_{gs}$	Gate-Source Charge		---	4.2	---	
$Q_{gd}$	Gate-Drain Charge		---	4.3	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V, V_{GS}=10V, R_G=3.3\Omega, I_D=1A$	---	17.3	---	ns
$T_r$	Rise Time		---	2.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	50	---	
$T_f$	Fall Time		---	2.8	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	1077	---	pF
$C_{oss}$	Output Capacitance		---	46	---	
$C_{rss}$	Reverse Transfer Capacitance		---	32	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	11.8	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=8A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	30	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	16	---	nC

## Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

Typical Characteristics

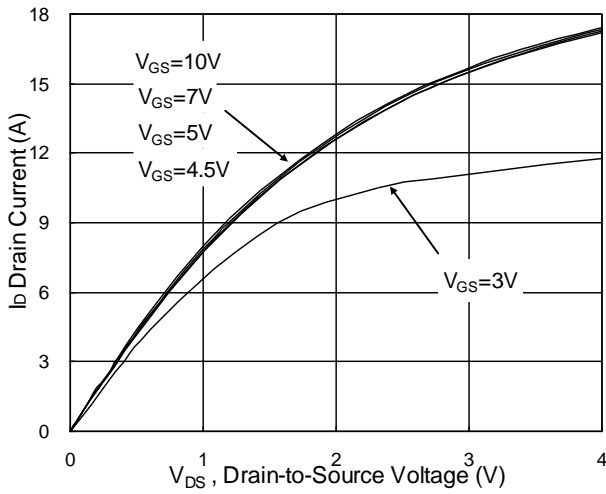


Fig.1 Typical Output Characteristics

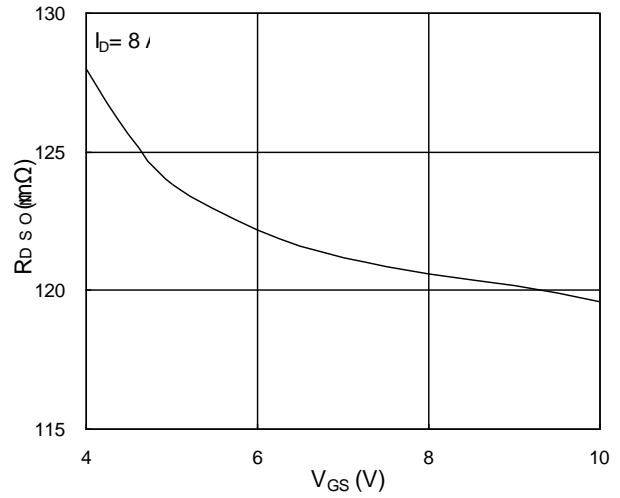


Fig.2 On-Resistance vs. Gate-Source

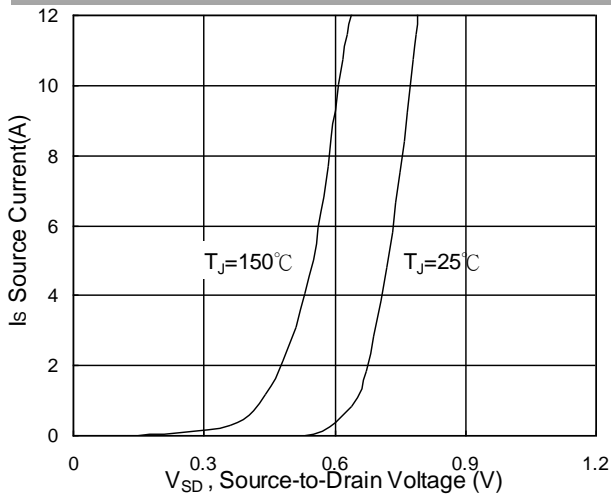


Fig.3 Forward Characteristics Of Reverse

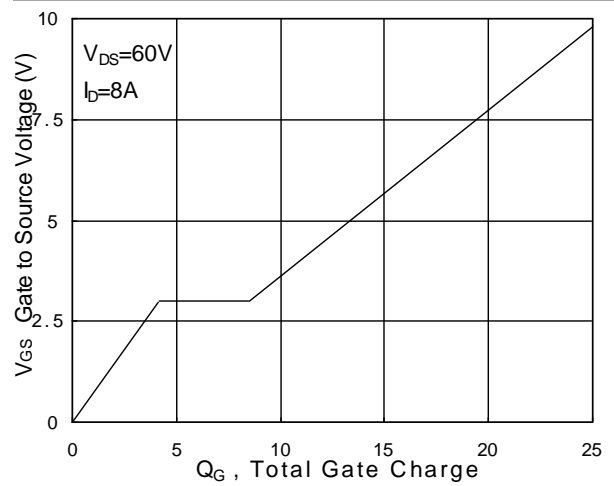


Fig.4 Gate-Charge Characteristics

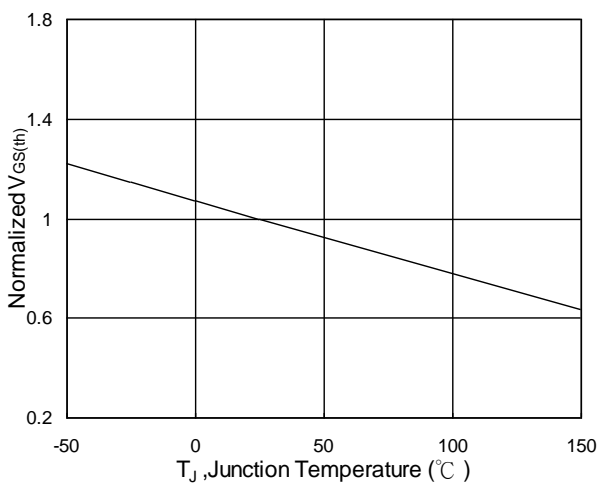


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

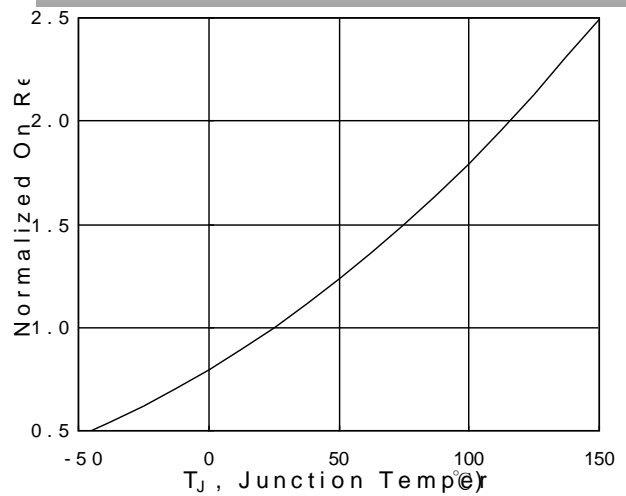


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

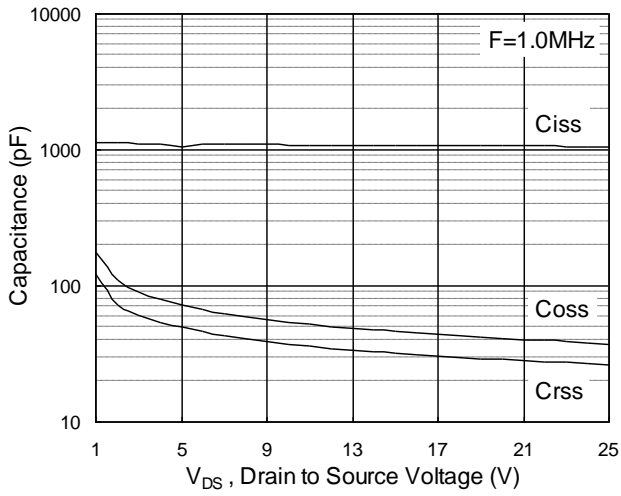


Fig.7 Capacitance

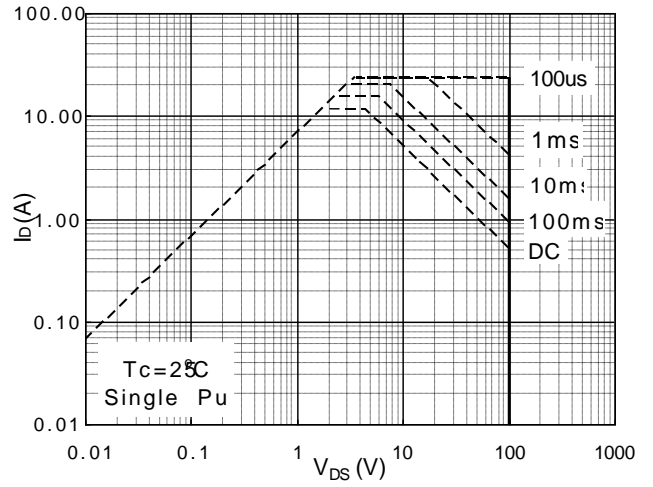


Fig.8 Safe Operating Area

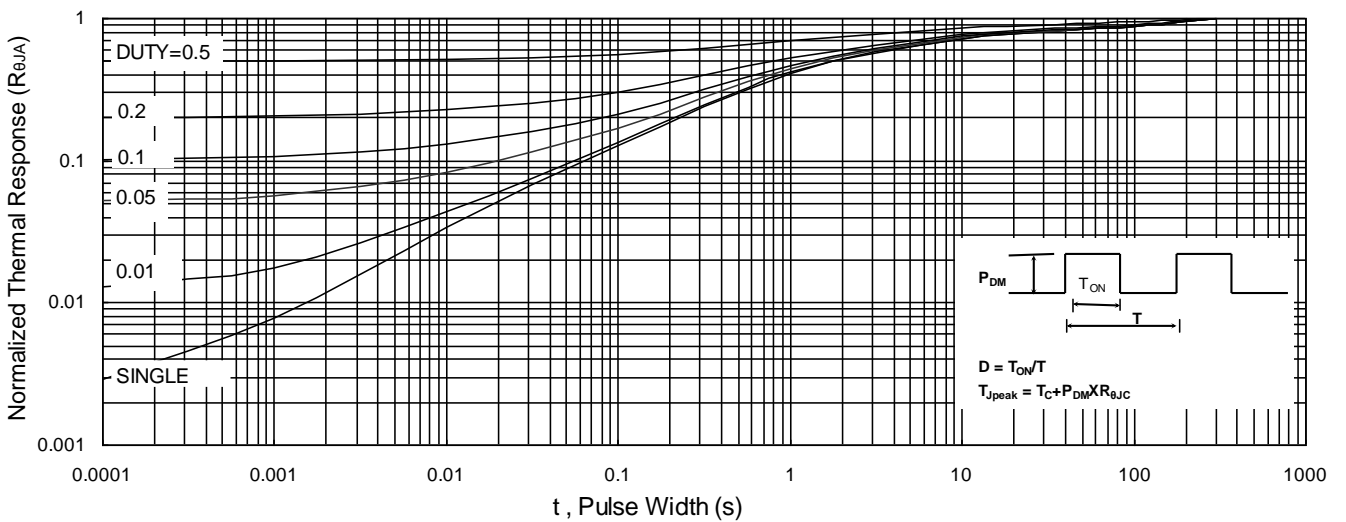


Fig.9 Normalized Maximum Transient Thermal Impedance

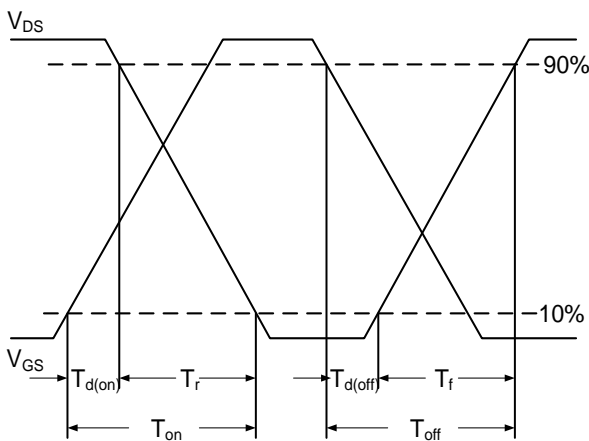


Fig.10 Switching Time Waveform

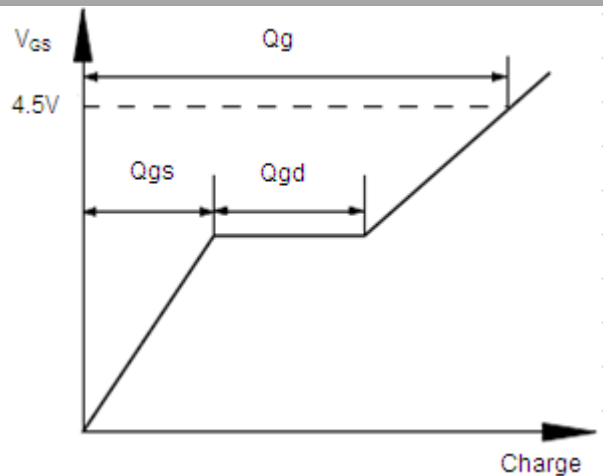


Fig.11 Gate Charge Waveform