FRESCO LOGIC

Product Datasheet

FL1100EX

PCI Express to 4-Port USB 3.0 Host Controller

Revision 1.30

August 2013

Fresco Logic **CONFIDENTIAL**

Revision History

Revision	Date	Comment
0.20	30 Jun 2011	Preliminary release
0.21	10 Jul 2011	Change signal type to LVTTL of following pins: SMIN, ROMSDA, ROMSCL
0.50	31 Oct 2011	Update features Update support ambient temperature Add Chapter 5 PCI Express Registers Update pins: NC: B16, B39, A47, AVCC12: A6, B10, B43, B50 Update Appendix A: reference footprint
1.00	15 Jan 2012	Update section 4.6: power consumption data Update Appendix A: update reference footprint Update Appendix C: add description in "long" and "hot" thermal profile recommendation. Update section 2.2: add pull up/down to below signals: PREST#, OVCN0-3, ROMSDA, ROMSCL, ROMPRES. Update section 3.6.2: Supplement HW LPM description. Update section 3.2: description of xHCI controller.
1.10	15 Aug 2012	Update Appendix A.1: Update POD from Amkor: exposure pad size change Update Appendix A.2: Update exposure pad footprint
1.20	16 Mar 2013	Updates for B0 Mass Production
1.30	1 Aug 2013	Add TFBGA 161 pin part, combined pins AGND and DGND to GND

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1. Introduction

The FL1100 is Fresco Logic's single-chip PCI Express to USB 3.0 host controller. It fully integrates an Extensible Host Controller Interface (xHCI) engine, a 4-port 5Gbps USB 3.0 transceiver, a PCI Express endpoint controller and a 5Gbps PCI Express transceiver. FL1100 implements the Universal Serial Bus 3.0 Specification Revision 1.0 and the Extensible Host Controller Interface (xHCI) Specification Revision 1.0, and complies with the PCI Express Rev 2.1 Specification at 5Gbps data rate, and is backward compatible to the PCI Local Bus Specification Revision 2.2. FL1100 is compatible for operation with USB 2.0 and USB 1.1 devices.

Adding the FL1100 into your PCI Express-based platform provides four high-performance USB ports that can be used for any USB application, including video displays, high definition cameras, high-performance storage, or countless other devices.

The FL1100 controller features Fresco Logic's patented GoXtream™ xHCI Accelerator Engine, which maps the xHCI standard directly into a set of parallel functional units, providing acceleration of all xHCI operations while maintaining compatibility with existing software driver models.

The FL1100 supports USB Debug Capability defined by the xHCI specification. Debug capability enables low-level system debug using a USB-to-USB connection between two computers, and is a requirement from Microsoft for those platforms that wish to achieve Windows Logo Certification for Windows 8 and beyond.

With its innovative architecture and high level of integration, FL1100 delivers exceptional performance, while minimizing total system cost and providing the most straightforward usage model in the industry.

The FL1100 controller is available in the following packages:

- DRQFN, 116 pin, 9mm×9mm
- TFBGA, 161 pin, 9mmx9mm

1.1 Features

- Compliant with USB 3.0 Specification Revision 1.0
- Compliant with Extensible Host Controller Interface (xHCI) Specification Revision 1.0
- 4 downstream USB ports support SS/HS/FS/LS data rates (5Gbps/480Mbps/12Mbps/1.5Mbps)
- Supports Battery Charging Specification Revision 1.2 for Charging Downstream Ports (CDP)
- Supports USB charging via Chinese Telecom Standard YD/T 1591-2009
- Supports Apple™ Charge
- Single (x1) PCI Express Lane
- Supports PCI Express Specification Revision 2.1 at 5GT/s
- Supports PCI Express Card Revision 1.0
- Supports PCI Bus Power Management Interface Specification Revision 1.2

- 3.3V/1.2V/1.05V power supply
- Supports 12MHz crystal oscillator
- Integrated SuperSpeed USB transceiver
- Integrated PCI Express transceiver
- WHQL certified driver support for Windows 8/8.1, Windows 7, Windows Vista and Windows XP
- Linux xHCI support under Linux kernel version 2.6.31 and after
- Supports UASP (USB Attached SCSI Protocol)
- Supports xHCI debug capability
- Support for Ultra High-performance isochronous applications
- Support for Latency Tolerance Reporting (PCIe) and Latency Tolerance Messaging (USB)

1.2 Applications

- Motherboard
- Notebook
- Add-in card
- Express card
- Thunderbolt and PCIe-based Docking
- DTV
- Embedded PC
- Any consumer product with PCIe interface

1.3 Ordering Information

Table 1-1 Ordering Information

Part Number	Description	Status
FL1100-1Q0-EX	Major Revision 1, DRQFN 116 pin, 9mm x 9mm	Production
FL1100-1G0-EX	Major Revision 1, TFBGA 161 pin, 9mm x 9mm	Production

1.4 Top Marking

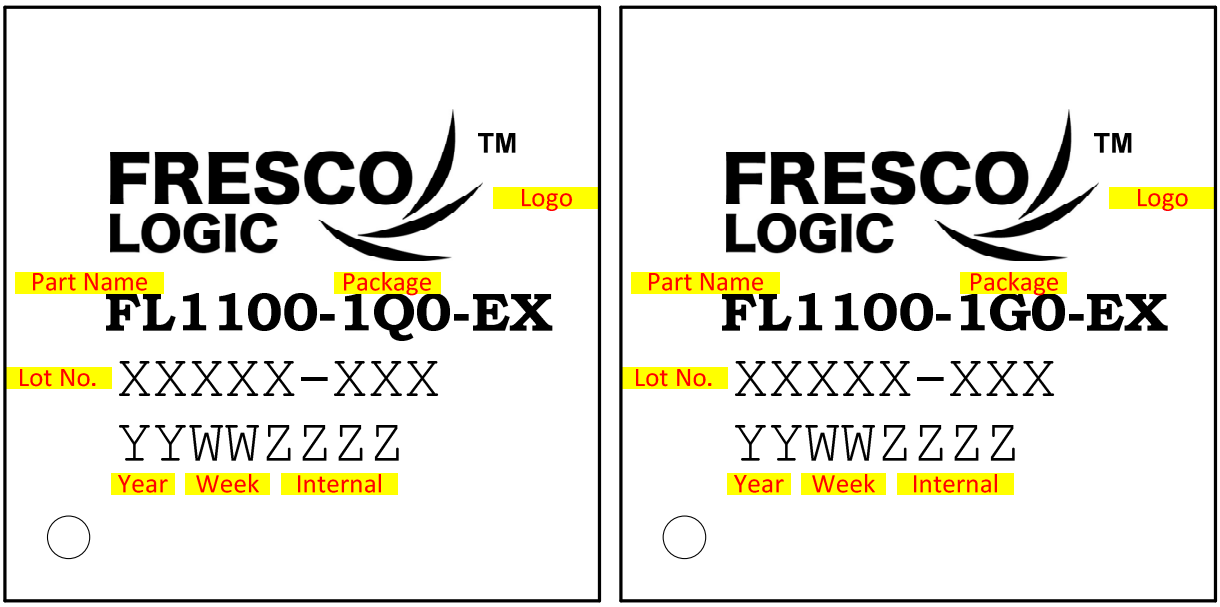


Figure 1 FL1100 Top Marking

Figure 1 illustrates the top marking of FL1100 samples. The part number is composed of two portions: “FL1100” is the part name, which tells the product family; the “1Q0” & “1G0” denote the major stepping and the package type as major revision 1 and DRQFN and TFBGA package respectively. The B0 indicates the full production stepping.

2. Signal Description

This chapter provides signal mapping and detailed description of each signal of FL1100. The following notations are the signal type:

- LVTTL Digital control signal
- DIFF Analog Differential pair
- ANA Analog I/O
- OD Open Drain I/O

2.1 Ballout Definition

Figure 2 shows the ballout map of FL1100 from the top of the package view.

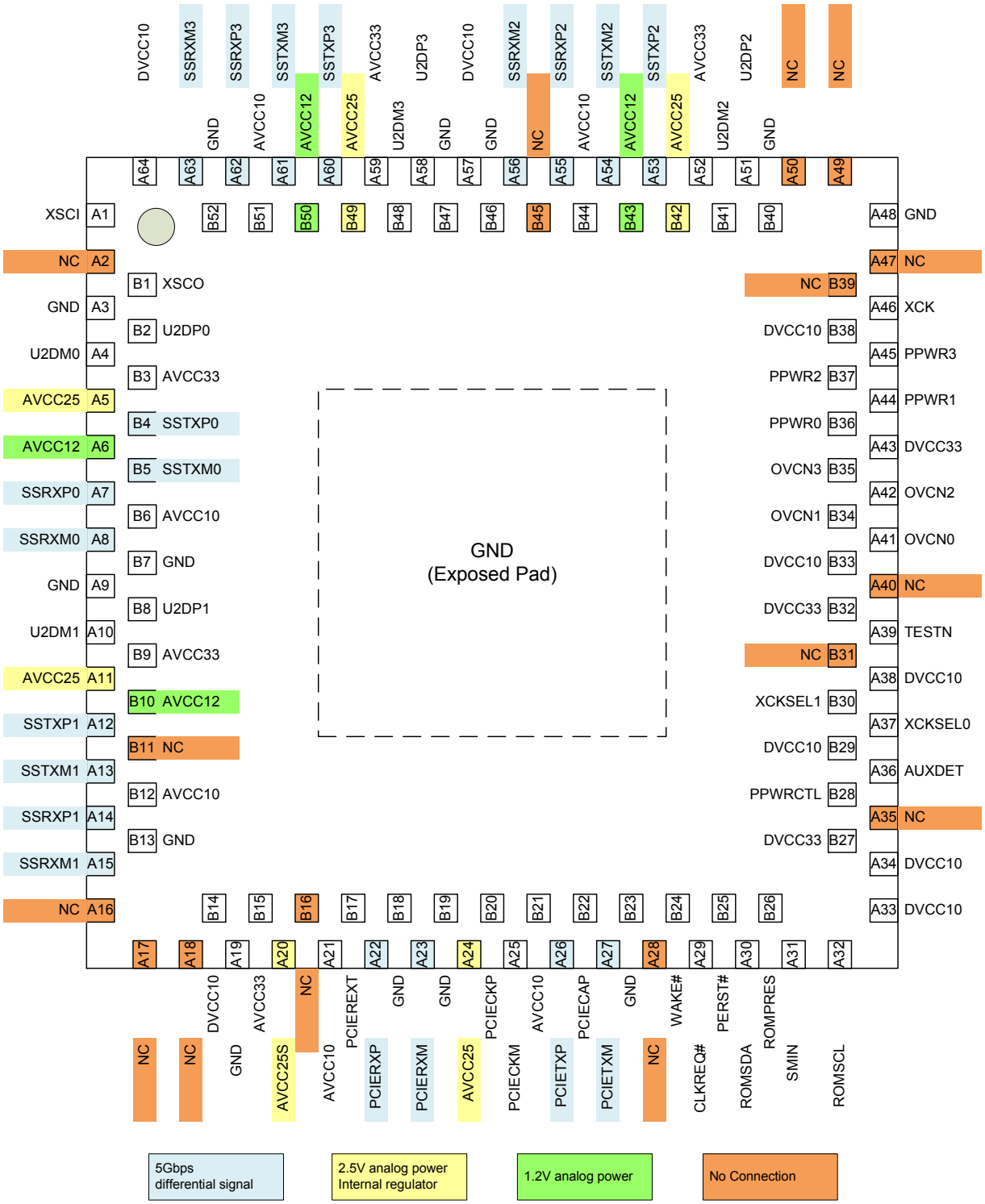
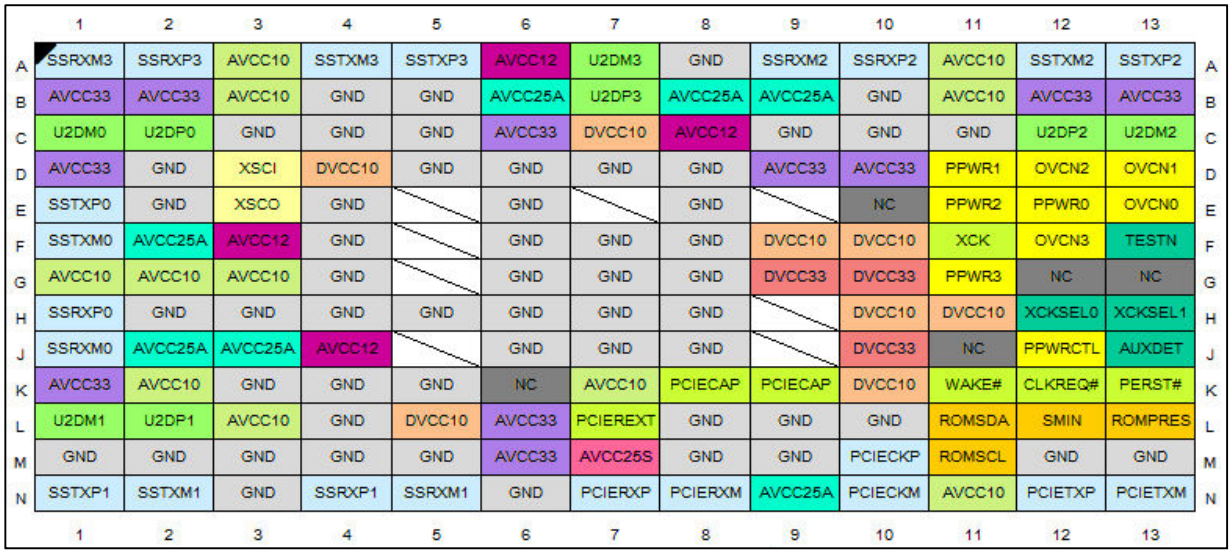


Figure 2 FL1100 DRQFN 116-pin 9mm×9mm Ballout Map (Top view / Transparent View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	SSRXM3	SSRXP3	AVCC10	SSTXM3	SSTXP3	AVCC12	U2DM3	GND	SSRXM2	SSRXP2	AVCC10	SSTXM2	SSTXP2	A
B	AVCC33	AVCC33	AVCC10	GND	GND	AVCC25A	U2DP3	AVCC25A	AVCC25A	GND	AVCC10	AVCC33	AVCC33	B
C	U2DM0	U2DP0	GND	GND	GND	AVCC33	DVCC10	AVCC12	GND	GND	GND	U2DP2	U2DM2	C
D	AVCC33	GND	XSCI	DVCC10	GND	GND	GND	GND	AVCC33	AVCC33	PPWR1	OVCN2	OVCN1	D
E	SSTXP0	GND	XSCO	GND		GND		GND		NC	PPWR2	PPWR0	OVCN0	E
F	SSTXM0	AVCC25A	AVCC12	GND		GND	GND	GND	DVCC10	DVCC10	XCK	OVCN3	TESTN	F
G	AVCC10	AVCC10	AVCC10	GND		GND	GND	GND	DVCC33	DVCC33	PPWR3	NC	NC	G
H	SSRXP0	GND	GND	GND	GND	GND	GND	GND		DVCC10	DVCC10	XCKSEL0	XCKSEL1	H
J	SSRXM0	AVCC25A	AVCC25A	AVCC12		GND	GND	GND		DVCC33	NC	PPWRCTL	AUXDET	J
K	AVCC33	AVCC10	GND	GND	GND	NC	AVCC10	PCIECAP	PCIECAP	DVCC10	WAKE#	CLKREQ#	PERST#	K
L	U2DM1	U2DP1	AVCC10	GND	DVCC10	AVCC33	PCIEREXT	GND	GND	GND	ROMSDA	SMIN	ROMPRES	L
M	GND	GND	GND	GND	GND	AVCC33	AVCC25S	GND	GND	PCIECKP	ROMSCL	GND	GND	M
N	SSTXP1	SSTXM1	GND	SSRXP1	SSRXM1	GND	PCIERXP	PCIERXM	AVCC25A	PCIECKM	AVCC10	PCIETXP	PCIETXM	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 3 FL1100 TFBGA 161-pin 9mm×9mm Ballout Map (Top view / Transparent View)

2.2 Signal Descriptions

This section contains detailed signal for each interface.

2.2.1 PCI Express Interface

Table 2-1 Signal description of PCIe Interface

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Type	Dir.	Description
WAKE#	B24	K11	OD	O	PCIe wakeup signal, active low
CLKREQ#	A29	K12	OD	O	Indicate when REFCLK is needed for express card, active low
PERST#	B25	K13	LVTTL	I	PCIe reset, active low, internal pull-up
PCIECKP	B20	M10	DIFF	I	PCIe differential clock (+), 100MHz
PCIECKM	A25	N10	DIFF	I	PCIe differential clock (-), 100MHz
PCIEREXT	B17	L7	ANA	O	Connect an external resistor (12kΩ ± 1%) to AGND33
PCIECAP	B22	K8, K9	ANA	O	Connect an external capacitor 100nF to AGND33
PCIERXP	A22	N7	DIFF	I	The PCI Express differential inputs to the PHY (+)
PCIERXM	A23	N8	DIFF	I	The PCI Express differential inputs to the PHY (-)
PCIETXP	A26	N12	DIFF	O	The PCI Express differential outputs from the PHY (+)
PCIETXM	A27	N13	DIFF	O	The PCI Express differential outputs from the PHY (-)

2.2.2 USB Port 0 Interface

Table 2-2 Signal description of USB Port 0 Interface

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Type	Dir.	Description
U2DP0	B2	C2	DIFF	IO	USB2.0 differential data (+).
U2DM0	A4	C1	DIFF	IO	USB2.0 differential data (-).
SSTXP0	B4	E1	DIFF	O	USB3.0 SuperSpeed differential output (+)
SSTXM0	B5	F1	DIFF	O	USB3.0 SuperSpeed differential output (-)
SSRXP0	A7	H1	DIFF	I	USB3.0 SuperSpeed differential input (+)
SSRXM0	A8	J1	DIFF	I	USB3.0 SuperSpeed differential input (-)
PPWR0	B36	E12	LVTTL	O	Vbus port power control, when PPWRCTL=1 (optional)
OVCN0	A41	E13	LVTTL	I	Indicate over current occurs on VBus, active low, internal pull-up (optional)

2.2.3 USB Port 1 Interface

Table 2-3 Signal description of USB Port 1 Interface

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Type	Dir.	Description
U2DP1	B8	L2	DIFF	IO	USB2.0 differential data (+).
U2DM1	A10	L1	DIFF	IO	USB2.0 differential data (-).
SSTXP1	A12	N1	DIFF	O	USB3.0 SuperSpeed differential output (+)
SSTXM1	A13	N2	DIFF	O	USB3.0 SuperSpeed differential output (-)
SSRXP1	A14	N4	DIFF	I	USB3.0 SuperSpeed differential input (+)
SSRXM1	A15	N5	DIFF	I	USB3.0 SuperSpeed differential input (-)
PPWR1	A44	D11	LVTTL	O	Vbus port power control, when PPWRCTL=1 (optional)
OVCN1	B34	D13	LVTTL	I	Indicate over current occurs on VBus, active low, internal pull-up (optional)

2.2.4 USB Port 2 Interface

Table 2-4 Signal description of USB Port 2 Interface

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Type	Dir.	Description
U2DP2	A51	C12	DIFF	IO	USB2.0 differential data (+).
U2DM2	B41	C13	DIFF	IO	USB2.0 differential data (-).
SSTXP2	A53	A13	DIFF	O	USB3.0 SuperSpeed differential output (+)
SSTXM2	A54	A12	DIFF	O	USB3.0 SuperSpeed differential output (-)
SSRXP2	A55	A10	DIFF	I	USB3.0 SuperSpeed differential input (+)
SSRXM2	A56	A9	DIFF	I	USB3.0 SuperSpeed differential input (-)
PPWR2	B37	E11	LVTTL	O	Vbus port power control, when PPWRCTL=1 (optional)
OVCN2	A42	D12	LVTTL	I	Indicate over current occurs on VBus, active low, internal pull-up (optional)

2.2.5 USB Port 3 Interface

Table 2-5 Signal description of USB Port 3 Interface

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Type	Dir.	Description
U2DP3	A58	B7	DIFF	IO	USB2.0 differential data (+).
U2DM3	B48	A7	DIFF	IO	USB2.0 differential data (-).
SSTXP3	A60	A5	DIFF	O	USB3.0 SuperSpeed differential output (+)
SSTXM3	A61	A4	DIFF	O	USB3.0 SuperSpeed differential output (-)
SSRXP3	A62	A2	DIFF	I	USB3.0 SuperSpeed differential input (+)
SSRXM3	A63	A1	DIFF	I	USB3.0 SuperSpeed differential input (-)
PPWR3	A45	G11	LVTTL	O	Vbus port power control, when PPWRCTL=1 (optional)
OVCN3	B35	F12	LVTTL	I	Indicate over current occurs on VBus, active low, internal pull-up (optional)

2.2.6 Miscellaneous Signals

Table 2-6 Signal description of miscellaneous signals

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Type	Dir.	Description
XSCI	A1	D3	ANA	I	Crystal oscillator output 12Mhz
XSCO	B1	E3	ANA	O	Crystal oscillator output 12Mhz
XCKSEL0	A37	H12	LVTTL	I	XCKSEL[1:0] is a 2-bit signal for selecting reference clock source 00: 12MHz crystal oscillator to XSCI/XSCO (default: internal pull-down) Other states reserved.
XCKSEL1	B30	H13	LVTTL	I	
XCK	A46	F11	LVTTL	I	Reference clock input (reserved)
SMIN	A31	L12	LVTTL	O	SMI interrupt output pin, active low, internal pull-up
ROMSDA	A30	L11	LVTTL	IO	External EEPROM interface. I2C data, internal pull-up (optional)
ROMSCL	A32	M11	LVTTL	O	External EEPROM interface. I2C clock, internal pull-up (optional)
ROMPRES	B26	L13	LVTTL	I	External EEPROM interface. ROM present, internal pull-down (optional)
PPWRCTL	B28	J12	LVTTL	I	VBus controllable via PPWR pins, internal pull-up 0: VBus is NOT controlled by FL1100 (connect a 4.7K resistor to GND) 1: VBus is controlled by FL1100 (default).
AUXDET	A36	J13	LVTTL	I	AUX power detection, internal pull-up Connect a 4.7K resistor to DGND to disable remote wake-up from D3cold.
TESTN	A39	F13	LVTTL	I	Test pin, connect a 4.7K resistor to DVCC33

2.2.7 Power / Ground

Table 2-7 Power / ground signals

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Description
AVCC33	A52, A59, B3, B9, B15	B1, B2, B12, B13, C6, D1, D9, D10, K1, L6, M6	Analog 3.3V power
GND	A3, A9, A19, A48, B7, B13, B18, B19, B23, B40, B46, B47, B52, Exposed Pad	A8, B4, B5, B10, C3, C4, C5, C9, C10, C11, D2, D5, D7, D8, E2, E4, E6, E8, F4, F6, F7, F8, G4, G6, H2, H3, H4, H5, H6, K3, K4, L4, L8, L9, L10, M1, M2, M3, M4, M5, M8, M9, N3, N6, D6, G7, G8, H7, H8, J6, J7, J8, K5, M12, M13	Ground
AVCC10	A21, B6, B12, B21, B44, B51	A3, A11, B3, B11, G1, G2, G3, K2, K7, L3, N11	Analog 1.05V power
AVCC12	A6, B10, B43, B50	A6, C8, F3, J4	Analog 1.2V power
DVCC33	A43, B27, B32	G9, G10, J10	Digital 3.3V power
DVCC10	A33, A34, A38, A57, A64, B14, B29, B33, B38	C7, D4, F9, F10, H10, H11, K10, L5	Digital 1.05V power

Table 2-8 Internal generate power supplies

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Description
AVCC25S	A20	M7	Generate internally 2.5V output
AVCC25	A5, A11, A24, B42, B49	B6, B8, B9, F2, J2, J3, N9	Connect to AVCC25S

2.2.8 NC Pins

Table 2-9 No connection pin list

Pin Name	Ball # DRQFN 116	Ball # TFBGA 161	Description
NC Pins	A2, A16, A17, A18, A28, A35, A40, A47, A49, A50, B11,B16, B31, B39, B45	E10, G12, G13, J11, K6,	Leave these pins no connection

3. Function Description

The FL1100 from Fresco Logic adds USB connectivity to any platform with a PCI Express bus. As shown in the

following block diagram, the FL1100 is a complete USB subsystem, incorporating virtually everything needed to attach 4 SuperSpeed-capable USB ports to a PCIe Interface. A high level of integration of the FL1100 makes adding USB to the platform simple and cost effective.

3.1 Block Diagram

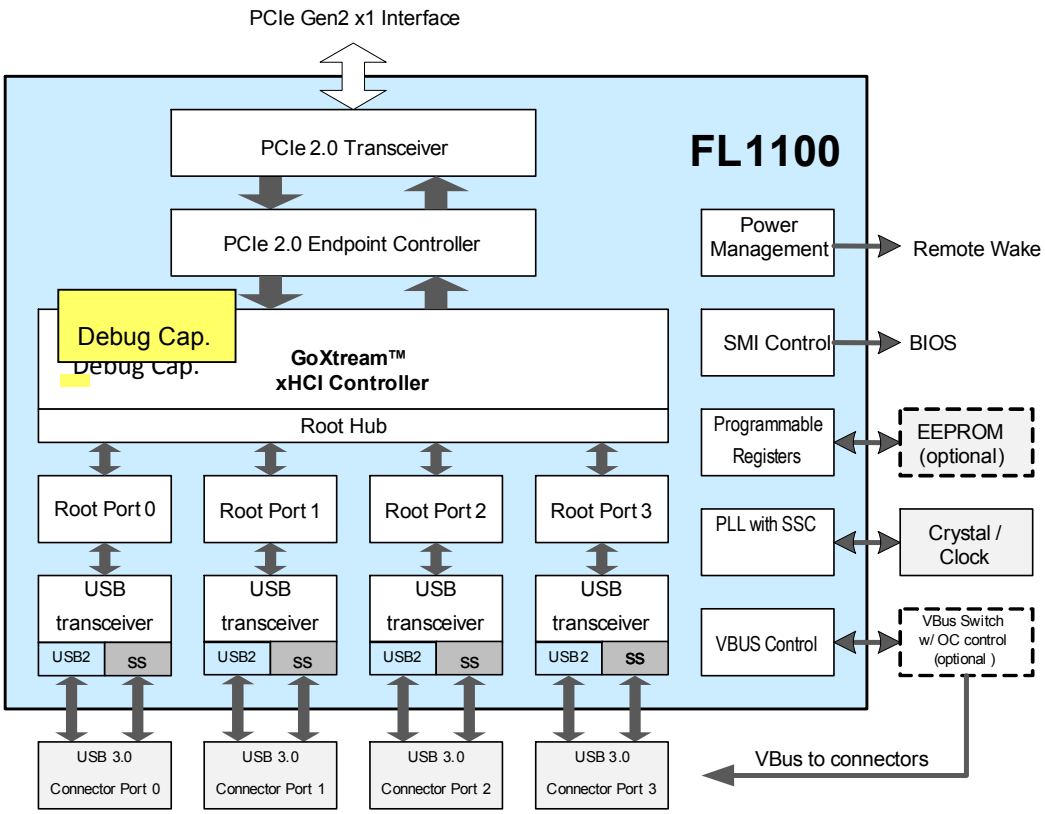


Figure 4 FL1100 block diagram

3.2 xHCI Controller

The FL1100 from Fresco Logic is a high-performance PCI Express-based xHCI host controller, which supports all required functions of the xHCI Specification Revision 1.0. The FL1100 controller is highly integrated and features Fresco Logic's patented GoXtream™ xHCI acceleration technology. Dedicated functional units provide full hardware acceleration of all xHCI functionality, guaranteeing the best possible performance while minimizing power.

The performance is enhanced by eliminating the inherent latencies and bottlenecks of hardware/software hand-offs. The power is reduced by eliminating the overhead of the additional processors, components and circuitry needed for software-based approaches. Additional benefits of this highly-integrated approach are lower

total system cost and a simpler deployment and usage model.

The FL1100 is fully integrated with PCI Express and USB transceivers and supports both USB 3.0 and USB 2.0 devices. The FL1100 features a Gen 2, x1 PCI Express lane and four USB 3.0 downstream ports.

The FL1100 supports the full capabilities of traversing the Scatter/Gather list to complete the DMA functions called out by the xHCI Specification. The general interfaces described in the xHCI Specification include a Host Configuration Space, a Memory- mapped IO space and a Host memory space. Chapter 5 contains the details of these memory spaces within the FL1100 xHCI controller.

FL1100's GoXtream™ engine furthers performance with improved caching and an enhanced scheduler which manages simultaneous data movement across all ports permitting maximum bandwidth utilization up to the limit of the system interface. The built-in scheduler also protects the priority of Isochronous and Interrupt transfers over other types of traffic.

3.3 xHCI Debug Capability

The FL1100 supports Debug Capability that enables low-level system debug over USB. The xHCI debugging capability provides a means of connecting two systems where one system is a Debug Host and the other a Debug Target (System under Test). The USB Debug Capability defines the implementation requirements of a Debug Target presenting a Debug Device to a Debug Host. A Debug Device is fully compliant with the USB Framework and provides the equivalent of a very high performance full-duplex serial link between a Debug Host and a Debug Target.

Each port of FL1100 is fully compliant to the required implementation and behavior of the USB3 Debug Capability defined in the xHCI specification.

3.4 Root Hub and Root Ports

The FL1100 implements the Root Hub functionality described in the USB 3.0 Specification. FL1100 supports a 4 port configuration.

The root port provides USB-specified link functionality for SuperSpeed, high-speed, full-speed and low-speed links. It communicates with the USB transceiver (PHY) to transfer the data onto the link. Each root port has buffers to support the bandwidth requirements of its link.

Additionally, each port has its own power management and link negotiation capabilities, allowing individual ports to power down separately. Link management is done in each of the root ports, which can be suspended or reset by software without affecting overall xHCI controller operation.

3.5 USB Transceiver

FL1100 integrates a 4-port 5Gbps SuperSpeed USB transceiver which is fully compliant with USB 3.0 specification and backward compatible with all USB 2.0 speeds: High-speed, full-speed and low-speed. The transceiver is equipped with adaptive receiver equalization, which enhances the receiving capability from signal attenuation due to the channel or crosstalk noise. As to clock generation, the transceiver supports a 12MHz external crystal, and provides the generation of Spread Spectrum Clocking (SSC), as required by the specification.

3.6 PCI Express Transceiver

FL1100 integrates a 5.0GT/s PCI Express transceiver which is fully compliant with the PCI Express Specifications Revision 2.0. It is capable of transmitting and receiving data at a rate of 5Gbps.

3.7 Power Management

3.7.1 USB Power States

FL1100 supports all power modes defined in USB 3.0 Specification. Table 3-1 addresses the USB 3.0 power modes.

Table 3-1 USB 3.0 Power State

Link State	Description	Characteristic	Exit Latency Range
U0	Link active	Link operational state	N/A
U1	Link idle – fast exit	RX and TX circuitry quiesced	us
U2	Link idle – slower exit	Clock generation circuitry may additionally be quiesced	us – ms
U3	Link suspend	Transceiver power is off	ms

FL1100 supports remote wake from USB device.

3.7.2 USB 2.0 Link Power Management (LPM)

FL1100 is compliant with "USB 2.0 Link Power Management Addendum", and supports both software and hardware managed LPM L1 power management. Table 3-2 compares the LPM L1 states and Suspend (L2) states.

Hardware LPM in FL1100 is a function to provide automatic power management of the USB2 link between the host root port and the first connected device. It achieves link power savings at latencies at least 2 to 3 orders of magnitude less than can be achieved by a typical host bus driver. Any bus idle that exceeds a pre-programmed latency threshold will cause the host to initiate the USB2 L1 state. Hardware LPM is schedule aware meaning the host will auto wake the device on any new transfer request or at periodic intervals required for interrupt and/or Isochronous endpoints.

Table 3-2 USB Link Power Management (Lx) States

Link State	Description	Entry handshake	Entry/Exit Latency
L0	Link active	N/A	N/A
L1	Link sleep	Explicitly entered via LPM extended transaction	Entry: ~10us Exit: ~70us to 1ms
L2	Suspend	Implicitly entered via 3ma of link inactivity	Entry: ~3ms Exit: > 30ms

The USB-IF release an errata in October, 2011 that changed the resume timescale duration of USB2 Link Power Management from a Host Initiated Resume Duration (HIRD) definition to a Best Effort Service Latency (BESL) definition. FL1100 has been updated to meet this new specification while continuing to allow HIRD specification for legacy software implementations. The new BESL method supports a wider range of timescales and thus a wider operating range of wake-up latencies, providing more opportunity for power savings.
Original behavior remains intact through proprietary controls and can be programmed back to HIRD behavior on a per-port basis, however the new BESL timescale is default to comply with ECN to xHCI specification.

3.7.3 PCIe Power States

FL1100 supports both PCI Power Management (PCIPM) and PCI Express Active State Power Management (ASPM). The ASPM may be initiated by FL1100 or by system software. FL1100 supports D0, D1, D3hot and D3cold states as well as ASPM L0s and L1 states.

3.7.4 PCIe Latency Tolerance Reporting (LTR) and USB3 Latency Tolerance Messages (LTM)

FL1100 provides support for xHCI Set Latency Tolerance Value (LTV) command processing. The FL1100 also contains an engine to consolidate the USB3 Latency Tolerance Messages received, USB2 BESL values, and the LTV value into a single lowest best-effort latency tolerance value (BELT) for reporting to PCIe via LTR messaging. LTR and LTM provide critical information for managing power within the platform.

3.7.5 Apple™ Charge

FL1100's USB2 ports provide compatible voltage levels with Apple™ 5W/10W chargers. This new charging function can provide the appearance of a dedicated charging adapter for high current charging devices such as Apple™ iPad™ and iPhone™. Charging function, off by default, can be programmed to auto-enable whenever the system is in S3 and can auto-detect between Apple™ and USB Battery charge spec devices (rev. 1.2) in that state. Charging downstream port (CDP) from USB Battery charge specification 1.2 function remains intact, however, with FL1100 all additional charging modes can be enabled from BIOS and can afterwards operate autonomously with no assistance from xHCI driver.

4. Electrical Characteristics

4.1 Operating Conditions

Table 4-1 Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Unit
DVCC10	Digital core power supply	1.0	1.05	1.1	V
DVCC33	Digital IO power supply	2.97	3.3	3.63	V
AVCC10	Analog 1.0V power supply	1.0	1.05	1.1	V
AVCC12	Analog 1.2V power supply	1.13	1.19	1.25	V
AVCC33	Analog 3.3V power supply	3.15	3.3	3.45	V
T_A	Operating ambient temperature	0		70	°C
T_C	Operating case temperature ($T_C = T_A + \theta P$)	0		105	°C

4.2 Absolute Maximum Ratings

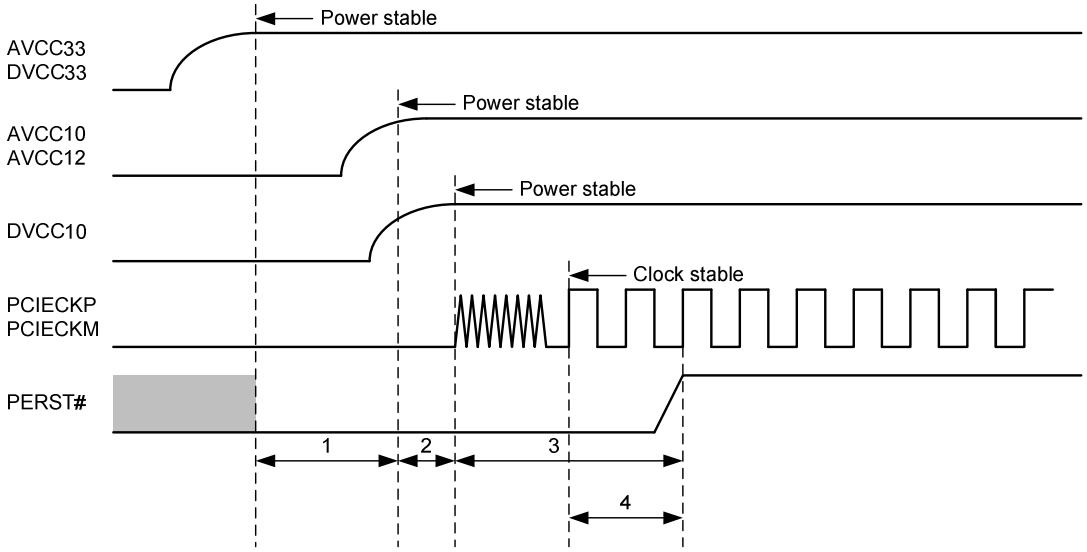
Permanent damage of devices may occur if the absolute maximum ratings are exceeded. These are only stress ratings, and the functional operations should be restricted within the conditions detailed in Table 4-2. Exposure to the absolute maximum rating conditions may also affect the reliability of the devices. The input and output negative voltage ratings may be exceeded if the input and output currents are not exceeded.

Table 4-2 Absolute Maximum Ratings

Symbol	Description	Rating	Unit
DVCC10	Digital core power supply	-0.5 ~ 1.4	V
DVCC33	Digital IO power supply	-0.5 ~ 4.6	V
AVCC10	Analog 1.0V power supply	-0.5 ~ 1.4	V
AVCC12	Analog 1.2V power supply	-0.5 ~ 1.4	V
AVCC33	Analog 3.3V power supply	-0.5 ~ 4.6	V
V_{IN3}	Input voltage of LVTTL IOs	-0.5 ~ 4.6	V
I_{IN}	DC input current	50	mA
I_{OUT}	DC output short circuit current	50	mA
T_{STG}	Storage temperature	-65 ~ 150	°C

4.3 Power-up Sequence

FL1100 has 1.05V and 3.3V voltage supplies for analog and digital functionalities respectively and also has 2 resets: PERST# and internal power-on reset. Please follow below power-up sequence including power supplies, resets, and reference clocks.



1. All 3.3V (AVCC33, DVCC33) stable to AVCC10 stable
2. AVCC10/AVCC12 stable to DVCC10 stable
3. DVCC10 stable to PERST# de-asserted
4. Reference clock (PCIECKP, PCIECKM) stable to PERST# de-asserted

Figure 5 Power-up sequence

Table 4-3 Power-up sequence parameters

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T_{PON33_A10}	Time interval of 3.3V stable to AVCC10 stable		1	-	-	ms
T_{PONA10_D10}	Time interval of AVCC10 stable to DVCC10 stable	DVCC10 must NOT be earlier than AVCC10	0			ms
T_{POND10_PRST}	Time interval of DVCC10 stable to PERST# de-asserted		100			ms
T_{PONCK_PRST}	Time interval of PCIe reference clock stable to PERST# de-asserted		100			us

4.4 Power-down Sequence

Figure 6 illustrates the power-down sequence requirement of FL1100. Please follow below power-down sequence including power supplies, resets, and reference clocks.

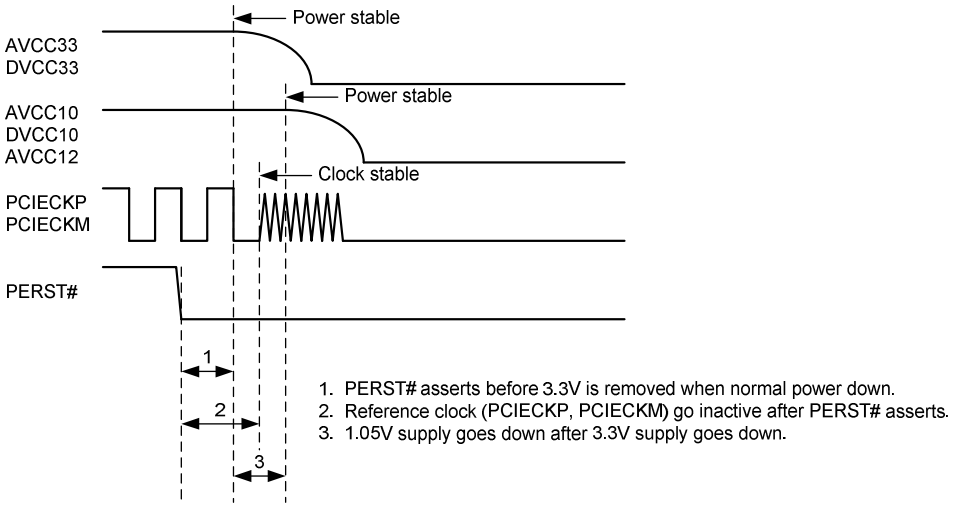


Figure 6 Power-down Sequence

Table 4-4 Power-down sequence parameters

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T_{PDN33_10}	Time interval of removing 3.3V to removing 1.05V supply.	1.05V must not be removed earlier than 3.3V supply removed.	0			ms

4.5 DC Electrical Specifications

The section defines the electrical specifications of digital signal pins which are defined as LVTTL in Chapter 2.

Table 4-5 LVTTL I/O DC Characteristic

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	3.3V LVTTL			0.8	V
V_{IH}	Input high voltage	3.3V LVTTL	2.0			V
V_{OL}	Output low voltage	3.3V LVTTL			0.4	V
V_{OH}	Output high voltage	3.3V LVTTL	2.4			V
R_{PU}	Internal pull-up resistor		40	75	190	KΩ
R_{PD}	Internal pull-down resistor		40	75	190	KΩ
C_{IN}	Input capacitance			2.1		pF

4.6 Power Consumption

Table 4-6 FL1100 maximum power consumption

Symbol	Condition	Power	Unit
P_{IDLE}	No device connected	300	mW
$P_{IDLE-LP}$	No device connected (low power mode)	50	mW
$P_{USB2-1P}$	1 USB 2.0 device connected	390	mW
$P_{USB3-1P}$	1 USB 3.0 device connected	450	mW
$P_{USB2-2P}$	2 USB 2.0 devices connected	480	mW

$P_{USB3-2P}$	2 USB 3.0 devices connected	600	mW
$P_{USB2-3P}$	3 USB 2.0 devices connected	550	mW
$P_{USB3-3P}$	3 USB 3.0 devices connected	790	mW
$P_{USB2-4P}$	4 USB 2.0 devices connected	615	mW
$P_{USB3-4P}$	4 USB 3.0 devices connected	970	mW
$P_{U3HUB-4P}$	4 USB 3.0 Hub connected (maximum condition)	1,220	mW
P_{SLEEP}	Host controller sleep with remote wake-up support	45	mW

Table 4-7 FL1100 operating current (typical corner measurement)

Symbol	Condition	Current of power lines					Total Current	Unit
		AVCC33	DVCC33	AVCC10	DVCC10	AVCC12		
I_{IDLE}	No device connected	46	0	43	88	0	177	mA
$I_{IDLE-LP}$	No device connected (low power mode)	3	0	24	13	0	40	mA
$I_{USB2-1P}$	1 USB 2.0 device connected	69	0	43	93	0	205	mA
$I_{USB3-1P}$	1 USB 3.0 device connected	57	0	75	94	49	235	mA
$I_{USB2-2P}$	2 USB 2.0 devices connected	86	0	43	104	0	233	mA
$I_{USB3-2P}$	2 USB 3.0 devices connected	70	0	107	111	98	386	mA
$I_{USB2-3P}$	3 USB 2.0 devices connected	109	0	43	115	0	267	mA
$I_{USB3-3P}$	3 USB 3.0 devices connected	98	0	139	130	147	514	mA
$I_{USB2-4P}$	4 USB 2.0 devices connected	131	0	43	124	0	298	mA
$I_{USB3-4P}$	4 USB 3.0 devices connected	118	0	171	148	196	633	mA
I_{SLEEP}	Sleep with remote wake-up support	3	0	13	13	0	29	mA

Table 4-8 FL1100 Maximum operating current (preliminary typical corner measurement)

Power	Description	Current	Unit
I_{10VMAX}	Maximum total current of AVCC10 and DVCC10	400	mA
I_{12VMAX}	Maximum total current of AVCC12	200	mA
I_{33VMAX}	Maximum total current of AVCC33 and DVCC33 (including 2.5V internal generation)	200	mA

4.7 AC Characteristics

The section defines the requirement of reference clock source and the power supplies.

Table 4-9 Reference clock specification

Symbol	Description	Condition	Min.	Type	Max.	Unit
F_{XTAL_12}	Frequency of 12MHz crystal		-30ppm	12	+30ppm	MHz
T_{DUTY}	Clock duty cycle		40	50	60	%
ESR	Crystal ESR		2.4		40	Ω

Table 4-10 Power noise specification

Symbol	Description	Condition	Min.	Type	Max.	Unit
$V_{NOISE33}$	Power noise on 3.3V supply	1 Hz ~ 100KHz			100	mVpp
$V_{NOISE12}$	Power noise on 1.2V supply	1 Hz ~ 100KHz			50	mVpp
$V_{NOISE10}$	Power noise on 1.0V supply	1 Hz ~ 100KHz			50	mVpp

4.8 USB Electrical Characteristics

Table 4-11 Electrical characteristic of SuperSpeed transmitter

Symbol	Description	Condition	Min.	Type	Max.	Unit
UI	Unit Interval		199.94	200.00	200.06	ps
$V_{TX-DIFF-PP}$	Differential peak-to-peak TX voltage swing	2 * $\|V_{TXP} – V_{TXN}\|$, measured at TX near-end	800		1200	mV
$V_{TX-DIFF-PP\_LOW}$	Low-power differential peak-to-peak TX voltage swing	2 * $\|V_{TXP} – V_{TXN}\|$, measured at TX near-end	400		1200	mV
$V_{TX-DE-RATIO}$	TX de-emphasis level		3.0		4.0	dB
$R_{TX-DIFF-DC}$	DC differential impedance		72		120	Ω
$C_{AC-COUPLING}$	AC coupling capacitor		75		200	nF
T_{TX-EYE}	Transmitter eye	Including all jitter sources, measured at the silicon pad.	0.625			UI
$T_{TX-DJ-NEAR}$	Near-end TX deterministic jitter	Deterministic jitter only assuming the Dual Dirac distribution, measured at the silicon pad by using the CP0 pattern.			0.205	UI
$T_{TX-DJ-FAR}$	Far-end TX deterministic jitter	Deterministic jitter only assuming the Dual Dirac distribution, measured at TP1			0.43	UI
$T_{TX-RJ-FAR}$	Far-end TX random jitter	Measured at the silicon pad by using the CP1 pattern at 10^{-12}BER			0.23	UI
$T_{TX-TJ-FAR}$	Far-end TX total jitter	Measured at the silicon pad (TJ = DJ + RJ)	-	-	0.66	UI
$C_{TX-PARASITIC}$	TX input capacitance for return loss	-	-	-	1.25	pF
R_{TX-DC}	Transmitter DC common-mode impedance	-	18	-	30	Ω
$V_{TX-DC-CM}$	TX DC common-mode voltage	-	-	0.75	1.2	V

$V_{TX-DC-CM-U0-U1}$	Absolute TX DC common-mode voltage between the U0 and U1 modes	-	-	0.75	1.2	V
V_{T-D-R}	The voltage change allowed during the receiver detection	The total amount of voltage change during TX-Detect-RX	-	-	200	mV

Table 4-12 Spread Spectrum Clocking (SSC) parameters

Symbol	Description	Condition	Min.	Type	Max.	Unit
$T_{SSC-MOD-RATE}$	Modulation rate	USB transceiver power	30	31.5	33	KHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	USB PLL power	0	4000	5000	ppm
$T_{SSC-SLEW-RATE}$	SSC slew rate	USB transceiver power	-	-	10	ms/s

Table 4-13 Electrical characteristics of LFPS

Symbol	Description	Condition	Min.	Type	Max.	Unit
T_{Period}	Period of the LFPS signal	-	20	-	100	ns
$V_{CM-AC-LFPS}$	LFPS AC common-mode voltage	-	-	0.75	1.2	V
$V_{TX-DIFF-PP-LFPS}$	Differential peak-to-peak LFPS voltage swing	2 * $\|V_{TXP} – V_{TXN}\|$, measured at TX near-end	800	-	1200	mV
$V_{TX-DIFF-PP-LFPS-LP}$	Low-power differential peak-to-peak LFPS voltage swing	2 * $\|V_{TXP} – V_{TXN}\|$, measured at TX near-end	400	-	1200	mV
$T_{RISE-FALL-2080}$	Rise/Fall time of the LFPS signal	-	-	-	4	ns

Table 4-14 Electrical characteristics of SuperSpeed receiver

Symbol	Description	Condition	Min.	Type	Max.	Unit
UI	Unit interval	-	199.94	200.00	200.06	ps
R_{RX-DC}	Receiver common-mode impedance	-	18	-	30	Ω
$R_{RX-DIFF-DC}$	Receiver DC differential impedance	-	72	-	120	Ω
$V_{RX-LFPSDET-DIFF-PP}$	LFPS detect threshold	-	100	-	300	mV
$V_{RX-DIFF-PP-POSTEQ}$	Differential RX peak-to-peak voltage	-	30	-	-	mV
T_{RX-TJ}	Max RX inherent timing error	-	-	-	0.45	UI
T_{RX-DJ}	Max RX inherent deterministic timing error	-	-	-	0.285	UI
$C_{RX-PARASITIC}$	RX input capacitance for return loss	-	-	-	1.1	pF
$V_{RX-AC-CM}$	RX AC common-mode voltage	-	-	-	150	mV
$V_{RX-AC-CM-U0-U1}$	RX AC common-mode voltage during the U0-to-U1 transition	-	-	-	200	mV

Table 4-15 Electrical characteristic of USB 2.0 High-speed

Symbol	Description	Condition	Min.	Typ.	Max.	Unit

Driver characteristic						
$T_{HSRDRATE}$	High-speed TX data rate	-	479.76	-	480.24	Mbps
$T_{HSRDRATE}$	High-speed RX data rate	-	479.76	-	480.24	Mbps
t_{HSR}	High-speed differential rise time	-	500	-	-	ps
t_{HSF}	High-speed differential fall time	-	500	-	-	ps
Input level of differential receiver						
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$, measured at the connection of an application circuit.	300	-	-	mV
V_{HSCM}	High-speed data signaling common-mode voltage range	-	−50	-	500	mV
V_{HSDSC}	High-speed disconnection detection threshold	Disconnection detected	625	-	-	mV
		No disconnection detected	-	-	525	mV
Output Level						
V_{HSOI}	High-speed idle level output voltage (Differential)	-	-10	-	10	mV
V_{HSOL}	High-speed low level output voltage (Differential)	-	-10	-	10	mV
V_{HSOH}	High-speed high level output voltage (Differential)	-	360	400	440	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential)	-	700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential)	-	-900	-	-500	mV
$I_{DP/DM}$	Allowable output current of DP/DM	The termination is 45 Ω ±10%.	14.55	17.78	21.79	mA
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
Z_{HSTERM}	Differential impedance	-	76.5	90	103.5	Ω

Table 4-16 Electrical characteristic of USB 2.0 full-speed/low-speed

Symbol	**Description**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Full-speed driver characteristic						
$T_{FSDRATE}$	Full-speed TX data rate	-	11.994	-	12.006	Mbps
$T_{FSRDRATE}$	Full-speed RX data rate	-	11.97	-	12.03	Mbps
t_{FR}	Rise time	CL = 50 pF 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time	CL = 50 pF 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR}/t_{FF})	Excluding the first transition from the idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Low-speed driver characteristic						
$T_{LSDRATE}$	Low-speed TX data rate	-	1.49925	-	1.50075	Mbps
$T_{LSRDRATE}$	Low-speed RX data rate	-	1.49625	-	1.50375	Mbps
t_{LR}	Rise time	CL = 200 pF ~ 600 pF 10% ~ 90% of |VOH – VOL|	75	-	300	ns
t_{LF}	Fall time	CL = 200 pF ~ 600 pF	75	-	300	ns

		90% ~ 10% of $\|V_{OH} - V_{OL}\|$				
t_{LRMA}	Differential rise/fall time matching (t_{LR}/t_{LF})	Excluding the first transition from the idle mode	80	-	125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Input level of differential receiver						
V_{DI}	Differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common-mode voltage	-	0.8	-	2.5	V
ZHSDRV	Driver output resistance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
RPU1	Pull-up resistor during idle	Equivalent resistance used for the internal chip	900	-	1575	Ω
RPU2	Driver output resistance	Equivalent resistance used for the internal chip	525	-	1515	Ω
RPD	Driver output resistance	Equivalent resistance used for the internal chip	14.25	-	24.8	kΩ
Input level of single-ended receiver						
V_{SE}	Single-ended receiver threshold	-	0.8	-	2.0	V
Output level						
V_{OL}	Low-level output voltage	-	0	-	0.3	V
V_{OH}	High-level output voltage	-	2.8	-	3.6	V

4.9 PCIe Electrical Characteristics

Table 4-17 Electrical characteristic of PCIe

Symbol	Description	Condition	Min.	Type	Max.	Unit
Input level						
$V_{RX-DIFF}$	High speed differential input signals	$\|V_{RX(DIP)} - V_{RX(DIN)}\|$, measured at the connection of receiver's near end.	87.5	-	600	mV
T_{RX-EYE}	Receiver eye time opening	Minimum eye time at Rx pins to yield a 10E-12 BER	0.4	-	-	UI
V_{IDLE}	Electrical idle detect threshold	IDLE detected	-	-	87.5	mV
		Non IDLE detected	87.5	-		mV
$V_{RX-CM-AC}$	RX and AC common-mode voltage	Peak voltage	-	-	150	mV
Output levels						
$V_{TX-DIFF}$	High speed differential output signal	$\|V_{TX(DOP)} - V_{TX(DON)}\|$, measured at the connection of transmitter's near end.	400	-	600	mV
T_{TX-EYE}	Transmitter eye time opening	Minimum eye time at Rx pins to yield 10E-12 BER	0.75	-	-	UI
$V_{TX-IDLE-AC}$	Electrical idle differential peak output voltage	-	-	-	20	mV
V_{T-D-R}	The amount of voltage change allowed during receiver detection	The total amount of voltage change during TX-Detect-RX	-	-	600	mV
$V_{TX\_CM\_AC}$	Transmitter AC common-mode voltage	AC RMS value	-	-	20	mV

V_{TX_DEM}	TX de-emphasis level		-3	-	-4	dB
F_{BEACON}	Frequency of beacon signaling	-	2	-	150	MHz
Resistance						
R_{RX}	Built-in receiver input impedance	-	40	50	60	Ω
R_{TX}	Built-in driver output impedance	-	40	50	60	Ω
Capacitance						
C_{TX}	AC coupling capacitor	-	75	-	200	nF

5. PCI Express Registers

5.1 Register Types

Table 5-1 Register Types

Register Attribute	Description
RO	Read-only Register bits are read-only and cannot be altered by software
RW	Read-write Register bits are read-write and are permitted to be Set or Cleared by software
RW1C	Write-1-to-clear status Register bits indicate status when read. The status is cleared by writing 1b. Writing 0b has no effect.
RW1S	Write-1-toset status Register bits indicate status when read. The status is set by writing 1b. Writing 0b has no effect
ROS	Read-only, Sticky Register bits are read-only and cannot be altered by software. Bits are not be initialized nor modified by hot reset or functional level reset (FLR)
RWS	Read-write, Sticky Register bits are read-write and are permitted to be Set or Cleared by software. Bits are not initialized nor modified by hot reset or functional level reset (FLR)
RW1CS	Write-1-to-clear status, Sticky Register bits indicate status when read. The status is cleared by writing 1b. Writing 0b has no effect. Bits are not initialized nor modified by hot reset or functional level reset (FLR)

5.2 PCI Express Configuration Register Map

FL1100 xHCI controller is a PCI-based xHC (extensible Host Controller) which is required to implement a PCI, Type 0 PCI device header as Table 5-2. FL1100 also implements two Base Address Registers (BAR 0 and BAR 1) to enable 64-bit addressing. These Base Address Registers are used to point to the start of the host controller's memory-mapped Input/Output (MMIO) register spaces, as described in section 5.3.

Table 5-2 PCIe Configuration Register Map

Registers 31 0				Offset
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
BIST	Header type	Latency Timer	Cache Line Size	00Ch
Base Address Registers (BAR)				010h
				014h
				018h

				01Ch
				020h
				024h
Reserved				028h
Subsystem ID		Subsystem Vendor ID		02Ch
Reserved				030h
Reserved			Capabilities Pointer	034h
Reserved				038h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	03Ch
Power Management Capability		Next Capability Pointer	PM Cap ID	40h
PM Data	PMCSR_BSE	Power Management Control/Status		44h
Reserved				48h
				4Ch
MSI Message Control		Next Capability Pointer	MSI Cap ID	50h
MSI Message Address				54h
MSI Upper Message Address				58h
Reserved		MSI Message Data		5Ch
Reserved		FLADJ	SBRN	60h
Reserved				64h
				68h
				6Ch
PCI Express Capability Register		Next Capability Pointer	PCI Express Cap ID	70h
Device Capabilities				74h
Device Status		Device Control		78h
Link Capabilities				7Ch
Link Status		Link Control		80h
Reserved				84h
				…
				90h
Device Capabilities 2				94h
Device Status 2		Device Control 2		98h
Link Capability 2				9Ch
Link Status 2		Link Control 2		A0h
Reserved				A4h
				A8h
				ACh
MSI-X Message Control		Next Item Pointer	MSI-X Cap ID	B0h
MSI-X Table Offset and BIR				B4h
MSI-X PBA Offset and BIR				B8h
Reserved				BCh
				…
EEPROM Control				F0h
Programmability Offset				F4h
Programmability Data				F8h
Reserved				FCh

5.2.1 PCI Express Configuration Register Description

5.2.1.1 Vendor ID Register

Address Offset:	00h	Attribute:	RO
Default value:	1B73h	Size:	16 bits

Bit	Description	Attribute
15:0	Vendor ID. A 16-bit value assigned to Fresco Logic Inc: 1B73h.	RO

5.2.1.2 Device ID Register

Address Offset:	02h	Attribute:	RO
Default value:	1100h	Size:	16 bits

Bit	Description	Attribute
15:0	Device ID. A 16-bit value assigned to FL1100: 1100h.	RO

5.2.1.3 Command Register

Address Offset:	04h	Attribute:	RW, RO
Default value:	0000h	Size:	16 bits

Bit	Description	Attribute
8	SERR# Enable	RW
6	Parity Error Response	RW
2	Bus Master Enable. Default value of this bit is 0b.	RO
Other bits	Reserved	RO

5.2.1.4 Status Register

Address Offset:	06h	Attribute:	RW1C, RO
Default value:	0010h	Size:	16 bits

Bit	Description	Attribute
15	Detected Parity Error	RW1C (Read, Write 1 to Clear)
14	Signaled System Error	RW1C
13	Received Master Abort	RW1C
12	Received Target Abort	RW1C
11	Signaled Target Abort	RW1C
8	Master Data Parity Error	RW1C
4	Capabilities List	RO
3	Interrupt Status	RO
Other bits	Reserved	RO

5.2.1.5 Revision ID Register

Address Offset:	08h	Attribute:	RO
Default value:	10h	Size:	8 bits

Bit	Description	Attribute
7:0	Silicon Revision. FL1100-EX is read 10h	RO

5.2.1.6 Class Code Register

Address Offset:	09	Attribute:	RO
Default value:	0C 0330h	Size:	24 bits

Bit	Description	Attribute
23:16	Base Class Code (BASEC). 0Ch = Serial Bus controller.	RO
15:8	Sub-Class Code (SCC). 03h = Universal Serial Bus Host Controller.	RO
7:0	Programming Interface (PI). 30h = USB 3.0 Host Controller that conforms to this specification	RO

5.2.1.7 Cache Line Size Register

Address Offset:	0Ch	Attribute:	RW
Default value:	0h	Size:	8 bits

Bit	Description	Attribute
7:0	This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but not applied to FL1100 functionalities.	RW

5.2.1.8 Latency Timer Register

Address Offset:	0Dh	Attribute:	RO
Default value:	0h	Size:	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1100.	RO

5.2.1.9 Header Type Register

Address Offset:	0Eh	Attribute:	RO
Default value:	0h	Size:	8 bits

Bit	Description	Attribute
7:0	FL1100 supports type 0 PCI header.	RO

5.2.1.10 BIST

Address Offset:	0Fh	Attribute:	RO
Default value:	0h	Size:	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1100	RO

5.2.1.11 Base Address Register 0

Address Offset:	10h	Attribute:	RO, RW
Default value:	0000 0004h	Size:	32 bits

Bit	Description	Attribute
31:4	Base address	RW
3	Prefetchable	RO

2:1	Memory Type. This field is read 10b to indicate the memory can be located anywhere in 64-bit space	RO
0	Memory space indicator	RO

5.2.1.12 Base Address Register 1

Address Offset:	14h	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:0	Base address of upper 32 bit of the 64 bit memory address.	RW

5.2.1.13 Base Address Register 2

Address Offset:	18h	**Attribute:**	RO, RW
Default value:	0000 0004h	**Size:**	32 bits

Bit	Description	Attribute
31:4	Base address	RW
3	Prefetchable	RO
2:1	Memory Type. This field is read 10b to indicate the memory can be located anywhere in 64-bit space	RO
0	Memory space indicator	RO

5.2.1.14 Base Address Register 3

Address Offset:	1Ch	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:0	Base address of upper 32 bit of the 64 bit memory address.	RW

5.2.1.15 Base Address Register 4

Address Offset:	20h	**Attribute:**	RO, RW
Default value:	0000 0004h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:4	Base address	RW
3	Prefetchable	RO
2:1	Memory Type. This field is read 10b to indicate the memory can be located anywhere in 64-bit space	RO
0	Memory space indicator	RO

5.2.1.16 Base Address Register 5

Address Offset:	24h	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:0	Base address of upper 32 bit of the 64 bit memory address.	RW

5.2.1.17 Subsystem Vendor ID (SVID)

Address Offset:	2Ch	**Attribute:**	RO

Default value:	1B73h	Size:	16 bits

Bit	Description	Attribute
15:0	Defines the system manufacturer. This field should be chanced through programmability register.	RO

5.2.1.18 Subsystem ID (SSID)

Address Offset:	2Eh	Attribute:	RO
Default value:	1100h	Size:	16 bits

Bit	Description	Attribute
15:0	System Manufacturer defined Device ID. This field should be chanced through programmability register.	RO

5.2.1.19 Capability Pointer

Address Offset:	34h	Attribute:	RO
Default value:	40h	Size:	16 bits

Bit	Description	Attribute
15:0	Offset Pointer to PCIe configuration header.	RO

5.2.1.20 Interrupt Line Register

Address Offset:	3Ch	Attribute:	RO
Default value:	00h	Size:	8 bits

Bit	Description	Attribute
7:0	Interrupt line from FL1100 to issue interrupt to system software.	RO

5.2.1.21 Interrupt Pin Register

Address Offset:	3Dh	Attribute:	RO
Default value:	01h	Size:	8 bits

Bit	Description	Attribute
7:0	This field is read 01 to indicate FL1100 uses INTA.	RO

5.2.1.22 Min_Gnt Register

Address Offset:	3Eh	Attribute:	RO
Default value:	00h	Size:	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1100	RO

5.2.1.23 Max_Lat Register

Address Offset:	3Fh	Attribute:	RO
Default value:	0000h	Size:	8 bits

Bit	Description	Attribute
7:0	Not applied on FL1100	RO

5.2.1.24 PM Capability Identifier

Address Offset:	40h	Attribute:	RO
Default value:	01h	Size:	8 bits

Bit	Description	Attribute
7:0	Capability ID, this register is read 01h to identify this address is PCI Power Management registers	RO

5.2.1.25 Next Capability Pointer

Address Offset:	41h	Attribute:	RO
Default value:	50h	Size:	8 bits

Bit	Description	Attribute
7:0	Next Item Pointer Offset to point to the next MSI capability registers.	RO

5.2.1.26 Power Management Capability Register

Address Offset:	42h	Attribute:	RO
Default value:	DBC3h	Size:	16 bits

Bit	Description	Attribute
15:11	PME Support This field is read 11011b. FL1100 support D0, D1, D3hot and D3cold	RO
10	D2 Support This bit is read 0b to indicate FL1100 doesn't support D2 state	RO
9	D1 Support This bit is read 1b to indicate FL1100 support D1 state	RO
8:6	AUX current This field is read 111b. FL1100 required 375mA AUX current	RO
5	Device Specific Initialization (DSI)	RO
4	Reserved	RO
3	PME clock, tied 0 on PCIe device	RO
2:0	PM Version This field is read 011b to indicate FL1100 is compliant with PCI Power Management Interface Specification Revision 1.2	RO

5.2.1.27 Power Management Control/Status Register

Address Offset:	44h	Attribute:	RO, RWC, RW
Default value:	0000h	Size:	16 bits

Bit	Description	Attribute
15	PME_Status	RWC (Read, Write to clear)
14:13	Data_Scale, not supported by FL1100, read 00b	RO
12:9	Data_Select, not supported by FL1100, read 0000b	RO
8	PME# enable	RW
7:4	Reserved	RO
3	No_Soft_Reset	RO

2	Reserved	RO
1:0	PowerState 00b: D0 01b: D1 10b: D2 11b: D3hot	RW

5.2.1.28 MSI Capability Identifier

Address Offset:	50h	**Attribute:**	RO
Default value:	05h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Capability ID, this register is read 05h to identify this address is MSI	RO

5.2.1.29 Next Capability Pointer

Address Offset:	51h	**Attribute:**	RO
Default value:	70h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Next Item Pointer Offset to point to the next PCI Express capability registers.	RO

5.2.1.30 MSI Message Control Register

Address Offset:	52h	**Attribute:**	RO, RW
Default value:	0086h	**Size:**	16 bits

Bit	Description	Attribute
15:9	Reserved	RO
8	Per-vector masking capable	RO
7	64 bit address capable	RO
6:4	Multiple Message Enable	RW
3:1	Multiple Message Capable	RO
0	MSI enable	RW

5.2.1.31 MSI Message Address Register

Address Offset:	54h	**Attribute:**	RO, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:2	Message Address System-specified message address	RW
1:0	Reserved	RO

5.2.1.32 MSI Message Upper Address Register

Address Offset:	58h	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute

31:0	Message Address System-specified message upper address. Optional for 64-bit message address	RW

5.2.1.33 MSI Message Data Register

Address Offset:	5Ch	**Attribute:**	RW
Default value:	0000h	**Size:**	16 bits

Bit	Description	Attribute
15:0	Message Data System-specified message data.	RW

5.2.1.34 SBRN (Serial Bus Release Number) Register

Address Offset:	60h	**Attribute:**	RO
Default value:	30h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Serial Bus Specification Release Number 30h = Release 3.0, FL1100 is compliance to USB 3.0 specification All other combinations are reserved	RO

5.2.1.35 FLADJ (Frame Length Adjustment) Register

Address Offset:	61h	**Attribute:**	RWS
Default value:	20h	**Size:**	8 bits

Bit	Description	Attribute
7:6	Reserved	
5:0	Frame Length Timing Value. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF microframe length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000 (125us). **Frame Length**	RO

# HS bit times in decimal	FLADJ value decimal, (heximal)
59488	0 (00h)
59504	1 (01h)
59520	2 (02h)
…	…
59984	31 (1Fh)
60000 (125us)	32 (20h)
…	…
60480	62 (3Eh)
60496	63 (3Fh)

5.2.1.36 PCI Express Capability ID

Address Offset:	70h	**Attribute:**	RO

Default value:	10h	Size:	8 bits

Bit	Description	Attribute
7:0	Return 10h to indicate this is a PCI Express Capability Structure	RO

5.2.1.37 Next Capability Pointer

Address Offset:	71h	Attribute:	RO
Default value:	B0h	Size:	8 bits

Bit	Description	Attribute
7:0	Next Item Pointer Offset to point to the next MSI-X capability registers.	RO

5.2.1.38 PCI Express Capability Register

Address Offset:	72h	Attribute:	RO
Default value:	0002h	Size:	16 bits

Bit	Description	Attribute
15:14	Reserved	
13:9	Interrupt Message Number	RO
8	Slot Implemented Not applicable on FL1100, return 0.	RO
7:4	Device/Port type FL1100 returns 0h to indicate a PCIe Express Endpoint	RO
3:0	Capability version. FL1100 returns 2h to indicate compliant to PCIe Base R2.1	RO

5.2.1.39 Device Capabilities Register

Address Offset:	74h	Attribute:	RO
Default value:	00288FC2h	Size:	32 bits

Bit	Description	Attribute
31:29	Reserved	RO
28	Function Level Reset Capability	RO
27:26	Captured Slot Power Limit Scale	RO
25:18	Captured Slot Power Limit Value	RO
17:16	Reserved	RO
15	Role-Based Error Reporting	RO
14:12	Reserved	RO
11:9	Endpoint L1 Acceptable Latency	RO
8:6	Endpoint L0s Acceptable Latency	RO
5	Extended Tag Field Supported	RO
4:3	Phantom Function Supported FL1100 returns 00b to advertise no function number bits are used for Phantom Functions	RO
2:0	Max Payload Size Supported FL1100 returns 010b to advertise 512 bytes max payload	RO

5.2.1.40 Device Control Register

Address Offset:	78h	**Attribute:**	RW, RO
Default value:	2810h	**Size:**	16 bits

Bit	**Description**	**Attribute**
15	Reserved	RO
14:12	Max Read Request Size	RW
11	Enable No Snoop	RW
10	AUX Power PM Enable	RW
9	Phantom Functions Enable	RW
8	Extended Tag Field Enable	RW
7:5	Max Payload Size	RW
4	Enable Relaxed Ordering	RW
3	Unsupported Request Reporting Enable	RW
2	Fatal Error Reporting Enable	RW
1	Non-Fatal Error Reporting Enable	RW
0	Correctable Error Reporting Enable	RW

5.2.1.41 Device Status Register

Address Offset:	7Ah	**Attribute:**	RO, RW1C
Default value:	0010h	**Size:**	16 bits

Bit	**Description**	**Attribute**
15:6	Reserved	RO
5	Transaction Pending	RO
4	AUX Power Detected	RO
3	Unsupported Request Detected	RW1C (Read, Write 1 to Clear)
2	Fatal Error Detected	RW1C
1	Non-Fatal Error Detected	RW1C
0	Correctable Error Detected	RW1C

5.2.1.42 Link Capabilities Register

Address Offset:	7Ch	**Attribute:**	RO
Default value:	0003 FC12h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:24	Port Number	RO
23:22	Reserved	RO
21	Link Bandwidth Notification Capability	RO
20	Data Link Layer Link Active Reporting Capable	RO
19	Surprise Down Error Reporting Capable	RO
18	Clock Power Management	RO
17:15	L1 Exit Latency L1 Exit Latency of FL1100 is more than 64us (111b)	RO
14:12	L0s Exit latency L0s Exit Latency of FL1100 is more than 4us (111b)	RO

11:10	ASPM Support FL1100 returns 11b to support ASPM L0s and L1	RO
9:4	Max Link Width FL1100 returns 000001b to indicate supporting of x1 link	RO
3:0	Supported Link Speeds FL1100 returns 0010b to indicate supporting of 5GT/s and 2.5GT/s	RO

5.2.1.43 Link Control Register

Address Offset:	80h	**Attribute:**	RW, RO
Default value:	0040h	**Size:**	16 bits

Bit	Description	Attribute
15:12	Reserved	RO
11	Link Autonomous Bandwidth Interrupt Enable	RW
10	Link Bandwidth Management Interrupt Enable	RW
9	Hardware Autonomous Width Disable	RW
8	Enable clock power management	RW
7	Extended Synch	RW
6	Common Clock Configuration	RW
5	Retrain Link	RW
4	Link Disable	RW
3	Read Completion Boundary (RCB)	RW
2	Reserved	
1:0	ASPM Control 00b: disable 01b: L0s enable 10b: L1 enable 11b: L0s and L1 enable	RW

5.2.1.44 Link Status Register

Address Offset:	82h	**Attribute:**	RO, RW1C
Default value:	1012h	**Size:**	16 bits

Bit	Description	Attribute
15	Link Autonomous Bandwidth Status	RW1C
14	Link Bandwidth Management Status	RW1C
13	Data Link Layer Link Active	RO
12	Set Clock Configuration	RO
11	Link Training	RO
10	Reserved	RO
9:4	Negotiated Link Width 000001b: x1	RO
3:0	Current Link Speed 0001: 2.5GT/s 0010: 5GT/s	RO

5.2.1.45 Device Capabilities 2 Register

Address Offset:	94h	**Attribute:**	RO

Default value:	0000 0010h	Size:	32 bits

Bit	Description	Attribute
31:24	Reserved	RO
23:22	Max End-End TLP Prefixes	RO
21	End-End TLP Prefix Supported	RO
20	Extended Fmt Field Supported	RO
13:12	TPH Completer Supported	RO
11	LTR Mechanism Supported	RO
10	No RO-enabled PR-PR Passing	RO
9	128-bit CAS Completer Supported	RO
8	64-bit AtomicOp Completer Supported	RO
7	32-bit AtomicOp Completer Supported	RO
6	AtomicOp Routing Supported	RO
5	ARI Forwarding Supported	RO
4	Completion Timeout Disable Supported	RO
3:0	Completion Timeout Ranges Supported	RO

5.2.1.46 Device Control 2 Register

Address Offset:	98h	Attribute:	RO
Default value:	0000h	Size:	16 bits

Bit	Description	Attribute
15	End-End TLK Prefix Blocking	RO
14:11	Reserved	RO
10	LTR Mechanism Enable	RO
9	IDO Completion Enable	RO
8	IDO Request Enable	RO
7	AtomicOp Egress Blocking	RO
6	AtomicOp Requester Enable	RO
5	ARI Forwarding Enable	RO
4	Completion Timeout Disable	RO
3:0	Completion Timeout Value	RO

5.2.1.47 Device Status 2 Register

Address Offset:	9Ah	Attribute:	RO
Default value:	0000h	Size:	16 bits

Bit	Description	Attribute
15:0	Reserved	RO

5.2.1.48 Link Capabilities 2 Register

Address Offset:	9Ch	Attribute:	RO
Default value:	0000 0000h	Size:	32 bits

Bit	Description	Attribute
31:0	Reserved	RO

5.2.1.49 Link Control 2 Register

Address Offset:	A0h	Attribute:	RWS, RO
Default value:	0002h	Size:	16 bits

Bit	Description	Attribute
15:13	Reserved	RO
12	Compliance De-emphasis	RWS
11	Compliance SOS	RWS
10	Enter Modified Compliance	RWS
9:7	Transmit Margin	RWS
6	Selectable De-emphasis	RO
5	Hardware Autonomous Speed Disable	RWS
4	Enter Compliance	RWS
3:0	Target Link Speed This field is read 0010b to indicate FL1100 support 5.0GT/s Target Link Speed	RWS

5.2.1.50 Link Status 2 Register

Address Offset:	A2h	Attribute:	RO
Default value:	0001h	Size:	16 bits

Bit	Description	Attribute
15:1	Reserved	RO
0	Current De-emphasis Level 1b: -3.5 dB; 0b:-6 dB	RO

5.2.1.51 MSI-X Capability ID

Address Offset:	B0h	Attribute:	RO
Default value:	11h	Size:	8 bits

Bit	Description	Attribute
7:0	Return 11h to indicate this is a MSI-X Capability Structure	RO

5.2.1.52 Next Capability Pointer

Address Offset:	B1h	Attribute:	RO
Default value:	00h	Size:	8 bits

Bit	Description	Attribute
7:0	Next Item Pointer Return 00h for the final item in the list.	RO

5.2.1.53 MSI-X Message Control Register

Address Offset:	B2h	Attribute:	RW, RO
Default value:	0007h	Size:	16 bits

Bit	Description	Attribute
15	MSI-X Enable	RW
14	Function Mask	RW

13:11	Reserved	RO
10:0	MSI-X Table Size	RO

5.2.1.54 MSI-X Table Offset and BIR Register

Address Offset:	B4h	**Attribute:**	RO
Default value:	0000 0002h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:3	Table Offset	RO
2:0	Table BIR (Bar Indicator Register)	RO

5.2.1.55 MSI-X PBA Offset and BIR Register

Address Offset:	B8h	**Attribute:**	RO
Default value:	0000 0004h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:3	PBA (Pending Bit Array) Offset	RO
2:0	PBA BIR	RO

5.3 Memory-Mapped I/O Register Map

5.3.1 Host Controller Capability Registers

These registers specify the limits and capabilities of the FL1100 USB 3.0 host controller implementation. All Capability Registers are Read-Only (RO). Please refer to section 5.3 of xHCI Specification Rev 1.0 for detail.

Table 5-3 Host controller capability registers

Register Symbol	Register Name	Base offset start	Base offset end	Default Value
CAPLENGTH	Capability Registers Length	00h	00h	80h
HCIVERSION	Host Controller Interface Version Number	02h	03h	0100h
HCSPARAMS1	Structural Parameters 1	04h	07h	08000820h
HCSPARAMS2	Structural Parameters 2	08h	0Bh	84000054h
HCSPARAMS3	Structural Parameters 3	0Ch	0Fh	00040001h
HCCPARAMS	Capability Parameters	10h	13h	200073E1h
DBOFF	Doorbell Offset	14h	17h	00003000h
RTSOFF	Runtime Register Space Offset	18h	1Bh	00002000h

5.3.1.1 CAPLENGTH - Capability Registers Length

Address Offset:	0h	**Attribute:**	RO
Default value:	80h	**Size:**	8 bits

Bit	Description	Attribute
7:0	Capability Registers Length (CAPLENGTH)	RO

This register is modified and maintained by BIOS

5.3.1.2 HCIVERSION - Host Controller Interface Version Number

Address Offset:	02h	**Attribute:**	RO
Default value:	0100h	**Size:**	16 bits

Bit	Description	Attribute
15:0	Host Controller Interface Version Number (HCIVERSION) FL1100 is compliant with xHCI version 1.0	RO

This register is modified and maintained by BIOS

5.3.1.3 HCSPARAMS1 - Structural Parameters 1

Address Offset:	04h	**Attribute:**	RO
Default value:	0800 0820h	**Size:**	32 bits

Bit	Description	Attribute
31:24	Number of ports (MaxPorts)	RO
23:19	Reserved	RO
18:8	Number of interrupters (MaxIntrs)	RO
7:0	Number of device slots (MaxSlots)	RO

This register is modified and maintained by BIOS

5.3.1.4 HCSPARAMS2 - Structural Parameters 2

Address Offset:	08h	Attribute:	RO
Default value:	8400 0054h	Size:	32 bits

Bit	Description	Attribute
31:27	Max Scratchpad Buffers (MaxScratchpadBufs)	RO
26	Scratchpad Restore (SPR)	RO
25:8	Reserved	RO
7:4	Event Ring Segment Table Max (ERSTMax)	RO
3:0	Isochronous Scheduling Threshold (IST)	RO

This register is modified and maintained by BIOS

5.3.1.5 HCSPARAMS3 - Structural Parameters 3

Address Offset:	0Ch	Attribute:	RO
Default value:	0004 0001h	Size:	32 bits

Bit	Description	Attribute
31:16	U2 Device Exit Latency (U2DEL). Worst case latency to transition a root hub Port Link Stat (PLS) from U2 to U0. Applies to all root hub ports. FL1100 has default set as Less than 4us.	RO
15:8	Reserved	RO
7:0	U1 Device Exit Latency (U1DEL) Worst case latency to transition a root hub Port Link Stat (PLS) from U2 to U0. Applies to all root hub ports. FL1100 has default set as Less than 1us.	RO

This register is modified and maintained by BIOS

5.3.1.6 HCCPARAMS - Capability Parameters

Address Offset:	10h	Attribute:	RO
Default value:	2000 73E1h	Size:	32 bits

Bit	Description	Attribute
31:16	xHCI Extended Capabilities Pointer (xECP)	RO
15:12	Maximum Primary Stream Array Size (MaxPSASize)	RO
11:8	Reserved	RO
7	No Secondary SID Support (NSS)	RO
6	Latency Tolerance Messaging Capability (LTC)	RO
5	Light HC Reset Capability (LHRC)	RO
4	Port Indicators (PIND)	RO
3	Port Power Control (PPC)	RO
2	Context Size (CSZ)	RO
1	BW Negotiation Capability (BNC)	RO
0	64-bit Addressing Capability (AC64)	RO

This register is modified and maintained by BIOS

5.3.1.7 DBOFF - Doorbell Offset

Address Offset:	14h	**Attribute:**	RO
Default value:	0000 3000h	**Size:**	32 bits

Bit	Description	Attribute
31:2	Doorbell Array Offset (DBAO)	RO
1:0	Reserved	RO

5.3.1.8 RTSOFF - Runtime Register Space Offset

Address Offset:	18	**Attribute:**	RO
Default value:	0000 2000h	**Size:**	32 bits

Bit	Description	Attribute
31:5	Runtime Register Space Offset (RTRSO)	RO
4:0	Reserved	RO

5.3.2 Host Controller Operational Registers

This section defines the xHCI Operational Registers. All registers are multiples of 32 bits in length. Unless otherwise stated, all registers should be accessed as a 32-bit width on reads using an appropriate software mask, if needed. A software read/modify/write mechanism should be invoked for partial writes. Please refer to section 5.4 of xHCI Specification Rev 1.0 for detail.

Table 5-4 Host controller operational registers

Register Symbol	Register Name	Base offset start	Base offset end	Default Value
USBCMD	USB Command	80h	83h	00000000h
USBSTS	USB Status	84h	87h	00000001h
PAGESIZE	Page Size	88h	8Bh	00000001h
DNCTRL	Device Notification Control	94h	97h	00000000h
CRCR_LO	Command Ring Low	98h	9Bh	00000000h
CRCR_HI	Command Ring High	9Ch	9Fh	00000000h
DCBAAP_LO	Device Context Base Address Array Pointer Low	B0h	B3h	00000000h
DCBAAP_HI	Device Context Base Address Array Pointer High	B4h	B7h	00000000h
CONFIG	Configure	B8h	BBh	00000000h
PORTSC0(USB2)	Port 0 Status and Control USB2	480h	483h	000002A0h
PORTPMSC0(USB2)	Port 0 Power Management Status and Control USB2	484h	487h	00000000h
PORTSC1(USB2)	Port 1 Status and Control USB2	490h	493h	000002A0h
PORTPMSC1(USB2)	Port 1 Power Management Status and Control USB2	494h	497h	00000000h
PORTSC2(USB2)	Port 2 Status and Control USB2	4A0h	4A3h	000002A0h
PORTPMSC2(USB2)	Port 2 Power Management Status and Control USB2	4A4h	4A7h	00000000h
PORTSC3(USB2)	Port 3 Status and Control USB2	4B0h	4B3h	000002A0h
PORTPMSC3(USB2)	Port 3 Power Management Status and Control USB2	4B4h	4B7h	00000000h
PORTSC0(USB3)	Port 0 Status and Control USB3	4C0h	4C3h	000002A0h
PORTPMSC0(USB3)	Port 0 Power Management Status and Control	4C4h	4C7h	00000000h
PORTLI0	Port 0 Link Info	4C8h	4CBh	00000000h
PORTSC1(USB3)	Port 1 Status and Control USB3	4D0h	4D3h	000002A0h
PORTPMSC1(USB3)	Port 1 Power Management Status and Control	4D4h	4D7h	00000000h
PORTLI1	Port 1 Link Info	4D8h	4DBh	00000000h
PORTSC2(USB3)	Port 2 Status and Control USB3	4E0h	4E3h	000002A0h
PORTPMSC2(USB3)	Port 2 Power Management Status and Control	4E4h	4E7h	00000000h
PORTLI2	Port 2 Link Info	4E8h	4EBh	00000000h
PORTSC3(USB3)	Port 3 Status and Control USB3	4F0h	4F3h	000002A0h
PORTPMSC3(USB3)	Port 3 Power Management Status and Control	4F4h	4F7h	00000000h
PORTLI3	Port 3 Link Info	4F8h	4FBh	00000000h

5.3.2.1 USBCMD - USB Command

Address Offset:	80h	**Attribute:**	RW, RO

Default value:	0000 0000h	Size:	32 bits

Bit	Description	Attribute
31:12	Reserved	RO
11	Enable U3 MFINDEX Stop (EU3S)	RW
10	Enable Wrap Event (EWE)	RW
9	Controller Restore State (CRS)	RW
8	Controller Save State (CSS)	RW
7	Light Host Controller Reset (LHCRST)	RW
6:4	Reserved	RO
3	Host System Error Enable (HSEE)	RW
2	Interrupter Enable (INTE)	RW
1	Host Controller Reset (HCRST)	RW
0	Run/Stop (RS)	RW

5.3.2.2 USBSTS - USB Status

Address Offset:	84h	Attribute:	RO, RW1C
Default value:	0000 0001h	Size:	32 bits

Bit	Description	Attribute
31:13	Reserved	RO
12	Host Controller Error (HCE) This bit is not preset in HC, this is deviation from xHCI 1.0 spec.	RO
11	Controller Not Ready (CNR) This is deviation from xHCI 1.0 spec.	RO
10	Save/Restore Error (SRE)	RW1C
9	Restore State Status (RSS)	RO
8	Save State Status (SSS)	RO
7:5	Reserved	RO
4	Port Change Detect (PCD)	RW1C
3	Event Interrupt (EINT)	RW1C
2	Host System Error (HSE)	RW1C
1	Reserved	RO
0	HCHalted (HCH)	RO

5.3.2.3 PAGESIZE - Page Size

Address Offset:	88h	Attribute:	RO
Default value:	0000 0001h	Size:	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Page Size (PAGESIZE)	RO

5.3.2.4 DNCTRL - Device Notification Control

Address Offset:	94h	Attribute:	RO, RW
Default value:	0000 0000h	Size:	32 bits

Bit	Description	Attribute

31:16	Reserved	RO
15:0	Notification Enable (N0_N15)	RW

5.3.2.5 CRCR_LO - Command Ring Low

Address Offset:	98h	**Attribute:**	RO, RW, RW1S
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:6	Command Ring Pointer (CRP)	RW
5:4	Reserved	RO
3	Command Ring Running (CRR)	RO
2	Command Abort (CA)	RW1S
1	Command Stop (CS)	RW1S
0	Ring Cycle State (RCS)	RW

5.3.2.6 CRCR_HI - Command Ring High

Address Offset:	9Ch	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Command Ring Pointer (CRP)	RW

5.3.2.7 DCBAAP_LO - Device Context Base Address Array Pointer Low

Address Offset:	B0h	**Attribute:**	RO, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:6	Device Context Base Address Array Pointer (DCBAAP)	RW
5:0	Reserved	RO

5.3.2.8 DCBAAP_HI - Device Context Base Address Array Pointer High

Address Offset:	B4h	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Device Context Base Address Array Pointer (DCBAAP)	RW

5.3.2.9 CONFIG – Configure

Address Offset:	B8h	**Attribute:**	RO, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:8	Reserved	RO
7:0	Max Device Slots Enabled (MaxSlotsEn)	RW

5.3.2.10 PORTSCx(USB2) - Port 0~3 Status and Control (USB2)

Address Offset:	Port 0: 480h Port 1: 490h	**Attribute:**	RO, RW, RWS, RW1S, RW1CS, ROS,

	Port 2: 4A0h Port 3: 4B0h		
Default value:	0000 02A0h	**Size:**	32 bits

Bit	Description	Attribute
31	Warm Port Reset (WPR)	RW1S
30	Device Removable (DR)	RO
29:28	Reserved	RO
27	Wake on Over-current Enable (WOE)	RWS
26	Wake on Disconnect Enable (WDE)	RWS
25	Wake on Connect Enable (WCE)	RWS
24	Cold Attach Status (CAS)	RO
23	Port Config Error Change (CEC)	RW1CS
22	Port Link State Change (PLC)	RW1CS
21	Port Reset Change (PRC)	RW1CS
20	Over-current Change (OCC)	RW1CS
19	Warm Port Reset Change (WRC)	RW1CS
18	Port Enabled Disabled Change (PEC)	RW1CS
17	Connect Status Change (CSC)	RW1CS
16	Port Link State Write Strobe (LWS)	RW
15:14	Port Indicator Control (PIC)	RWS
13:10	Port Speed (Port_Speed) This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 1: Full-speed 2: Low-speed 3: High-speed 3: SuperSpeed	ROS
9	Port Power (PP)	RWS
8:5	Port Link State (PLS) Read Value Meaning 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspend) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12:14 Reserved 15 Link is in the Resume State	RWS
4	Port Reset (PR) 1: Port Reset signaling is asserted.	RW1S

	0: Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated	
3	Over-current Active (OCA) This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.	ROS
2	Reserved	RO
1	Port Enabled/Disabled (PED) Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.	RW1CS
0	Current Connect Status (CCS) 1: Device is present on port. 0: No device is present.	ROS

5.3.2.11 PORTPMSCx(USB2) - Port 0~3 Power Management Status and Control (USB2)

Address Offset:	Port 0: 484h Port 1: 494h Port 2: 4A4h Port 3: 4B4h	**Attribute:**	RO, RWS, ROS
Default value:	0000 0000h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31:28	Port Test Control (PTC)	RWS
27:17	Reserved	RO
16	Hardware LPM Enable (HLE)	RO
15:8	L1 Device Slot (L1DS)	RWS
7:4	Host Initiated Resume Duration (HIRD)	RWS
3	Remote Wake Enable (RWE)	RWS
2:0	L1 Status (L1S)	ROS

5.3.2.12 PORTSCx(USB3) - Port 0~3 Status and Control (USB3)

Address Offset:	Port 0: 4C0h Port 1: 4D0h Port 2: 4E0h Port 3: 4F0h	**Attribute:**	RO, RWS, RW, RW1S, RW1CS, ROS
Default value:	0000 02A0h	**Size:**	32 bits

Bit	**Description**	**Attribute**
31	Warm Port Reset (WPR)	RW1S
30	Device Removable (DR)	RO
29:28	Reserved	RO
27	Wake on Over-current Enable (WOE)	RWS
26	Wake on Disconnect Enable (WDE)	RWS
25	Wake on Connect Enable (WCE)	RWS
24	Cold Attach Status (CAS)	RO
23	Port Config Error Change (CEC)	RW1CS
22	Port Link State Change (PLC)	RW1CS
21	Port Reset Change (PRC)	RW1CS

20	Over-current Change (OCC)	RW1CS
19	Warm Port Reset Change (WRC)	RW1CS
18	Port Enabled Disabled Change (PEC)	RW1CS
17	Connect Status Change (CSC)	RW1CS
16	Port Link State Write Strobe (LWS)	RW
15:14	Port Indicator Control (PIC)	RWS
13:10	Port Speed (Port_Speed) This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 1: Full-speed 2: Low-speed 3: High-speed 3: SuperSpeed	ROS
9	Port Power (PP)	RWS
8:5	Port Link State (PLS) Read Value Meaning 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspend) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12:14 Reserved 15 Link is in the Resume State	RWS
4	Port Reset (PR) 1: Port Reset signaling is asserted. 0: Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated	RW1S
3	Over-current Active (OCA) This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.	ROS
2	Reserved	RO
1	Port Enabled/Disabled (PED) Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag.	RW1CS
0	Current Connect Status (CCS) 1: Device is present on port. 0: No device is present.	ROS

5.3.2.13 PORTPMSCx(USB3) - Port 0-3 Power Management Status and Control (USB3)

Address Offset:	Port 0: 4C4h Port 1: 4D4h Port 2: 4E4h Port 3: 4F4h	**Attribute:**	RO, RWS, RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:17	Reserved	RO
16	Force Link PM Accept (FLA)	RW
15:8	U2 Timeout (U2TO)	RWS
7:0	U1 Timeout (U1TO)	RWS

5.3.2.14 PORTLIx - Port 0~3 Link Info (USB3)

Address Offset:	Port 0: 4C8h Port 1: 4D8h Port 2: 4E8h Port 3: 4F8h	**Attribute:**	RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Link Error Count (LEC)	RO

5.3.3 Host Controller Runtime Registers

This section defines the FL1100 xHCI Runtime Register space. All Runtime registers are multiples of 32 bits in length. Unless otherwise stated, all registers should be accessed with Dword references on reads, using an appropriate software mask if needed. A software read/modify/write mechanism should be invoked for partial writes. Software should write registers containing a Qword address field using only Qword references. Please refer to Section 5.5 of xHCI Specification Rev 1.0 for detail.

Table 5-5 Host controller runtime registers

Register Symbol	Register Name	Base offset start	Base offset end	Default Value
MFINDEX	Microframe Index	2000	2003	00000000h
IMAN1	Interrupter 1 Management	2020	2023	00000000h
IMOD1	Interrupter 1 Moderation	2024	2027	00000FA0h
ERSTSZ1	Event Ring 1 Segment Table Size	2028	202B	00000000h
ERSTBA_LO1	Event Ring 1 Segment Table Base Address Low	2030	2033	00000000h
ERSTBA_HI1	Event Ring 1 Segment Table Base Address High	2034	2037	00000000h
ERDP_LO1	Event Ring 1 Dequeue Pointer Low	2038	203B	00000000h
ERDP_HI1	Event Ring 1 Dequeue Pointer High	203C	203F	00000000h
IMAN2	Interrupter 2 Management	2040	2043	00000000h
IMOD2	Interrupter 2 Moderation	2044	2047	00000FA0h
ERSTSZ2	Event Ring 2 Segment Table Size	2048	204B	00000000h
ERSTBA_LO2	Event Ring 2 Segment Table Base Address Low	2050	2053	00000000h
ERSTBA_HI2	Event Ring 2 Segment Table Base Address High	2054	2057	00000000h
ERDP_LO2	Event Ring 2 Dequeue Pointer Low	2058	205B	00000000h
ERDP_HI2	Event Ring 2 Dequeue Pointer High	205C	205F	00000000h
IMAN3	Interrupter 3 Management	2060	2063	00000000h
IMOD3	Interrupter 3 Moderation	2064	2067	00000FA0h
ERSTSZ3	Event Ring 3 Segment Table Size	2068	206B	00000000h
ERSTBA_LO3	Event Ring 3 Segment Table Base Address Low	2070	2073	00000000h
ERSTBA_HI3	Event Ring 3 Segment Table Base Address High	2074	2077	00000000h
ERDP_LO3	Event Ring 3 Dequeue Pointer Low	2078	207B	00000000h
ERDP_HI3	Event Ring 3 Dequeue Pointer High	207C	207F	00000000h
IMAN4	Interrupter 4 Management	2080	2083	00000000h
IMOD4	Interrupter 4 Moderation	2084	2087	00000FA0h
ERSTSZ4	Event Ring 4 Segment Table Size	2088	208B	00000000h
ERSTBA_LO4	Event Ring 4 Segment Table Base Address Low	2090	2093	00000000h
ERSTBA_HI4	Event Ring 4 Segment Table Base Address High	2094	2097	00000000h
ERDP_LO4	Event Ring 4 Dequeue Pointer Low	2098	209B	00000000h
ERDP_HI4	Event Ring 4 Dequeue Pointer High	209C	209F	00000000h
IMAN5	Interrupter 5 Management	20A0	20A3	00000000h
IMOD5	Interrupter 5 Moderation	20A4	20A7	00000FA0h
ERSTSZ5	Event Ring 5 Segment Table Size	20A8	20AB	00000000h
ERSTBA_LO5	Event Ring 5 Segment Table Base Address Low	20B0	20B3	00000000h
ERSTBA_HI5	Event Ring 5 Segment Table Base Address High	20B4	20B7	00000000h
ERDP_LO5	Event Ring 5 Dequeue Pointer Low	20B8	20BB	00000000h

ERDP_HI5	Event Ring 5 Dequeue Pointer High	20BC	20BF	00000000h
IMAN6	Interrupter 6 Management	20C0	20C3	00000000h
IMOD6	Interrupter 6 Moderation	20C4	20C7	00000FA0h
ERSTSZ6	Event Ring 6 Segment Table Size	20C8	20CB	00000000h
ERSTBA_LO6	Event Ring 6 Segment Table Base Address Low	20D0	20D3	00000000h
ERSTBA_HI6	Event Ring 6 Segment Table Base Address High	20D4	20D7	00000000h
ERDP_LO6	Event Ring 6 Dequeue Pointer Low	20D8	20DB	00000000h
ERDP_HI6	Event Ring 6 Dequeue Pointer High	20DC	20DF	00000000h
IMAN7	Interrupter 7 Management	20E0	20E3	00000000h
IMOD7	Interrupter 7 Moderation	20E4	20E7	00000FA0h
ERSTSZ7	Event Ring 7 Segment Table Size	20E8	20EB	00000000h
ERSTBA_LO7	Event Ring 7 Segment Table Base Address Low	20F0	20F3	00000000h
ERSTBA_HI7	Event Ring 7 Segment Table Base Address High	20F4	20F7	00000000h
ERDP_LO7	Event Ring 7 Dequeue Pointer Low	20F8	20FB	00000000h
ERDP_HI7	Event Ring 7 Dequeue Pointer High	20FC	20FF	00000000h
IMAN8	Interrupter 8 Management	2100	2103	00000000h
IMOD8	Interrupter 8 Moderation	2104	2107	00000FA0h
ERSTSZ8	Event Ring 8 Segment Table Size	2108	210B	00000000h
ERSTBA_LO8	Event Ring 8 Segment Table Base Address Low	2110	2113	00000000h
ERSTBA_HI8	Event Ring 8 Segment Table Base Address High	2114	2117	00000000h
ERDP_LO8	Event Ring 8 Dequeue Pointer Low	2118	211B	00000000h
ERDP_HI8	Event Ring 8 Dequeue Pointer High	211C	211F	00000000h
DOORBELL1, ... 32	Door Bell 1, ..., 32	3000, ..., 307C	3003, ..., 307F	00000000h

5.3.3.1 MFINDEX - Microframe Index

Address Offset:	2000h	**Attribute:**	RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:14	Reserved	RO
13:0	Microframe Index (MI)	RO

5.3.3.2 IMANx - Interrupter x Management

There are 8 IMAN registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2020h-2023h x=2, 2040h-2043h x=3, 2060h-2063h … x=8, 2100h-2103h	**Attribute:**	RO, RW, RW1C
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:2	Reserved	RO
1	Interrupt Enable (IE)	RW

0	Interrupt Pending (Interrupt Pending)	RW1C

5.3.3.3 IMODx - Interrupter x Moderation

There are 8 IMOD registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2024h-2027h x=2, 2044h-2047h x=3, 2064h-2067h … x=8, 2104h-2107h	**Attribute:**	RW
Default value:	0000 0FA0h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Interrupt Moderation Counter (IMODC)	RW
15:0	Interrupt Moderation Interval (IMODI)	RW

5.3.3.4 ERSTSZx - Event Ring Segment Table Size x

There are 8 ERSTSZ registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2028h-202Bh x=2, 2048h-204Bh x=3, 2068h-206Bh … x=8, 2108h-210Bh	**Attribute:**	RW, RO
Default value:	00000000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	Reserved	RO
15:0	Event Ring Segment Table Size (ERSTS)	RW

5.3.3.5 ERSTBA_LOx - Event Ring Segment Table Base Address Low x

There are 8 ERSTBA_LO registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2030h-2033h x=2, 2050h-2053h x=3, 2070h-2073h … x=8, 2110h-2113h	**Attribute:**	RW, RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:6	Event Ring Segment Table Base Address Register (ERSTBA_LO)	RW
5:0	Reserved	RO

5.3.3.6 ERSTBA_HIx - Event Ring Segment Table Base Address High x

There are 8 ERSTBA_HI registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2034h-2037h x=2, 2054h-2057h	**Attribute:**	RW

	x=3, 2074h-2077h … x=8, 2114h-2117h		
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Event Ring Segment Table Base Address (ERSTBA_HI)	RW

5.3.3.7 ERDP_LOx - Event Ring Dequeue Pointer Low x

There are 8 ERDP_LO registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 2038h-203Bh x=2, 2058h-205Bh x=3, 2078h-207Bh … x=8, 2118h-211Bh	**Attribute:**	RW, RW1C
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:4	Event Ring Dequeue Pointer (ERDP)	RW
3	Event Handler Busy (EHB)	RW1C
2:0	Dequeue ERST Segment Index (DESI)	RW

5.3.3.8 ERDP_HIx - Event Ring Dequeue Pointer High x

There are 8 ERDP_HI registers: x = 1, 2, 3, …, 8.

Address Offset:	x=1, 203Ch-203Fh x=2, 205Ch-205Fh x=3, 207Ch-207Fh … x=8, 211Ch-211Fh	**Attribute:**	RW
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:0	Event Ring Dequeue Pointer (ERDP)	RW

5.3.3.9 DOORBELLx - Door Bell Registers x

There are 32 DOORBELL registers: x = 1, 2, 3,…, 32

Address Offset:	x=1, 3000h-3003h x=2, 3004h-3007h x=3, 3008h-300Bh … x=32, 307Ch-307Fh	**Attribute:**	RW, RO
Default value:	0000 0000h	**Size:**	32 bits

Bit	Description	Attribute
31:16	DB Stream ID (DBSID)	RW

15:8	Reserved	RO
7:0	DB Target (DBT)	RW

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Appendix A Mechanical

A.1 Package Outline

Please refer to Figure 10 and Figure 11 of this appendix.

A.2 Reference of Amkor PCB footprint

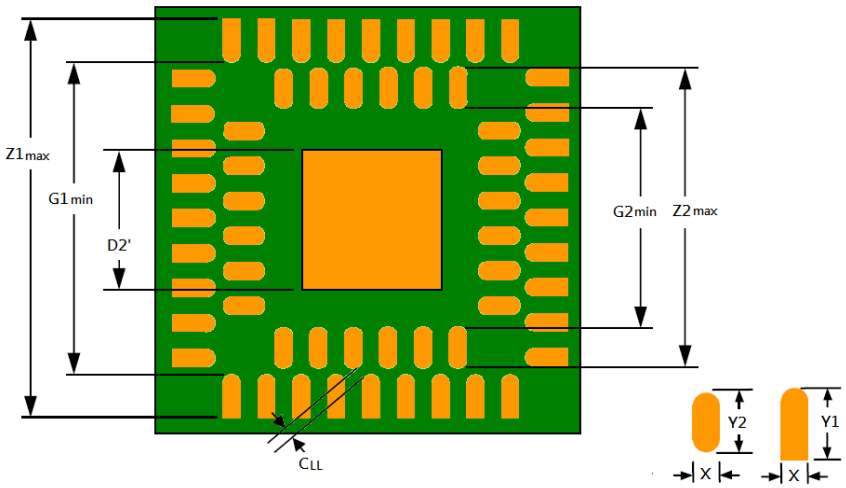


Figure 7 DRQFN PCB footprint

According to supplier Amkor's recommendation; the land width (X) for both inner and outer rows is needed (refer to Figure 7 above). Based on history of single row QFN, a lead width (X) of 0.280mm was chosen for 0.500mm pitch. Outer row land pattern dimension $Z1_{Max}$ is calculated using standard IPC methodology and expressed in terms of nominal body size dimension:

$$Z1_{Max} = D_{Min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$D_{Min} = BODYSIZE - \frac{C_L}{2}$$

$$Z1_{Max} = BODYSIZE + 0.340mm$$

For $G1_{Min}$ and $Z2_{Max}$ values, a minimum clearance of 0.200 mm between inner and outer leads must be maintained. For a 0.280 mm lead width and 0.650 mm row pitch, a spacing of 0.130 mm between the inner and outer row leads must be maintained (i.e. 1/2 ($G1_{Min}$ - $Z2_{Max}$) ≥ 0.13 mm). The nominal distance between package leads is 0.250 mm. Thus the extra 0.120 mm space for toe and heel fillets must be partitioned between the inner and outer leads. Because the toe fillet is more important to solder joint reliability, a design rule of $J_T \geq 2\ _{JH}$ is used (i.e. J_T = 0.080 mm, J_H = 0.040 mm). This results in the following:

$G1_{Min} = BODYSIZE - 0.880\ mm$

$Z2_{Max} = BODYSIZE - 1.140\ mm$

For G2Min dimension, the heel fillet is limited to conserve space for inner row vias between the leads and the thermal pad. A value similar to the toe fillet is chosen, JH = 0.080 mm. This results in the following:

$G2_{Min} = BODYSIZE - 2.260\ mm$

The individual lead dimensions derived from these values are:

Outer row leads: 0.280 x 0.610 mm

Inner row Lead: 0.280 x 0.560 mm

Figure 8 shows the land pattern in graphical format.

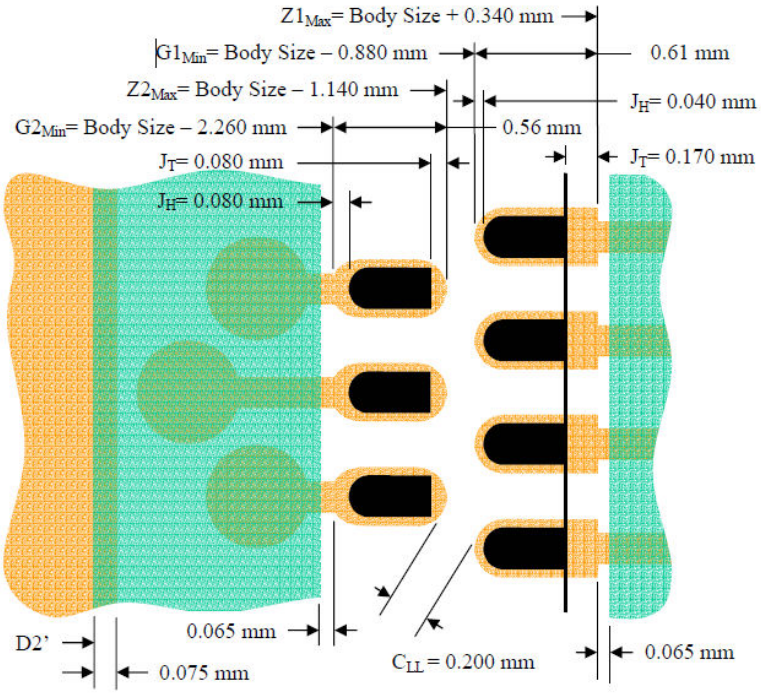


Figure 8 Land pattern of PCB for DRQFN

For some case, we can fine tune pad length for enough C_{LL} value in layout. Here is a PCB pad footprint that use on Fresco Logic's EVB for reference.

SYMBOL	PITCH VARIATION		
	MIN.	NOM.	MAX.
eT		0.50 BSC	
eR		0.715 BSC	
N		116	
NDa		16	
NDb		13	
NEa		16	
NEb		13	
La		0.61	
Lb		0.56	
b		0.28	
D2		**4.00**	
E2		**4.50**	

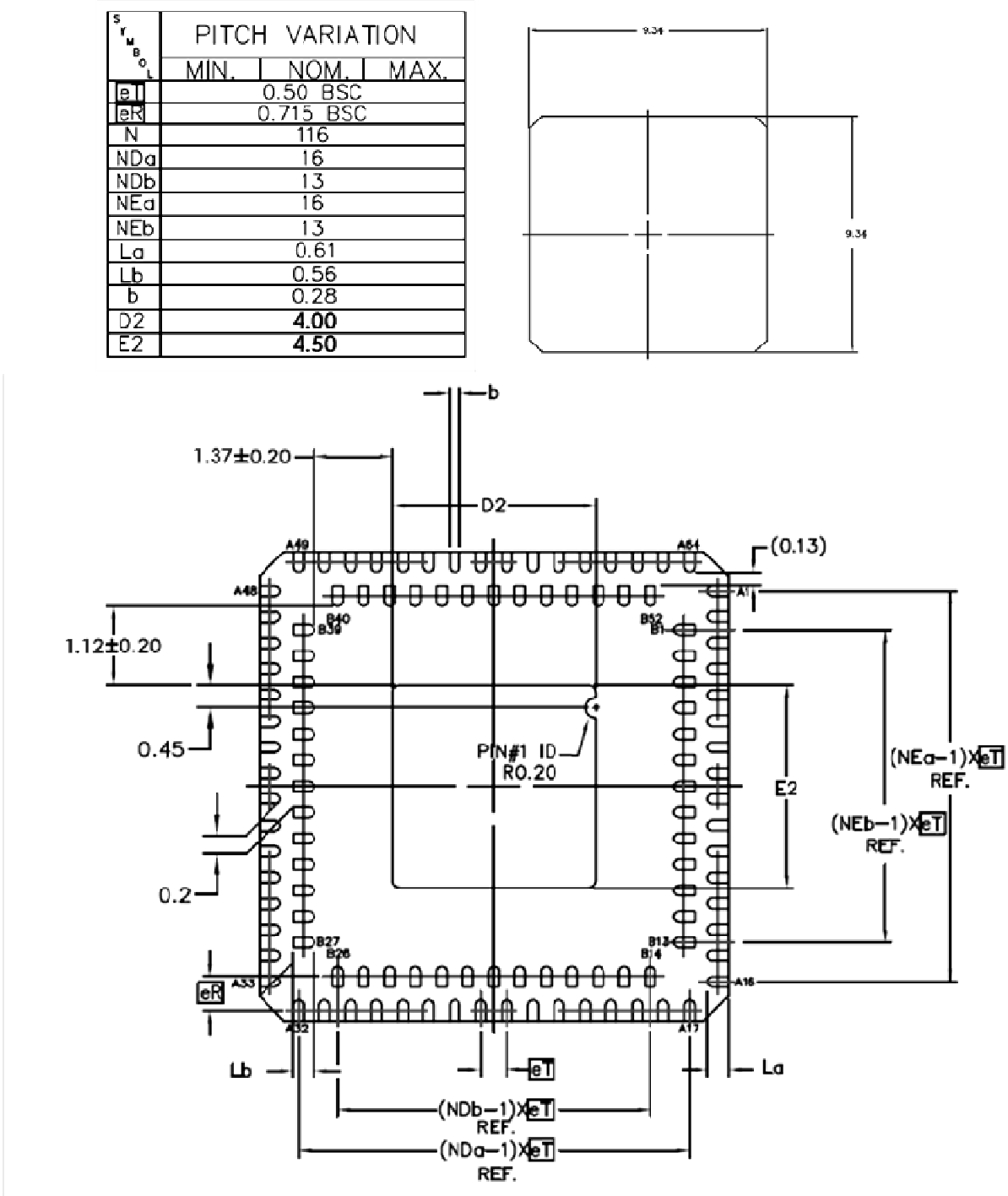
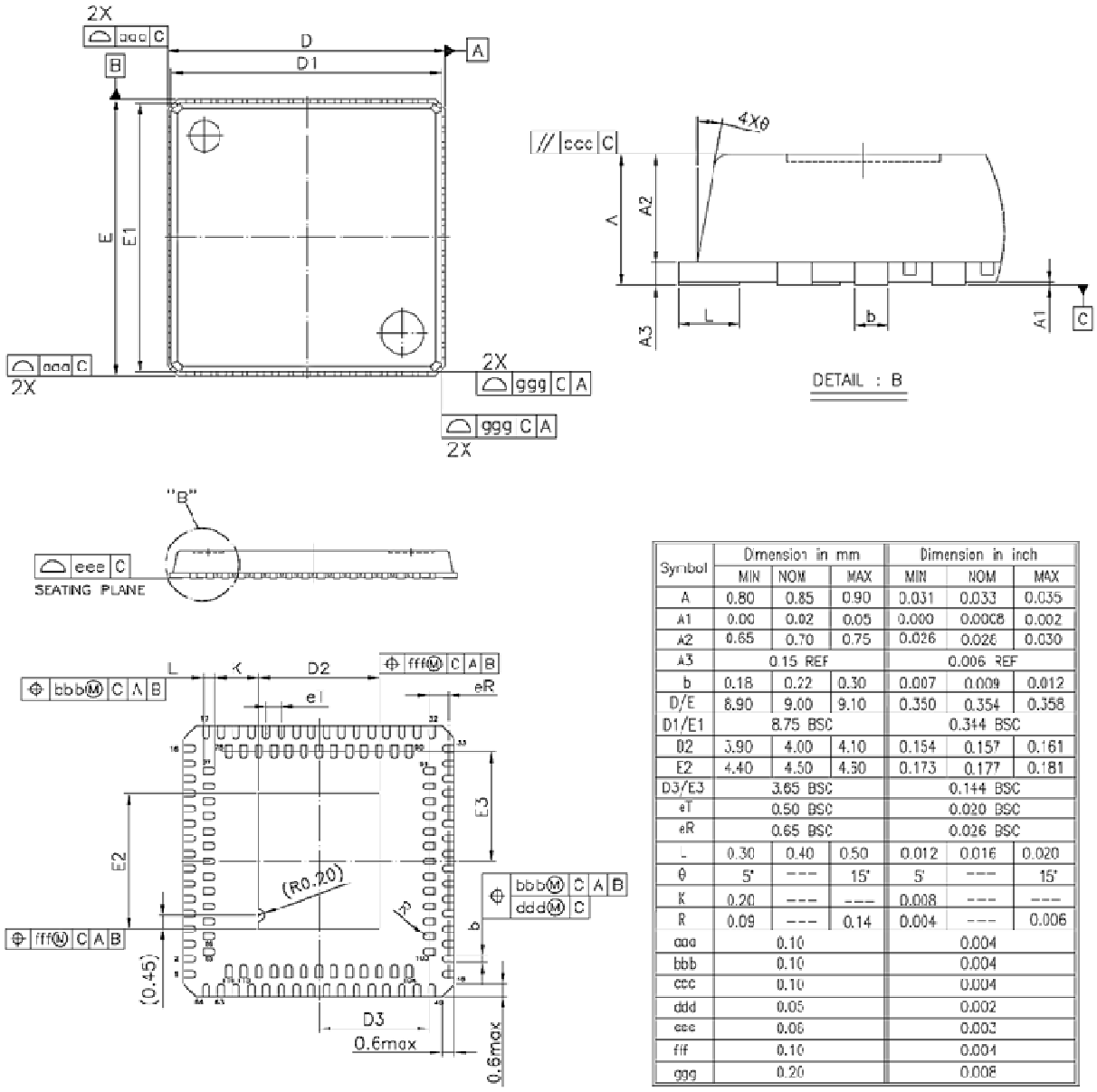
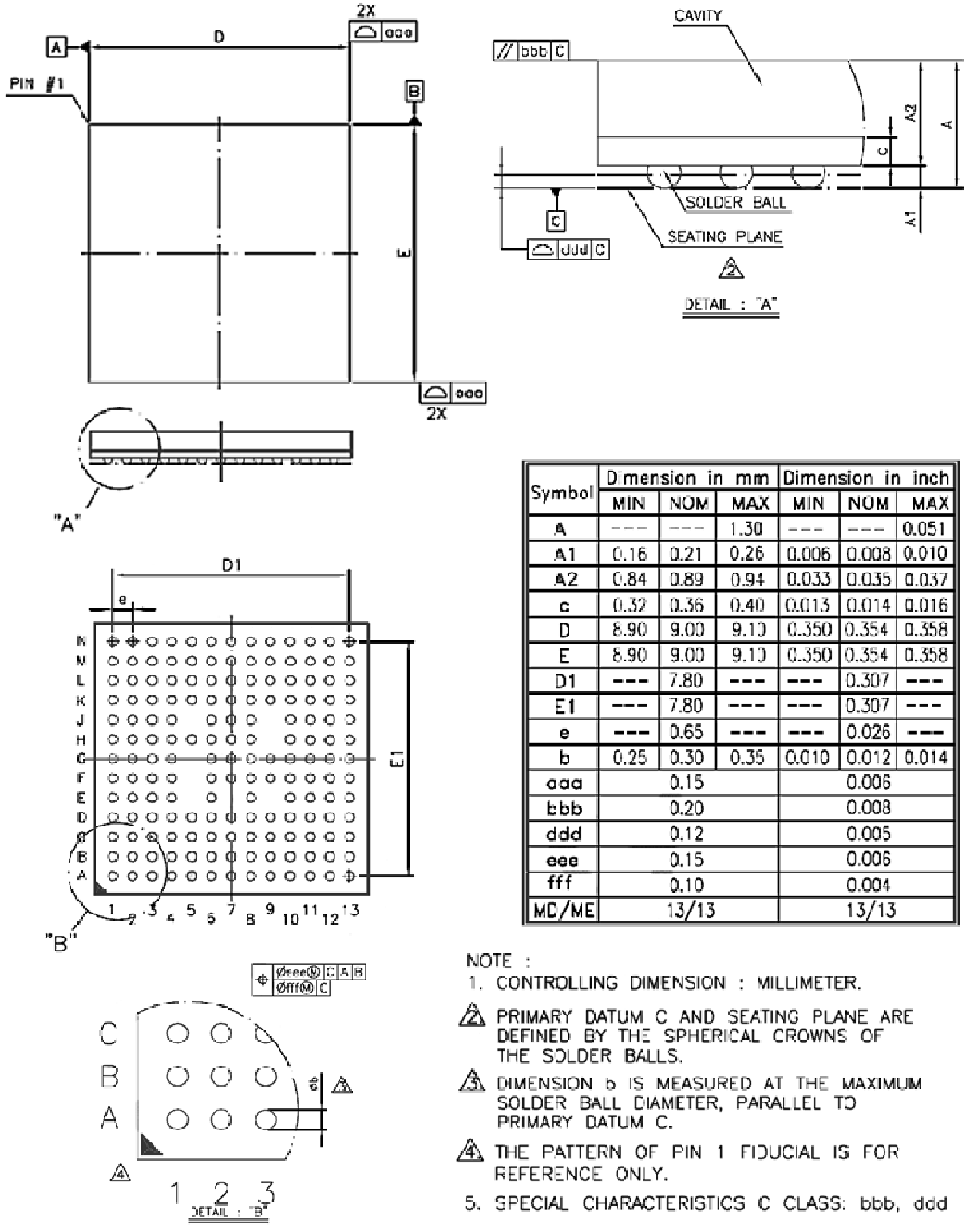


Figure 9 PCB Footprint of DRQFN



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	0.65	0.70	0.75	0.026	0.028	0.030
A3	0.15 REF			0.006 REF		
b	0.18	0.22	0.30	0.007	0.009	0.012
D/E	8.90	9.00	9.10	0.350	0.354	0.358
D1/E1	8.75 BSC			0.344 BSC		
D2	3.90	4.00	4.10	0.154	0.157	0.161
E2	4.40	4.50	4.60	0.173	0.177	0.181
D3/E3	3.65 BSC			0.144 BSC		
eT	0.50 BSC			0.020 BSC		
eR	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	5°	---	15°	5°	---	15°
K	0.20	---	---	0.008	---	---
R	0.09	---	0.14	0.004	---	0.006
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		
ggg	0.20			0.008		

Figure 10 DRQFN 116-pin 9x9mm package outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
D1	---	7.80	---	---	0.307	---
E1	---	7.80	---	---	0.307	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.10			0.004		
MD/ME	13/13			13/13		

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd

Figure 11 TFBGA 161-pin 9x9mm package outline

Appendix B Moisture Sensitive Level

LEVEL

3

FL1100 is a **MOISTURE SENSITIVE DEVICE** and should meet **LEVEL 3** requirements as following:

1. Calculated shelf life in sealed bag: 12 months at < 40 ℃ and < 90% RH.
2. After bag opened, devices that will be subjected to reflow solder or other high temperature process must be:
   a. Mounted within 168 hours of factory conditions ≦ 30℃/ 60% RH.
   b. Stored at < 10% RH.
3. Reflow condition: Please refer to IPC / JEDEC J-STD-020.
4. Devices required baking, before mounting if:
   a. Humidity indicator card is > 20% RH when read at 23 +/-5℃, or
   b. 2.a or 2.b is not met.
5. If baking is required, devices may be baked for 12 hours at 125+/-5℃.

Appendix C SMT Thermal Profile

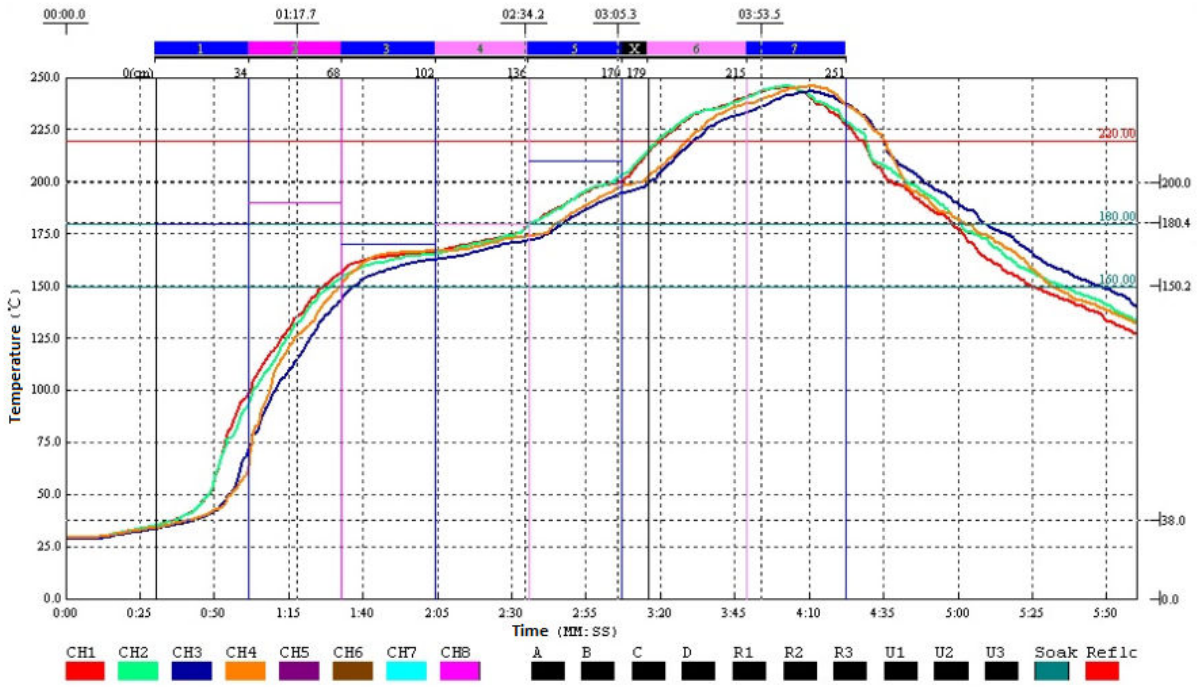


Figure 12 Thermal Profile on Fresco Logic's standard EVB

The soldering and void control in QFN package:

Quad Flat No Leads (QFN) package designs got more and more popular in electronic industry nowadays. The most challenges are in soldering and voiding control besides a number of benefits including (1) small size, such as a near die-sized footprint, thin profile, and light weight; (2) easy PCB trace routing due to the use of perimeter I/O pads; (3) reduced lead inductance; (4) easy PCB trace routing; and (5) good thermal and electrical performance due to the adoption of exposed copper die-pad technology. There are some attentions providing when using QFN package in design and SMT process to improve soldering and reduce voids.

1. QFN IC should by well packing due to it's a MSL 3 moisture sensitive component as defined by JTD-020 standard. The cleanness and roughness of pad of QFN will impact soldering.
2. Before SMT, bare PCB baking by 120 +/- 5˚C will help.
3. PCB design:
   - 3.1 Signal pad should use NSMD (Non Solder Mask Defined), die paddle should use SMD (Solder Mask Defined)
   - 3.2 Pad of PCB could be larger than pad of QFN, but limit is equal to.
   - 3.3 Pad of die paddle should match the dimension.
4. Stencil opening:
   - 4.1 Stencil thickness often use 0.1/ 0.12/ 0.13 mm for pitch 0.5 mm.

4.2 Signal pad & die paddle of stencil opening should match the dimensions.

4.3 Die paddle of stencil opening should be web shape to force a similar volume of solder paste to be deposited on all contacts for the QFN package. This is to prevent a stand-off situation where different solder paste heights on the Die Paddle and the Signal Pad contacts causes failure of some or all of the Signal Pad joints to form correctly.

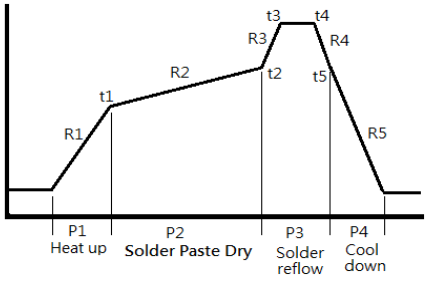
5. Depends on PCB size, trace layout & component numbers and package type to fine tune SMT thermal profile. And long hot SMT thermal profile will help improving soldering and reducing void issue.

5.1 Long: P2 (Solder Paste Dry area) should around 90 Sec, better > 90 Sec. refer to below diagram.

5.2 Hot: P3 area should > 220°C around 60 Sec, better > 60 Sec. Peak temp ≥ 243°C

5.3 Use thermal pad to measure temperature on “IC surface” to get temperature profile. If use measure on “bare PCB”, there are at least 5~10□ lower compared with actual product board while with all components.

5.4 Use Nitrogen process can improve SMT yield if available.



6. Solder cream (paste) type: high activity type will better.

7. Usage and storage of solder cream:

7.1 It should be well storage in 0~10˚C with well sealed.

7.2 Return to room temp should place 4 hrs before using.

7.3 When sealed is opened, the environment should controlled under 20~27˚C, 40~80%RH, within 1 hr. Then should return to 0~10˚C.

7.4 Stir solder cream at least 5 minutes.

8. All vias must be fully tented, especially those in the die paddle area and those close to the Signal Pad contacts.

9. Bow and warp spec of PCB should be careful defined.

10. Recommendations for QA engineering:

10.1 In-coming Inspection should pay special attention to the Bow and Warp characteristics of PCBs using this package;

10.2 Normal 2D X-Ray inspection will detect alignment issues between the QFN package and the PCB and can detect solder bridges easily and reliably. This technique will not adequately pick up solder deficiencies or improper wetting of solder pads. To find these types of defect, micro-sectioning of the solder joints is the usual preferred analytical method.

10.3 During the first few months of introduction of this package type, frequent sampling and destructive testing are strongly recommended to ensure good solder joints are being formed across normal variations in the manufacturing process. This is of particular significance for the solder joints at the corners of the package. Dependent upon facilities available, micro-sectioning along the center-lines of both Signal Pad contacts is preferred, but a lower-cost solution is to break the package from the PCB and visually inspect the joints with a microscope. This technique will pick up extreme failures, so occasional micro-sectioning is still recommended.

Please refer to Fresco Logic's "DRQFN package application reference" for more information.

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