August 2015

FL3100T
Low-Side Gate Driver with LED PWM Dimming Control for Smart LED Lighting

Features

- Non-inverting Input Logic with DIM Control Input for PWM Dimming Down to 0.1% for Hybrid Dimming
- 4.5 to 18 V Operating Range
- TTL Inputs Independent of Supply Voltage
- 2.5 A Sink / 1.8 A Source at V_{OUT} = 6 V
- Internal Resistors Turn Driver Off If No Inputs
- 13 ns Typical Rise Time and 9 ns Typical Fall-Time with 1 nF Load
- MillerDrive™ Technology
- Typical Propagation Delay Time Under 20 ns with Input Falling or Rising
- 6-Lead, 2 x 2 mm MLP or 5-Pin, SOT23 Packages
- Rated from -40°C to 125°C Ambient

Applications

- Smart LED Drivers with Accurate PWM Dimming
- General LED Lighting

Description

The FL3100T 2 A gate driver is designed to drive an N-channel enhancement-mode MOSFET in low-side switching applications by providing high peak current pulses during the short switching intervals. The FL3100T has two inputs that can be configured to operate in non-inverting (IN) mode with a DIM pin for PWM dimming control of the LED Driver. High accuracy PWM dimming control required in smart LED drivers is possible by adjusting the duty ratio of the DIM input. If one or both inputs are left unconnected, internal resistors bias the inputs such that the output is pulled LOW to hold the power MOSFET off.

The driver is available with fixed TTL input thresholds. Internal circuitry provides an under-voltage lockout function by holding the output LOW until the supply voltage is within operating range. The FL3100T delivers fast MOSFET switching performance, which helps maximize efficiency in high-frequency LED driver designs.

The FL3100T is available in a 5-pin, SOT23 or a 2 x 2 mm, 6-lead, Molded Leadless Package (MLP) for the smallest size with excellent thermal performance.

Typical Application Circuit

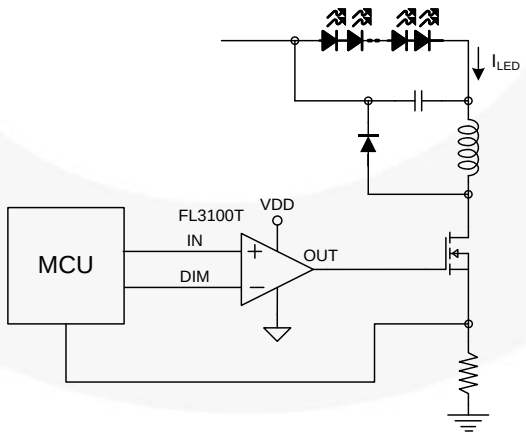

Figure 1. LED PWM Dimming Application Circuit for Smart LED Lighting

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Ordering Information

Part Number	Package	Packing Method	Quantity / Reel
FL3100TMPX	6-Lead, 2 x 2 mm MLP	Tape & Reel	3000
FL3100TSX	5-Pin, SOT23	Tape & Reel	3000

Block Diagrams

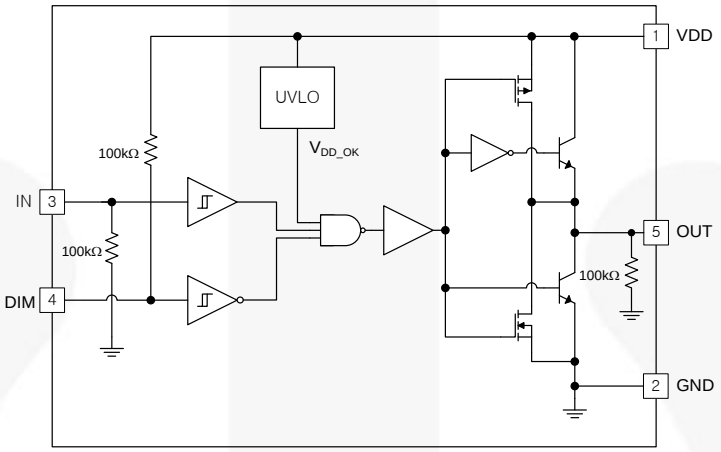

Figure 2. Simplified Block Diagram (SOT23 Pin-out)

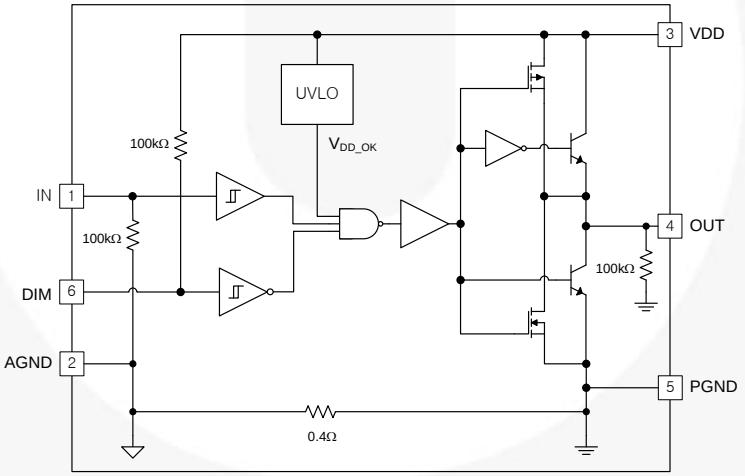

Figure 3. Simplified Block Diagram (MLP Pin-out)

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Functional Pin Configurations

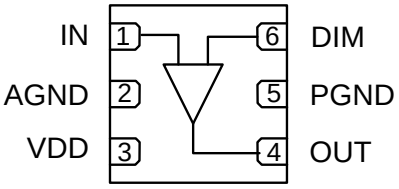

Figure 4. 6-Lead MLP (Top View)

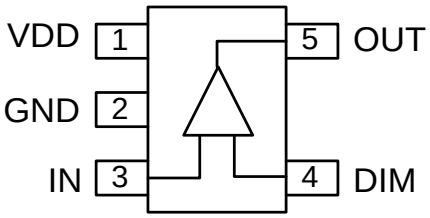

Figure 5. SOT23-5 (Top View)

Pin Definitions

SOT23 Pin #	MLP Pin #	Name	Pin Description
1	3	VDD	Supply Voltage. Provides power to the IC.
	2	AGND	Analog ground for input signals (MLP only). Connect to PGND underneath the IC.
2		GND	Ground (SOT-23 only). Common ground reference for input and output circuits.
3	1	IN	Input. Non-inverting logic. If IN is not used, connect to VDD to enable regular operation of the output.
4	6	DIM	Dimming Input. Used for PWM dimming. Inverting logic. If dimming is not used, connect to AGND or PGND to enable regular operation of the output.
5	4	OUT	Gate Drive Output: Held low unless required inputs are present and VDD is above UVLO threshold.
	Pad	P1	Thermal Pad (MLP only). Exposed metal on the bottom of the package, which is electrically connected to pin 5.
	5	PGND	Power Ground (MLP only). For output drive circuit; separates switching noise from inputs.

Output Logic

IN	DIM	OUT
0(1)	0	0
0(1)	1(1)	0
1	0	1
1	1(1)	0

Note:

1. Default input signal if no external connection is made.

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Thermal Characteristics[2]

Package	Θ_{JL}[3]	Θ_{JT}[4]	Θ_{JA}[5]	Unit
6-Lead, 2 x 2 mm Molded Leadless Package (MLP)	2.7	133.0	58.0	°C/W
SOT23-5	56	99	157	°C/W

Notes:

2. Estimates derived from thermal simulation; actual values depend on the application.
3. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
4. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
5. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2SP2 board, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	VDD to PGND	-0.3	20.0	V
V_{IN}	Voltage on IN and DIM to GND, AGND, or PGND	GND - 0.3	V_{DD} + 0.3	V
V_{OUT}	Voltage on OUT to GND, AGND, or PGND	GND - 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)		+260	ºC
T_J	Junction Temperature	-55	+150	ºC
T_{STG}	Storage Temperature	-65	+150	ºC

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{IN}	Input Voltage IN, DIM	0	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	ºC

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Electrical Characteristics

Unless otherwise noted, V_{DD} = 12 V, T_J = -40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Supply Current Inputs/ EN Not Connected			0.50	0.80	mA
V_{ON}	Turn-On Voltage		3.5	3.9	4.3	V
V_{OFF}	Turn-Off Voltage		3.3	3.7	4.1	V
Inputs						
V_{INL_T}	IN, DIM Logic LOW Voltage, Maximum		0.8			V
V_{INH_T}	IN, DIM Logic HIGH Voltage, Minimum				2.0	V
I_{IN}	Non-inverting Input	IN from 0 to V_{DD}	-1		175	µA
I_{DIMim}	DIM Input	IN from 0 to V_{DD}	-175		1	µA
V_{HYS}	IN, DIM Logic Hysteresis Voltage		0.2	0.4	0.8	V
Output						
I_{SINK}	OUT Current, Mid-Voltage, Sinking(6)	OUT at V_{DD}/2, C_{LOAD} = 0.1 µF, f = 1 kHz		2.5		A
I_{SOURCE}	OUT Current, Mid-Voltage, Sourcing(6)	OUT at V_{DD}/2, C_{LOAD} = 0.1 µF, f = 1 kHz		-1.8		A
I_{PK_SINK}	OUT Current, Peak, Sinking(6)	C_{LOAD} = 0.1 µF, f = 1 kHz		3		A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing(6)	C_{LOAD} = 0.1 µF, f = 1 kHz		-3		A
t_{RISE}	Output Rise Time(7)	C_{LOAD} = 1000 pF		13	20	ns
t_{FALL}	Output Fall Time(7)	C_{LOAD} = 1000 pF		9	14	ns
t_{D1}, t_{D2}	Output Prop. Delay, TTL Inputs(7)	0 – 5 V_{IN}; 1 V/ns Slew Rate	9	16	30	ns
I_{RVS}	Output Reverse Current Withstand(6)			500		mA

Notes:

6. Not tested in production.
7. *See Timing Diagrams of Figure 6 and Figure 7*.

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Timing Diagrams

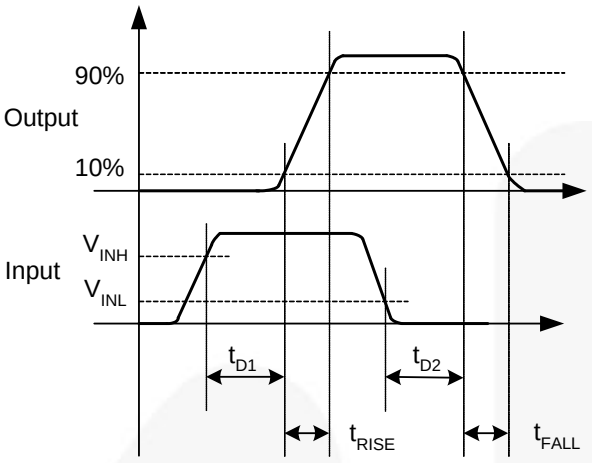

Figure 6. IN Pin

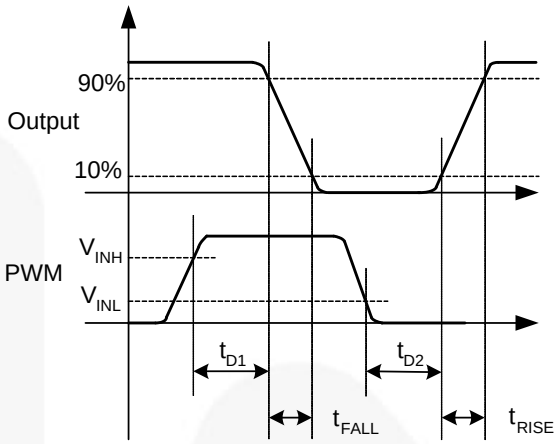

Figure 7. DIM Pin

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

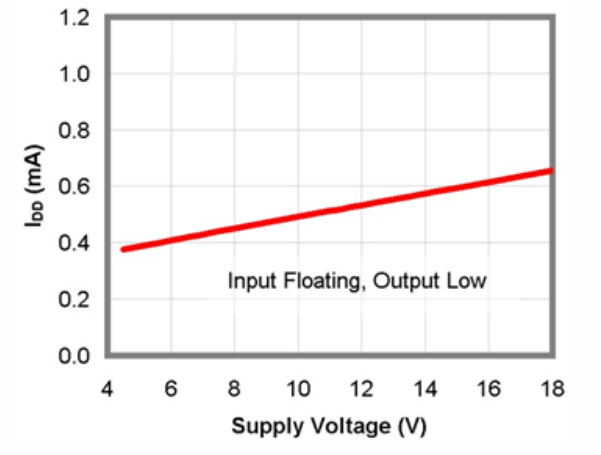

Figure 8. I_{DD} (Static) vs. Supply Voltage

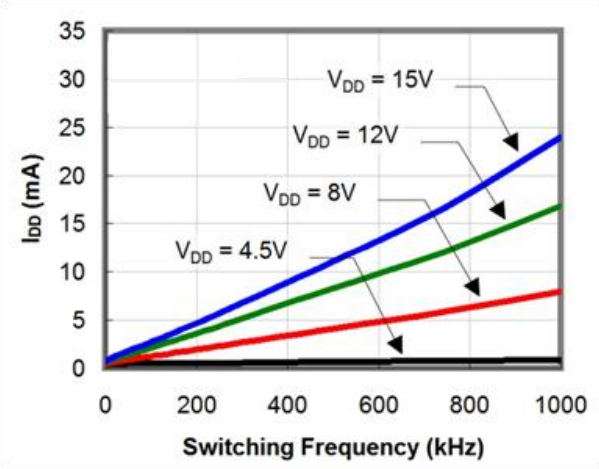

Figure 9. I_{DD} (No-Load) vs. Frequency

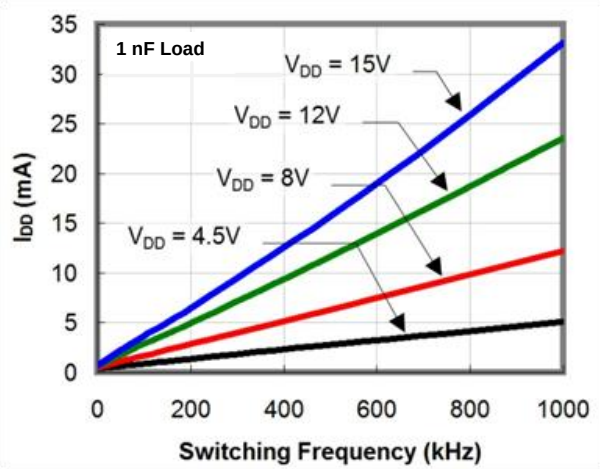

Figure 10. I_{DD} (1 nF Load) vs. Frequency

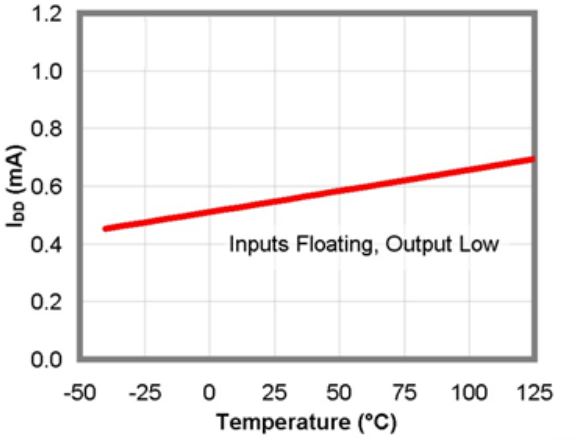

Figure 11. I_{DD} (Static) vs. Temperature

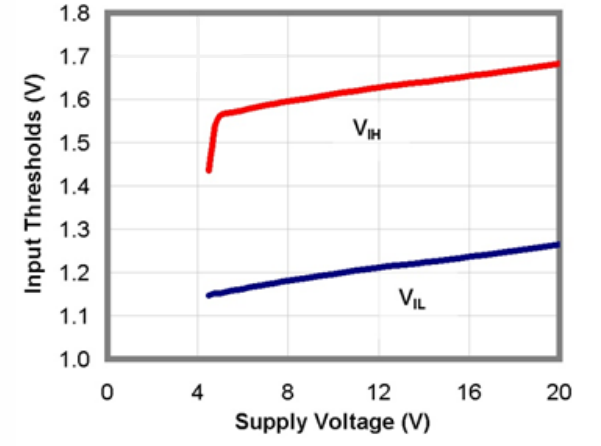

Figure 12. Input Thresholds vs. Supply Voltage

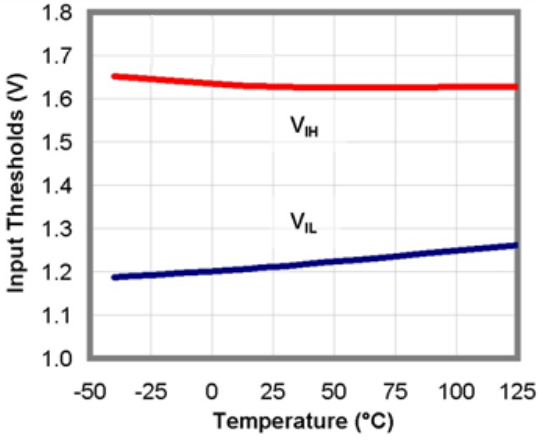

Figure 13. TTL Input Thresholds vs. Temperature

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Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

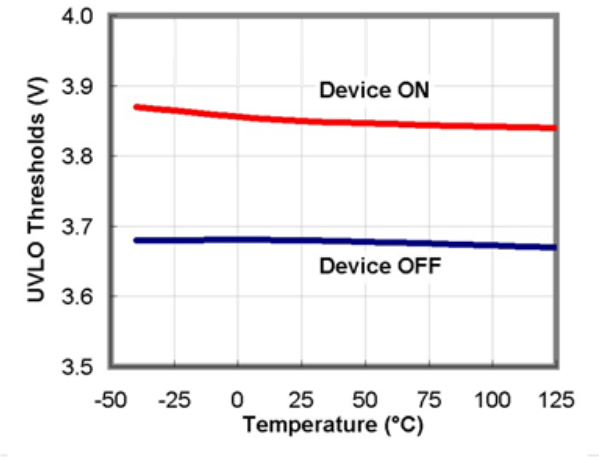

Figure 14. UVLO Thresholds vs. Temperature

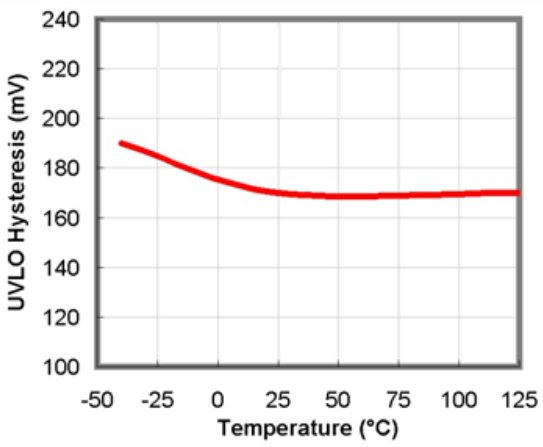

Figure 15. UVLO Hysteresis vs. Temperature

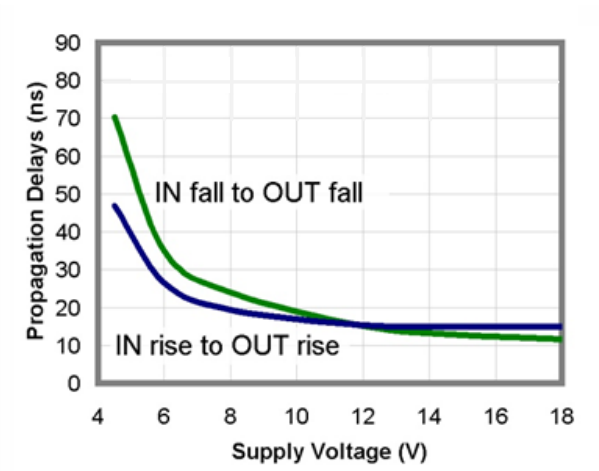

Figure 16. Propagation Delay vs. Supply Voltage

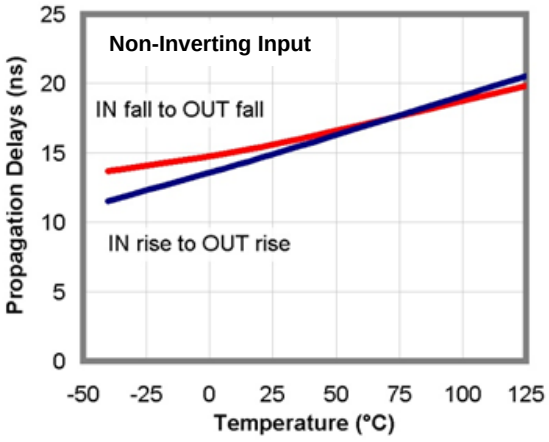

Figure 17. Propagation Delay vs. Temperature

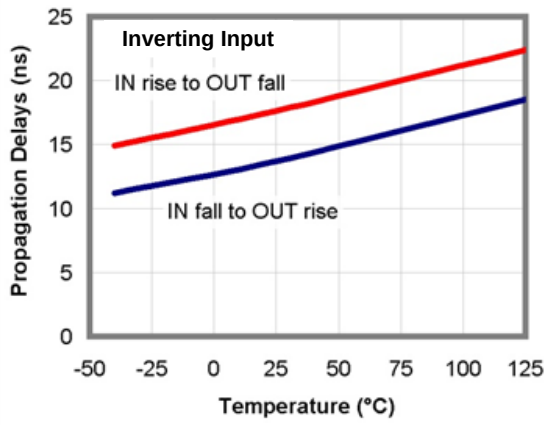

Figure 18. Propagation Delay vs. Temperature

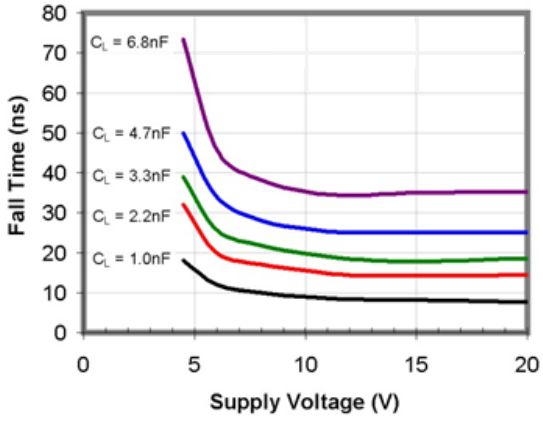

Figure 19. Fall Time vs. Supply Voltage

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

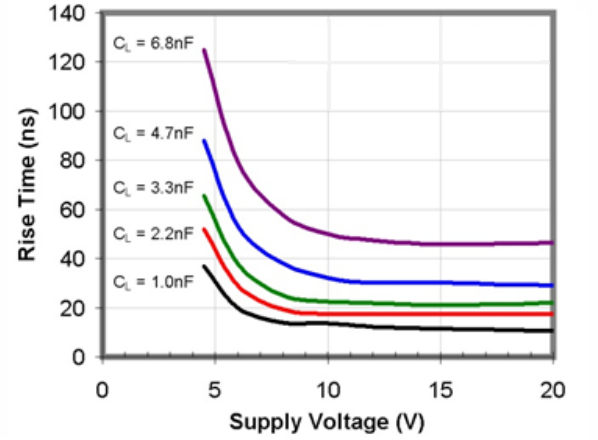

Figure 20. Rise Time vs. Supply Voltage

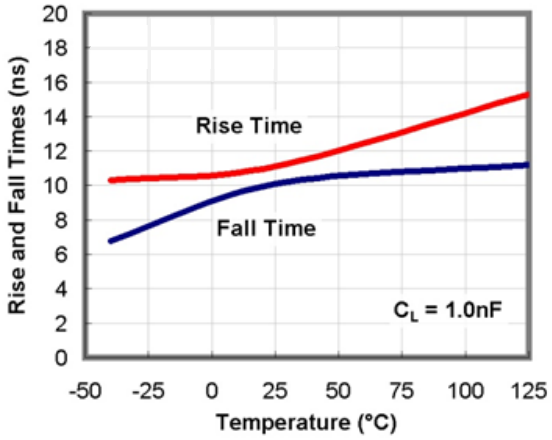

Figure 21. Rise and Fall Time vs. Temperature

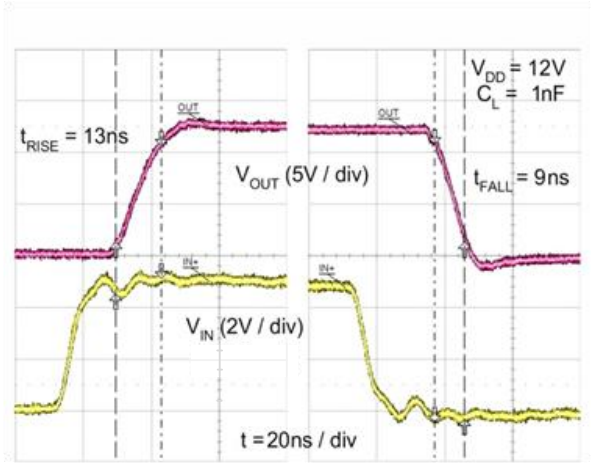

Figure 22. Rise / Fall Waveforms with 1 nF Load

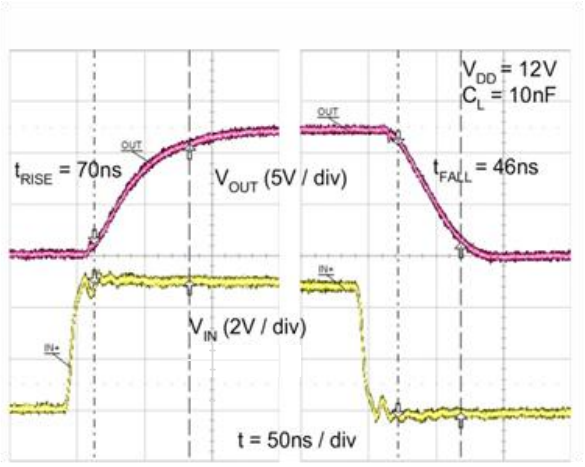

Figure 23. Rise / Fall Waveforms with 10 nF Load

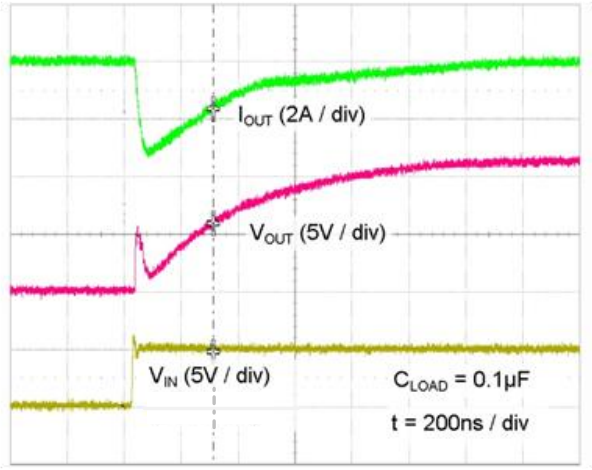

Figure 24. Quasi-Static Source Current with V_{DD}=12 V

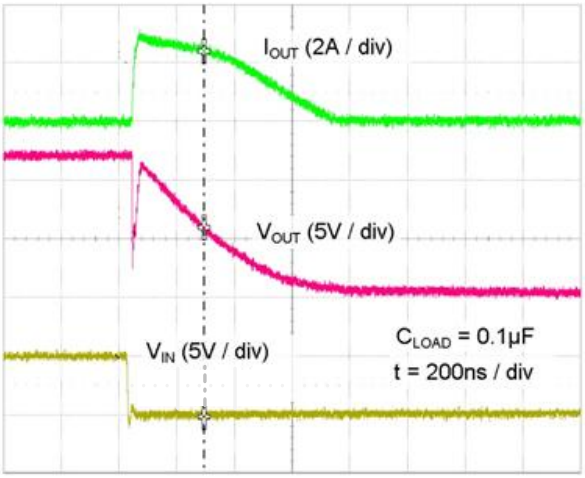

Figure 25. Quasi-Static Sink Current with V_{DD}=12 V

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

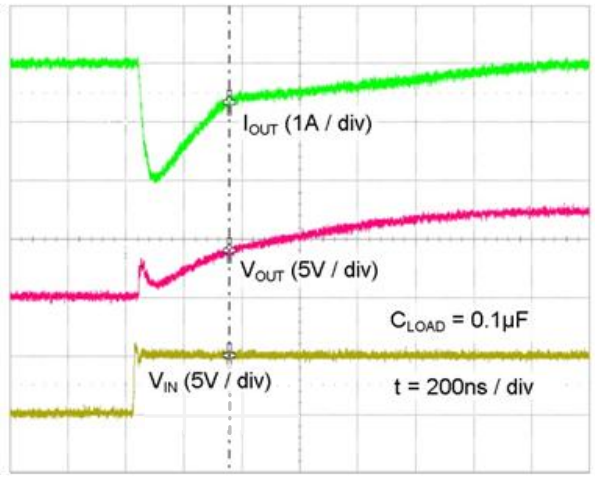

Figure 26. Quasi-Static Source Current with V_{DD}=8 V

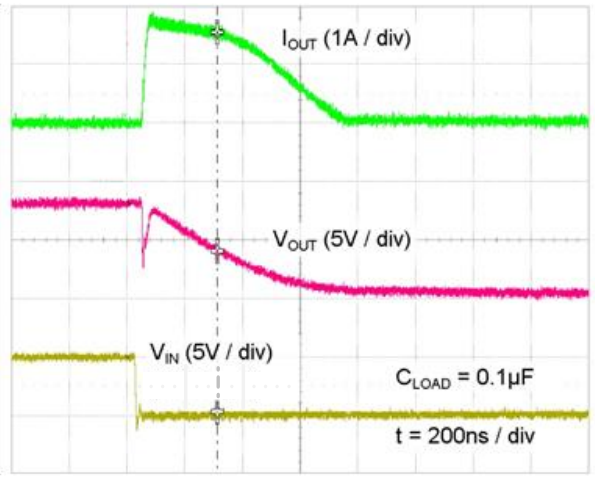

Figure 27. Quasi-Static Sink Current with V_{DD}=8 V

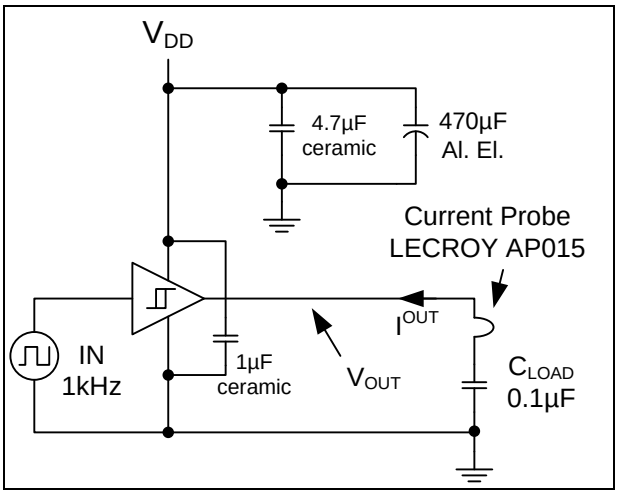

Figure 28. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

Applications Information

PWM Dimming

FL3100T is used for pulse-width modulation of the LED current to control the amount of light produced by the LED in MCU-driven hybrid dimming applications.

There are two factors to consider, $PWM_{amplitude}$ controls the LED light output by reducing the forward current in the LED and PWM_{light} controls the on time of forward current in the LED.

In the typical application circuit, Figure 1 and repeated here Figure 29, IN is connected to the $PWM_{amplitude}$ signal coming out of the MCU to control the amplitude of the overall LED current. This $PWM_{amplitude}$ signal from the MCU is the same PWM signal based on the switching frequency of the power stage and error signal in a closed loop LED driver stage.

DIM is connected to a different PWM signal, also from the MCU, but is usually a lower frequency signal to command the PWM_{light} dimming on the LED current, i.e. ~1 kHz and can be commanded from a wired or wireless interface such as DALI or ZigBee. Therefore, mixed mode dimming using both amplitude and PWM dimming on the LED current is possible.

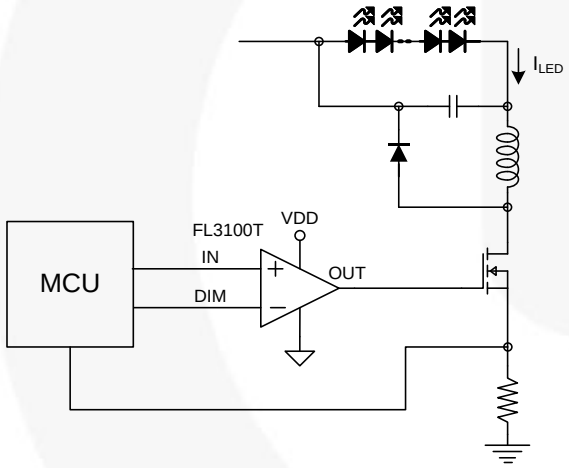

Figure 29. LED PWM Dimming Application

During amplitude dimming ($PWM_{amplitude}$), DIM stays low and there is no PWM_{light} dimming. When PWM_{light} dimming becomes active, e.g. below 20% of amplitude ($PWM_{amplitude}$) dimming, then amplitude dimming is held constant and PWM_{light} dimming is used to reduce the light output down to ~0.1% accurately. Figure 30 shows a possible implementation for mixed mode dimming.

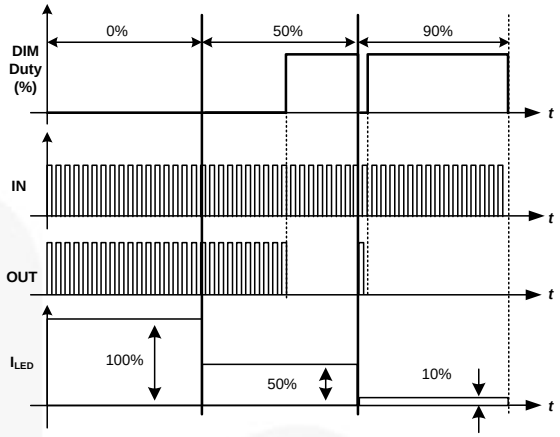

Figure 30. LED Current with PWM Dimming

Input Thresholds

In the FL3100T, the input thresholds meet industry-standard TTL logic thresholds, independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/µs or faster, so the rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

Static Supply Current

In the I_{DD} (static) typical performance graphs (Figure 8, and Figure 11), the curve is produced with all inputs floating (OUT is LOW) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagrams *(see Figure 2 - Figure 3).* In these cases, the actual static I_{DD} current is the value obtained from the curves plus this additional current.

Under-Voltage Lockout (UVLO)

The FL3100T startup logic is optimized to drive ground referenced N-channel MOSFETs with an Under-Voltage Lockout (UVLO) function to ensure that the IC starts up in an orderly fashion. When V_{DD} is rising, yet below the 3.9 V operational level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P-channel MOSFETs because the low output voltage of the driver would turn the P-channel MOSFET on with V_{DD} below 3.9 V.

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VDD Bypass Capacitor Guidelines

To enable this IC to turn a power device on quickly, a local, high-frequency, bypass capacitor C_{BYP} with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 µF to 47 µF often found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply ≤5%. Often this is achieved with a value ≥ 20 times the equivalent load capacitance C_{EQV}, defined here as Q_{gate}/V_{DD}. Ceramic capacitors of 0.1 µF to 1 µF or larger are common choices, as are dielectrics, such as X5R and X7R, which have good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50-100 times the C_{EQV}, or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10 nF, mounted closest to the VDD and GND pins to carry the higher-frequency components of the current pulses.

MillerDrive™ Gate Drive Technology

FL3100T drivers incorporate the MillerDrive™ architecture shown in Figure 31 for the output stage, a combination of bipolar and MOS devices capable of providing large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive™ architecture is to speed up switching by providing the highest current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but if a slower rise or fall time at the MOSFET gate is needed, a series resistor can be added.

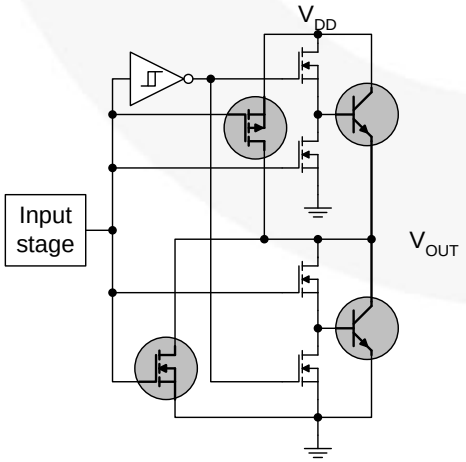

Figure 31. MillerDrive™ Output Architecture

Layout and Connection Guidelines

The FL3100T incorporates fast-reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 2 A to facilitate voltage transition times from under 10 ns to over 100 ns. The following layout and connection guidelines are strongly recommended:

- Keep high-current output and power ground paths separate from logic input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds.
- Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while reducing the loop area that can radiate EMI to the driver inputs and other surrounding circuitry.
- The FL3100T is available in two packages with slightly different pinouts, offering similar performance. In the 6-pin MLP package, Pin 2 is internally connected to the input analog ground and should be connected to power ground, Pin 5, through a short direct path underneath the IC. In the 5-pin SOT23, the internal analog and power ground connections are made through separate, individual bond wires to Pin 2, which should be used as the common ground point for power and control signals.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be especially obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn-on and turn-off current paths should be minimized as discussed in the following sections.

Figure 32 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak current pulses within this driver-MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

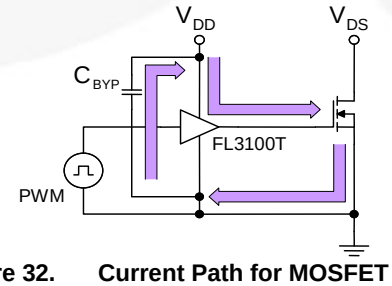

Figure 32. Current Path for MOSFET Turn-On

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Figure 33 shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn-off times, the resistance and inductance in this path should be minimized.

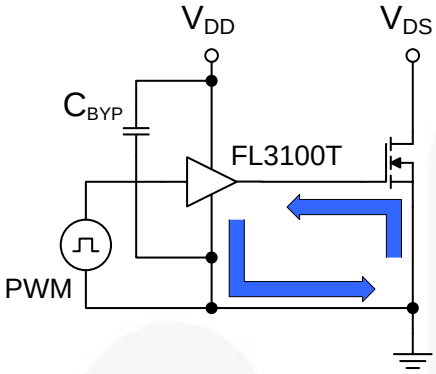


Figure 33. Current Path for MOSFET Turn-Off

Table 1. Truth Table of Logic Operation

The truth table indicates the operational states using the IN and DIM pins.

IN	DIM	OUT
0	0	0
0	1	0
1	0	1
1	1	0

If the DIM pin is connected to logic HIGH, a disable function is realized, and the driver output remains LOW regardless of the state of the IN pin. Likewise, If the IN pin is connected to logic LOW, a disable function is realized, and the driver output remains LOW regardless of the state of the DIM pin.

Operational Waveforms

At power up, the driver output remains LOW until the V_{DD} voltage reaches the turn-on threshold. The magnitude of the OUT pulses rises with V_{DD} until steady-state V_{DD} is reached. The non-inverting operation illustrated in Figure 34 shows that the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input.

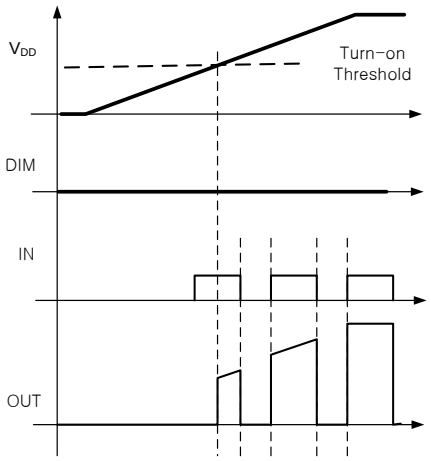


Figure 34. IN Startup Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components; P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad (1)$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \bullet V_{GS} \bullet f_{SW} \quad (2)$$

Dynamic Pre-drive / Shoot-through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors, can be obtained using the *I_{DD} (no-Load) vs. Frequency* graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \bullet V_{DD} \quad (3)$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming Ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \bullet \Psi_{JB} + T_B \quad (4)$$

where:

T_J = driver junction temperature

Ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation

T_B = board temperature in location defined in the Thermal Characteristics table.

In a typical MOSFET gate drive application, the FDS2672 would be a potential MOSFET selection. The typical gate charge would be 32 nC with $V_{GS} = V_{DD} =$ 10 V. Using a TTL input driver at a switching frequency of 500 kHz, the total power dissipation can be calculated as:

$$P_{GATE} = 32\ nC \bullet 10\ V \bullet 500\ kHz = 0.160\ W \quad (5)$$

$$P_{DYNAMIC} = 8\ mA \bullet 10\ V = 0.080\ W \quad (6)$$

$$P_{TOTAL} = 0.24\ W \quad (7)$$

The 5-pin SOT23 has a junction-to-lead thermal characterization parameter $\Psi_{JB} = 51°C/W$.

In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation (4) determines the board temperature required to maintain the junction temperature below 120°C:

$$T_{B,MAX} = T_J - P_{TOTAL} \bullet \Psi_{JB} \quad (8)$$

$$T_{B,MAX} = 120°C - 0.24W \bullet 51°C/W = 108°C \quad (9)$$

For comparison purposes, replace the 5-pin SOT23 used in the previous example with the 6-pin MLP package with $\Psi_{JB} = 2.8°C/W$. The 6-pin MLP package can operate at a PCB temperature of 119°C, while maintaining the junction temperature below 120°C. This illustrates that the physically smaller MLP package with thermal pad offers a more conductive path to remove the heat from the driver. Consider the tradeoffs between reducing overall circuit size with junction temperature reduction for increased reliability.

Typical Application Diagram

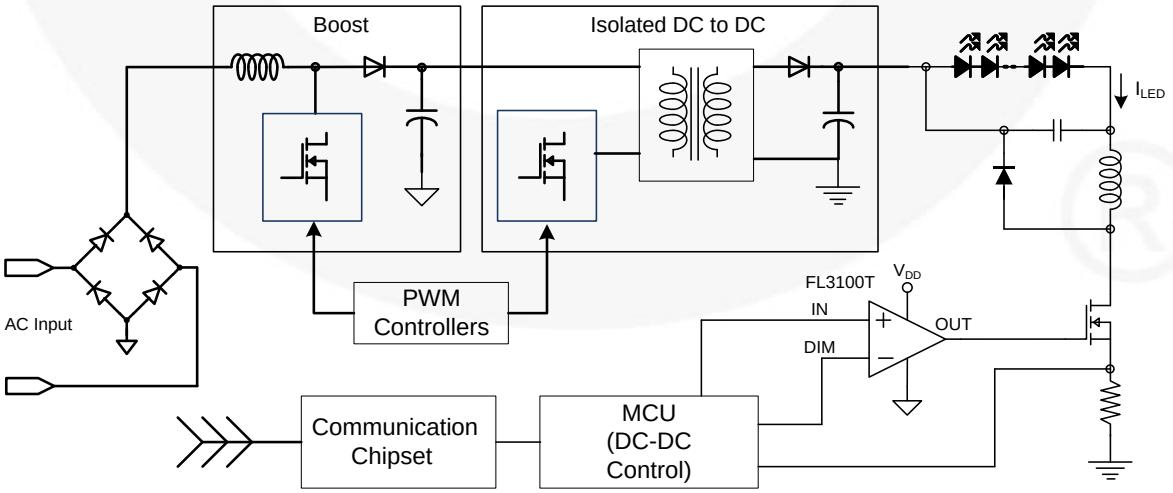
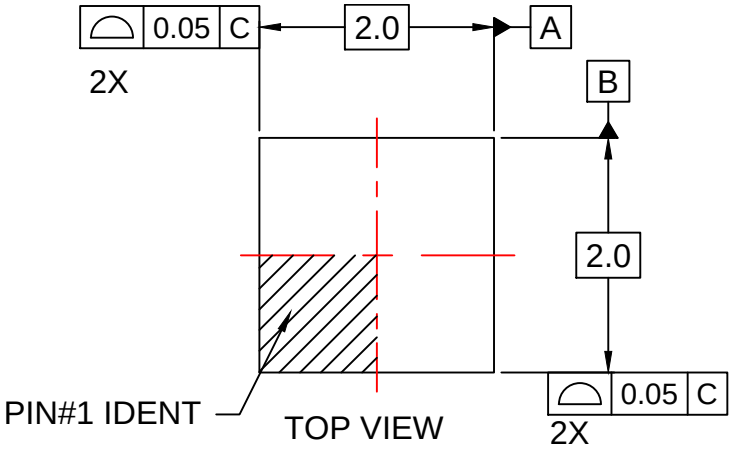
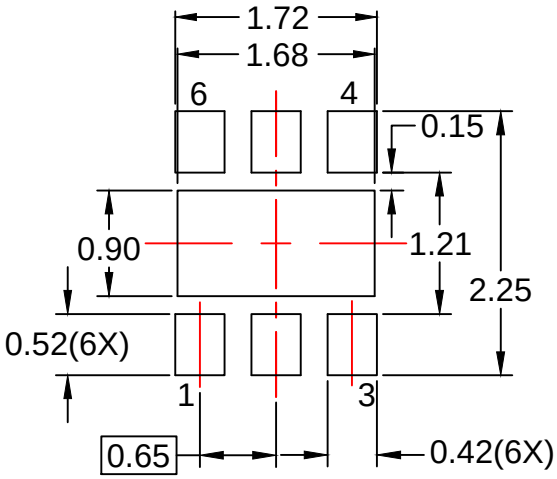


Figure 35. Smart LED Driver using the MCU and FL3100T in the Buck DC-DC Stage





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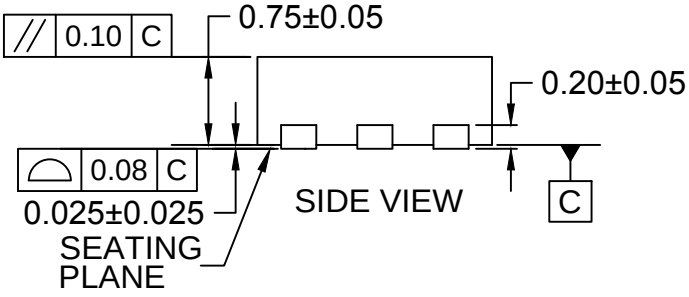

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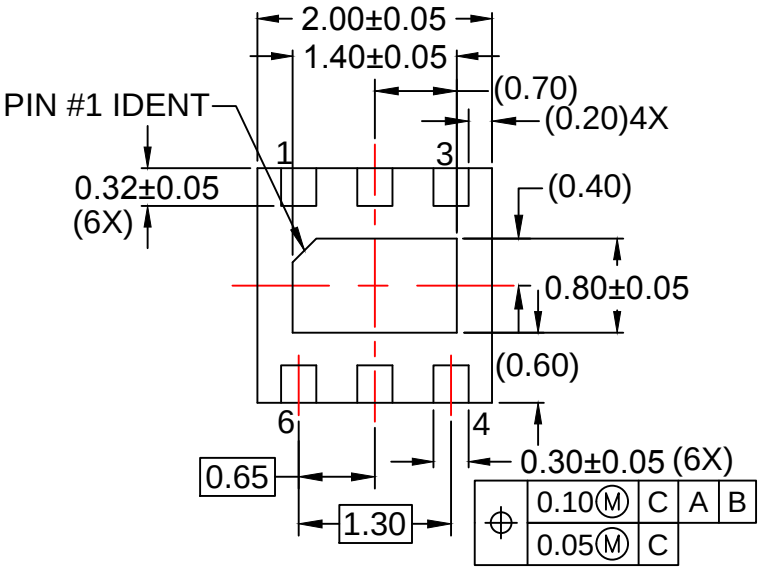

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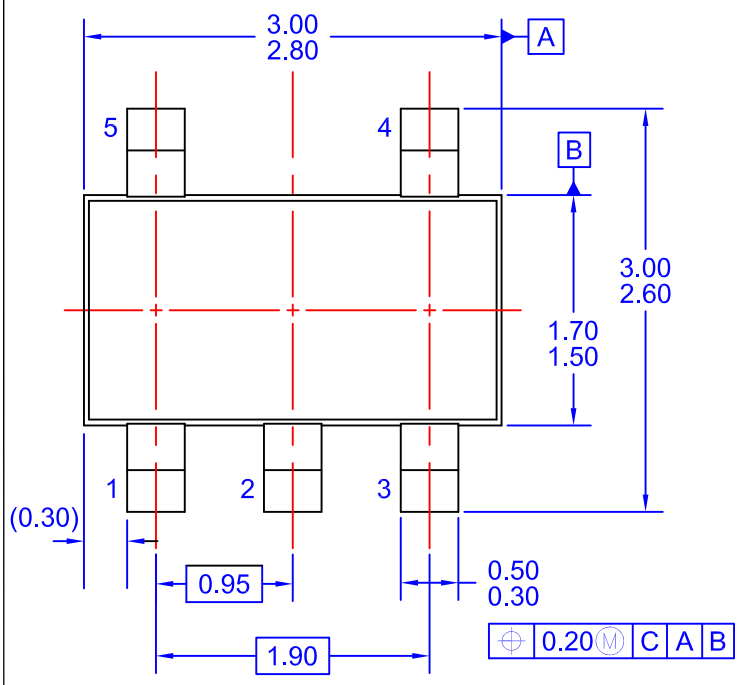

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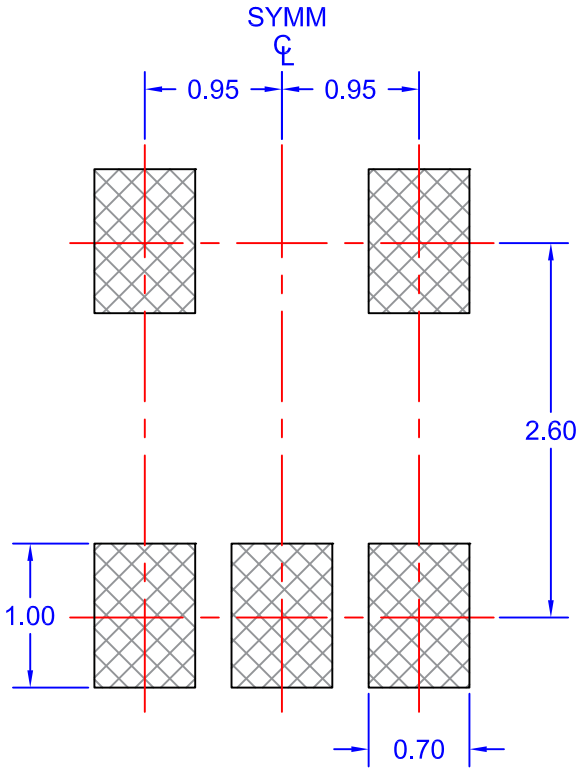

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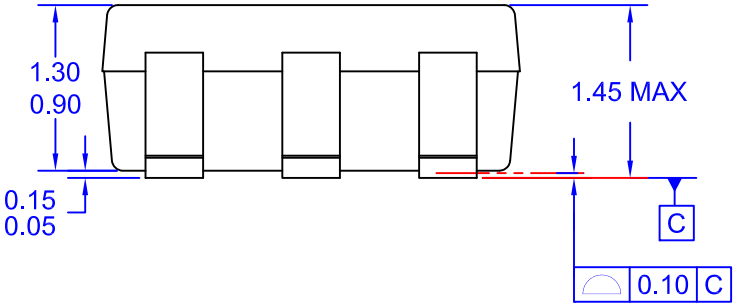

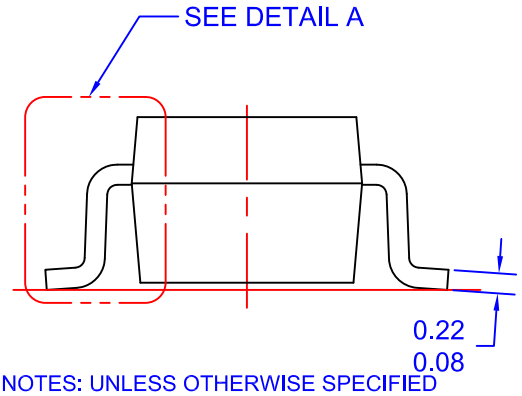

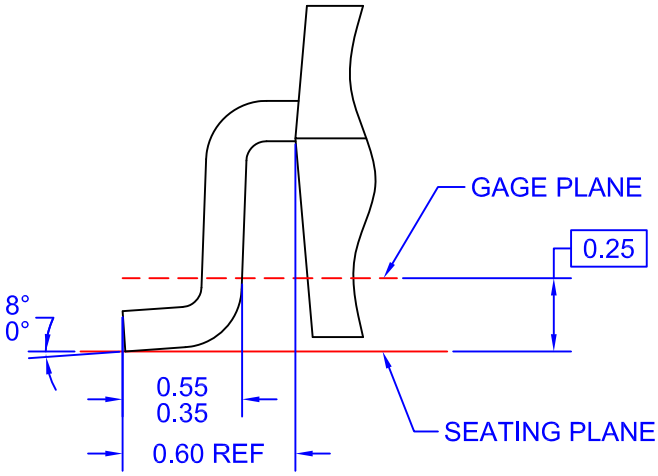

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