Faroudja Laboratories

a Division of Sage, Inc.

Rev. 1.04
January 19, 2001
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FLI 2200

Digital Component Video Deinterlacer/Line Doubler

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FLI 2200 Digital Component Video Deinterlacer/Line Doubler

Description

The FLI2200 is a single chip implementation of Faroudja Laboratories' award winning deinterlacing and post-processing algorithms that produce the highest quality progressive video output from a variety of interlaced video inputs including 525/60 (NTSC) or 625/50 (PAL or SECAM). It uses patented and patent pending motion-adaptive deinterlacing that selects the optimal filtering on a per-pixel basis. This includes detection and proper interleaving of 3:2 and 2:2 pulldown for film-base sources, including continuous monitoring and compensation for bad edits that occur frequently in broadcast material due to poor scene cuts or insertion of commercials. Video material is processed by a set of content-sensitive spatio-temporal filters that adapt to the appropriate direction for smoothest interpolation using the patented Faroudja DCDi™ algorithm. The FLI2200 also includes motion-adaptive cross-color suppression that removes highly objectionable coloration artifacts produced by commonly used video decoders. Its internal processing uses 10 bits per channel to maintain the highest quality. Its inputs and outputs are 10 bits/channel for best quality but also supports 8 bits/channel for more cost-sensitive applications. The FLI2200 requires 4 MB of low cost SDRAM for best quality deinterlacing, but it can also be operated in an optimized intra-field mode without memory for more cost-sensitive applications. This makes possible the use of a single design for both high-end and low-end applications.

The FLI2200 integrates a number of functions to provide maximum flexibility in a low cost configuration. This includes an on-chip clock generator, SDRAM controller, display controller, input and output color-space converters. It uses a standard 2-wire serial control interface for easy control and access to the registers.

The FLI2200 can be connected without glue logic to the FLI2000 video decoder and FLI2220 Enhancer and OSD Generator to produce the highest quality video pipeline for premium applications. It is also fully compatible with other decoders having a ITU-R BT 656 output format.
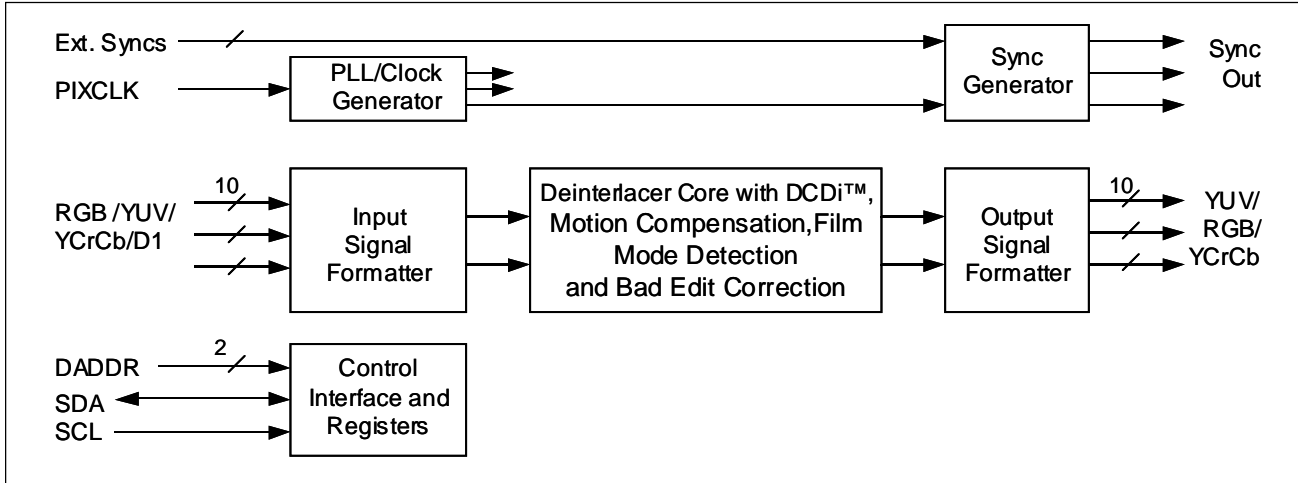
Applications

Flat panel TV – LCD, PDP

Progressive scan TVs

Multimedia front/rear projectors

Home Theater

Scan Converters

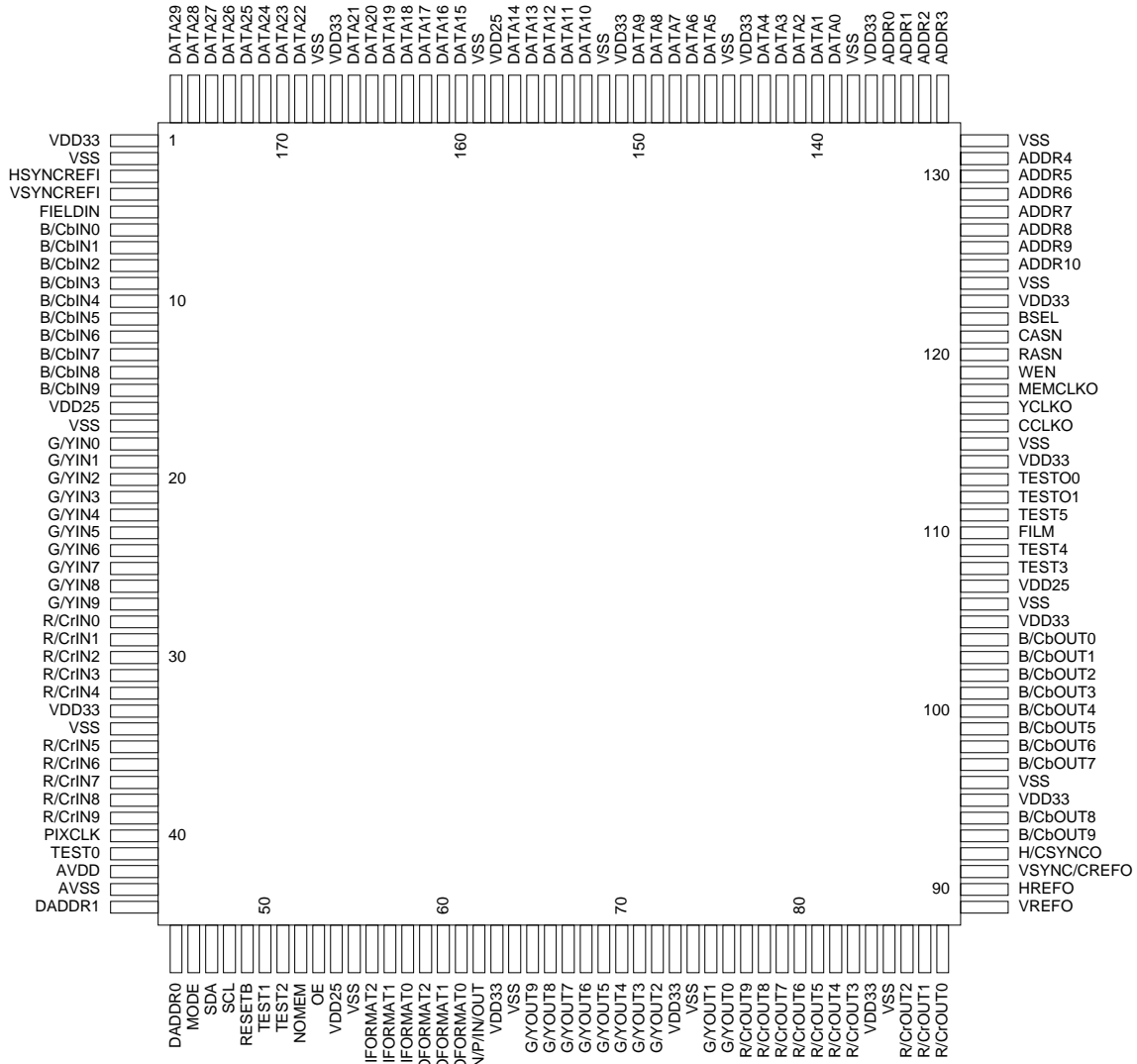Multimedia PCs/Workstations

DCDi™ is a Faroudja trademark

Features

♦ Motion-adaptive cross-color suppression removes artifacts produced by improper Y/C separation in low-cost video decoders

♦ Motion-adaptive video deinterlacing selects optimal filtering on a per-pixel basis
  • Film-mode for proper handling of 3:2 and 2:2 pulldown material
  • Bad-edit detection/correction compensates for poor scene cuts and insertions common in broadcast material
  • Motion-weighted interpolation for video sources produces maximum resolution without introducing motion artifacts
  • Directional Correlational Deinterlacing (DCDi™) minimizes jaggies on angled lines

♦ 8/10-bit Y/Cb/Cr (D1) (ITU-R BT 656), 16/20-bit Y Cb/Cr (ITU-R BT 601), 24/30-bit RGB or YCbCr/YPbPr interlaced input options
  • Supports 525/60 (NTSC), 625/50 (PAL/SECAM)
  • Accepts up to 1100 pixels/line

♦ 8/10-bit, 16/20-bit YUV, 24/30-bit RGB or YCbCr/YPbPr progressive output options

♦ Supports 8- or 10-bit inputs and outputs

♦ 10-bit internal processing for highest quality

♦ Includes color-space converters at input and output for maximum flexibility

♦ Auto-detection of NTSC/PAL/SECAM inputs

♦ High-order filtering produces smooth chroma output in 4:2:2 to 4:4:4 or 4:4:4 to 4:2:2 conversions

♦ Resolution recovery maximizes output signal-to-noise ratio and dynamic range

♦ Can be operated without glue logic with FLI2000 Video Decoder and FLI2220 Enhancer and OSD Generator ICs to produce highest quality video pipeline

♦ Glue-less interface to most standard video decoders

♦ Built-in display timing generator

♦ On-chip clock generator eliminates external PLLs

♦ On-chip SDRAM controller

♦ Uses low cost SDRAM as field memory – 4 MB

♦ Optimized intra-field operation allows memory-less configuration for lowest cost applications with same design and layout as for high-end applications

♦ 2-wire serial control interface for easy control

♦ 176-pin TQFP package

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Simplified Block Diagram

Ext. Syncs
PIXCLK
PLL/Clock Generator

Sync Generator → Sync Out

RGB /YUV/ YCrCb/D1 — 10 → Input Signal Formatter → Deinterlacer Core with DCDi™, Motion Compensation, Film Mode Detection and Bad Edit Correction → Output Signal Formatter — 10 → YUV/ RGB/ YCrCb

DADDR — 2 → Control Interface and Registers
SDA
SCL

Packaging and Pinout Information

Top pins (left to right): DATA29, DATA28, DATA27, DATA26, DATA25, DATA24, DATA23, DATA22, VSS, VDD33, DATA21, DATA20, DATA19, DATA18, DATA17, DATA16, DATA15, VSS, VDD25, DATA14, DATA13, DATA12, DATA11, DATA10, VSS, VDD33, DATA9, DATA8, DATA7, DATA6, DATA5, VSS, VDD33, DATA4, DATA3, DATA2, DATA1, DATA0, VSS, VDD33, ADDR0, ADDR1, ADDR2, ADDR3

Left pins (top to bottom):
1 VDD33
VSS
HSYNCREFI
VSYNCREFI
FIELDIN
B/CbIN0
B/CbIN1
B/CbIN2
B/CbIN3
10 B/CbIN4
B/CbIN5
B/CbIN6
B/CbIN7
B/CbIN8
B/CbIN9
VDD25
VSS
G/YIN0
G/YIN1
20 G/YIN2
G/YIN3
G/YIN4
G/YIN5
G/YIN6
G/YIN7
G/YIN8
G/YIN9
R/CrIN0
R/CrIN1
30 R/CrIN2
R/CrIN3
R/CrIN4
VDD33
VSS
R/CrIN5
R/CrIN6
R/CrIN7
R/CrIN8
R/CrIN9
40 PIXCLK
TEST0
AVDD
AVSS
DADDR1

Right pins (top to bottom):
VSS
ADDR4
130 ADDR5
ADDR6
ADDR7
ADDR8
ADDR9
ADDR10
VSS
VDD33
BSEL
CASN
120 RASN
WEN
MEMCLKO
YCLKO
CCLKO
VSS
VDD33
TESTO0
TESTO1
TEST5
110 FILM
TEST4
TEST3
VDD25
VSS
VDD33
B/CbOUT0
B/CbOUT1
B/CbOUT2
B/CbOUT3
100 B/CbOUT4
B/CbOUT5
B/CbOUT6
B/CbOUT7
VSS
VDD33
B/CbOUT8
B/CbOUT9
H/CSYNCO
VSYNC/CREFO
90 HREFO
VREFO

Bottom pins (left to right): DADDR0, MODE, SDA, SCL, RESETB, TEST1, TEST2, NOMEM, OE, VDD25, VSS, IFORMAT2, IFORMAT1, IFORMAT0, OFORMAT2, OFORMAT1, OFORMAT0, N/P/IN/OUT, VDD33, VSS, G/YOUT9, G/YOUT8, G/YOUT7, G/YOUT6, G/YOUT5, G/YOUT4, G/YOUT3, G/YOUT2, VDD33, VSS, G/YOUT1, G/YOUT0, R/CrOUT9, R/CrOUT8, R/CrOUT7, R/CrOUT6, R/CrOUT5, R/CrOUT4, R/CrOUT3, VDD33, VSS, R/CrOUT2, R/CrOUT1, R/CrOUT0

Package: 176-pin TQFP. θ_{ja} = xx °C/watt

Pin Connections and Functions

Pin #	Name	Description
Power Supply Connections (not shown on Block diagram)		
See list	V_{SS}	Ground connections. Connect to the digital ground plane. Pins: 2, 17, 34, 55, 64, 74, 85, 96, 106, 115, 124, 132, 138, 145, 152, 159, 168
See list	V_{DD33}	Pad Ring digital power connections. Connect to the digital 3.3 volt power supply and decouple to the digital ground plane. Pins: 1, 33, 63, 73, 84, 95, 105, 114, 123, 137, 144, 151, 167
See list	V_{DD25}	Core Logic digital power connections. Connect to the digital 2.5 volt power supply and decouple to the digital ground plane. Pins: 16, 54, 107, 158
43	AV_{SS}	Ground connection for the clock PLL circuits. Connect to the digital ground plane
42	AV_{DD}	Analog power connections for the clock PLL circuit. Connect to a separately decoupled 2.5 volt power supply and decouple directly to the AV_{SS} pin..
Control Signals		
49	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
53	OE	When this pin is set high the outputs of the FLI2200 will be enabled; when it is set low the outputs will be set into a high-impedance state.
56-58	$IFORMAT_{2-0}$	Input signal format control. The settings of these pins set the format of the input signal. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details.
59-61	$OFORMAT_{2-0}$	Output signal format control. The settings of these pins set the format of the output signal. This can be overridden by the OFmtOvr bit, bit 3 in register 07_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 07_H for details.
44-45	$DADDR_{1-0}$	The settings of $DADDR_{1-0}$ allow the device address of the control bus to be programmed to prevent conflict with the other devices connected to the bus. $DADDR_{1-0}$ allow the device address to be set to any of the following values: $C0/C1_H$, $C2/C3_H$, $E0/E1_H$, $E2/E3_H$. Please refer to the section "Control Bus Operation and Protocol" for further information.
46	MODE	When this pin is set low the control bus will operate in the slave mode; allowing the device to programmed from an external controller. When it is set high the FLI2200 will self-program from an external I^2C memory connected to the bus. Please refer to the "Control Bus Operation and Control Protocol" section for more details.
47	SDA	2-wire serial control bus data. Data can be written to the control registers via this pin when it is in the input mode and data can be read from the status registers when it is in the output mode. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
48	SCL	2-wire serial control bus clock. When the control port operates in slave mode this pin will be an input and when it operates in the self programming mode it will be an output.
40	PIXCLK	Pixel clock input. This clock is used to drive all the circuits in the FLI2200. An internal PLL is used to upconvert this clock to provide the master clock signal and other clocks used internally. Note that when the FLI2200 is used in the D1 input mode the PIXCLK input should run at the rate of two cycles per pixel (one for luma and one for chroma).
62	N/P/IN/OUT	NTSC/PAL input or output. The default function of this pin is NTSC/PAL signal indicator output. When the input video signal is a 525 line signal this pin will be set high and when it is a 625 line signal the pin is set low. This function of this pin can be programmed to be an input according to the setting of this pin if the $NPOp_{1-0}$ bits, bits 5-4 in register 03_H, are set to 00_H, overriding the internal line counter. i.e., it will treat the signal as a 525 line signal when it is set high and a 625 line signal when it is set low.

Pin #	Name	Description
Control Signals (contd.)		
52	NOMEM	No Memory Mode control input. This pin controls the operation of the FLI2200 as follows: When this pin is set low the device is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources). When this pin is set high the FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement. ***To ensure proper startup of the SDRAMs this pin should be set high during the power-up sequence.*** This can be overridden by the NMOvr bit, bit 1 in register 05_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 05_H for details.
Input Signals		
27-18	G/YIN$_{9-0}$	10-bit green or luminance signal input bus. The mode is set by the IFORMAT$_{2-0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. This signal is sampled on the rising edge of PIXCLK.
15-6	B/CbIN$_{9-0}$	10-bit blue or Cb chroma signal input bus. The mode is set by the IFORMAT$_{2-0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. Bits 6, 4 and 3 in register 08_H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr and Y Pb Pr modes the Cb or Pb signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
39-35 32-28	R/CrIN$_{9-0}$	10-bit red or Cr chroma signal input bus. The mode is set by the IFORMAT$_{2-0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. Bits 6, 4 and 3 in register 08_H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr mode the Cr signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
3	HSYNCREFI	Horizontal sync or reference. The horizontal sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H. The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
4	VSYNCREFI	Vertical sync or reference. The vertical sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H. The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
5	FLDIN	Field identifier input. The field identifier output of the source signal should be connected to this pin. A low setting signifies an even field and a high level signifies an odd field. When bit 4 in register 00_H is set low, the input timing is based on HREF and VREF and this signal is required. When this bit is set high the input timing is based on HSYNC and VSYNC and this signal is generated internally and is not required. When bit 5 in register 06 is set high this signal is also used as the frame boundary identifier for 30 Hz film sources.

Pin #	Name	Description
Output Signals		
65-72 75-76	G/YOUT$_{9-0}$	Green or luminance output bus. In the RGB mode this output is the Green signal and in the YCbCr mode it is the Y signal. The mode is set by the OFORMAT$_{2-0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07$_H$, allowing this function to be set or changed via the I^{2}C bus. Please refer to the description of register 07$_H$ for details. The signal is clocked out on the falling edge of YCLKO.
93-94 97-104	B/CbOUT$_{9-0}$	Blue or Cb chrominance output bus. In the RGB mode this output is the Blue signal, in the Y Cb Cr mode it is the Cb signal. The mode is set by the OFORMAT$_{2-0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07$_H$, allowing this function to be set or changed via the I^{2}C bus. Please refer to the description of register 07$_H$ for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08$_H$. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
77-83 86-88	R/CrOUT$_{9-0}$	Red or Cr chrominance output bus. In the RGB mode this output is the Red signal, in the YCbCr mode it is the Cr signal. The mode is set by the OFORMAT$_{2-0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07$_H$, allowing this function to be set or changed via the I^{2}C bus. Please refer to the description of register 07$_H$ for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08$_H$. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
116	CCLKO	Chroma output sampling clock. This clock is derived from PIXCLK and will be at half the frequency of YCLKO. In 30-bit 4:2:2 output mode the chroma output signals will change on the falling edge of YCLKO prior to the next rising edge this clock.
117	YCLKO	Luma output sampling clock. This clock is derived from PIXCLK and is double the frequency of PIXCLK. In 30-bit and 20-bit output modes the output signals will change on the falling edge of this clock.
89	VREFO	Start of active field or frame indicator. This signal goes high to indicate the first active line in each field or frame and goes low during the vertical blanking interval. The polarity and timing of this signal are programmable.
90	HREFO	Start of active line indicator output. This signal goes high to indicate the first active pixel in each line and goes low during the horizontal blanking interval. The polarity and timing of this signal are programmable.
91	VSYNC/ CREFO	Vertical sync output. This signal provides the vertical sync function for the outputs. Its polarity is programmable to be active high or active low. It can also be programmed to be a composite reference for applications requiring this instead of sync.
92	H/CSYNCO	Horizontal or composite sync output. This signal provides the horizontal sync function for the outputs. Its polarity is programmable to be active high or active low. This signal can also be programmed to be the composite sync output, CSYNC.
110	FILM	Film mode detector output. This pin will be set high when the FLI2200 detects that the video input was converted from 24 fps film with a teleciné machine. If film mode is not detected this pin will be set low.

Pin #	Name	Description
SDRAM Interface Signals		
125-131 133-136	$ADDR_{10-0}$	SDRAM Address bus. This signal bus is used to address the external SDRAM(s) used for field memories. It should be connected to the A_{10-0} bus of the memory chip(s). Please refer to the Applications section of this data sheet for further details.
176-169 166-160 157-153 150-146 143-139	$DATA_{29-0}$	SDRAM Data bus. This signal bus is used to transfer the data to and from the external SDRAM(s) used for field memories. It should be connected to the DQ_{29-0} bus of the memory chip when using a 64 Mbit SDRAM. When using two 16 Mbit SDRAMs this 30-bit bus may be connected to the two 16-bit data busses of the memories in two ways: either connect 16 lines to one chip and 14 to the other, or connect 15 to both. In all cases the two unused data lines on the memory chip(s) should be connected to ground via 22 kΩ resistors. Please refer to the Applications section of this data sheet for further details.
118	MEMCLKO	SDRAM clock and 2x output sampling clock. This clock is derived from PIXCLK and will be at double the frequency of YCLKO. This active signal should be connected to the CLK pin(s) on the SDRAM(s). When the 10-bit output mode selected the output signals will also change at this clock rate and this should then be used as the output clock..
119	WEN	SDRAM Write Enable. This active low signal should be connected to the WE pin(s) on the SDRAM(s).
120	RASN	SDRAM Row Address Select. This active low signal should be connected to the RAS pin(s) on the SDRAM(s).
121	CASN	SDRAM Column Address Select. This active low signal should be connected to the CAS pin(s) on the SDRAM(s).
122	BSEL	SDRAM Bank Select. When using two 16 Mbit SDRAMs this signal should be connected to the BA (also called BS or A_{11}) pin on both SDRAMs. When using a 64 Mbit SDRAM this signal should be connected to the BA0 (also called BS0 or A_{11}) pin on the SDRAM and BA1/BS1 (also called BA when BA0 is referred to as A_{11}) should be tied low.
Test Inputs		
41, 50, 51, 108, 109, 111	$TEST_{5-0}$	These pins are used for test purposes only and should always be tied low for normal operation.
Test Outputs		
112, 113	$TESTO_{1-0}$	These pins are test outputs and should be left unconnected in normal operation.

Description of Functional Blocks

Note on signal conventions used in this document:

The following conventions are used to denote the three component signal formats used in the FLI2200:

The name Cb is used to denote the B-Y component, regardless of the actual color space (Cb, Pb, etc.).

The name Cr is used to denote the R-Y component, regardless of the actual color space (Cr, Pr, etc.).

Y Cb Cr denotes a 3-bus signal, i.e., 3 x 10 bits, with the three components unmultiplexed. Signals in this format can have either 4:4:4 or 4:2:2 sampling structures. RGB signals will also be in this format, with a 4:4:4 sampling structure.

Y Cb/Cr denotes a 2-bus signal, i.e., 2 x 10 bits, with the Cb and Cr components multiplexed. Signals in this format will always have a 4:2:2 sampling structure.

Y/Cb/Cr denotes a 1-bus signal, i.e., 1 x 10 bits, with all three components multiplexed. Signals in this format will always have a 4:2:2 sampling structure. At the input this signal will be in parallel D1 format with either embedded timing codes or external horizontal and vertical timing references.

System Clock Generation Block

A number of system clocks are derived from the PIXCLK input using frequency multiplier circuits. This eliminates the need for an external high frequency clock driver and permits the device to be driven directly by the pixel clock of the input signal.

Control Interface and Register Block

The control interface and register block consists of a 2-wire serial bus controller and a number of control and status registers. When a write-byte command is received on the bus the controller writes bytes of data received from the bus into the control registers . When a read-byte command is received on the bus the decoder reads information bytes from the status registers and outputs them on the bus. The bus is generally I^{2}C compatible.

Input Formatter Block

The input formatter block consists of two sections, the color space converter and the multiplexer/demultiplexer. The FLI2200 processes all signals in 4:2:2 Y Cb/Cr format. In order to allow the device to be operated with RGB inputs an optional color space conversion matrix is incorporated. After conversion the chroma components will be decimated to provide the 4:2:2 format.

The FLI2200 can also be used with component inputs. The signals can be in 3 x 10-bit Y Cb Cr format, 2 x 10-bit Y Cb/Cr format or 1 x 10-bit Y/Cb/Cr (D1) format. Regardless of which format is used the signals will all be converted into 2 x 10-bit Y Cb/Cr format in this block before further processing. Thus, if the input format selected is 3 x 10-bit Y Cb Cr (or RGB) the chroma signals will be multiplexed, with an optional decimation stage for 4:4:4 inputs. Conversely, if the input mode selected is 1 x 10-bit Y/Cb/Cr at 27 MHz the luma and chroma signals will be demultiplexed. 2 x 10 bit Y Cb/Cr signals will not require any processing in this block.

At the input, a programmable gain function can be used to maximize the signal range if the input signal has sync on Y or G. After the sync is stripped from the signal the gain function expands R G B or Y Cb Cr to the full 10-bit dynamic range to minimize quantization effects in the processing. The Y and Cb Cr signal gains can also be programmed independently. When the D1 mode is selected the embedded codes will be detected to generate all timing information, eliminating the need to use external syncs in this mode. The gains will be set automatically in this case.

Luma Processing Block

The luma processing block consists of a motion detector, film mode detector with bad-edit detector, the interpolator and luma line doubling FIFOs.

The motion detector is frame based and compares the luma value of the current pixel and the same pixel in the previous frame. This is done in both the odd and even fields to generate a motion vector which is then used to switch the signal processing between field interleave and spatial interpolation modes on a pixel by pixel basis. In this way, non-moving parts of the picture, where sharpness is readily detected by the viewer, will not be interpolated and will have maximum sharpness. Conversely, moving parts of the picture, where sharpness is not easily detected by the viewer, will be interpolated to avoid motion artifacts. The consequences of interleaving fields in areas of the picture containing motion are significantly worse than the loss of resolution caused by interpolation.

The film mode detector detects the 3:2 or 2:2 pulldown sequences from teleciné conversion. Converting 24 frame/sec. film to 60 field/sec. maps two film frames ($^1/_{12}$ sec.) into five video fields (also $^1/_{12}$ sec.), alternating between three odd and two even fields and three even and two odd fields. This pattern repeats over ten video fields. For further information on film mode please refer to the Applications section of this data sheet. Converting 24 frame/sec. film to 50 field/sec. video is done by running the film at 25 frames/sec. This is the same procedure as converting 30 frame/sec. film to 60 field/sec. video and results in the much simpler pattern of one film frame being mapped into one odd and one even field of video. In all cases, the film mode detector detects these sequences in the signal and uses them to correctly pair odd and even fields originating from the same film frame. Once this is done, these field pairs can be interleaved without consideration of motion since there is, by definition, no motion between them. Film mode overrides video mode processing.

The bad edit detector continually monitors the sequences for breaks caused by video edits made after the teleciné transfer. There are 25 possible ways for the 3:2 pulldown sequence to be interrupted, and only two of these will not result in a break in the sequence. The bad edit detector looks for the break and forces the FLI2200 to switch out of film mode and into video mode before the bad edit is seen on the screen. The film mode detector will then reaquire the pulldown sequence, allowing the system to be switched back into film mode transparently.

Note that film mode detection is not done in the peripheral areas of the frame; this prevents the bad edit detector from causing the system to drop out of film mode in the presence of on-screen display (OSD) graphics, such as subtitles, added to the video in these regions by the source, e.g., a DVD player. However, any graphics added to the central zone can cause the system to drop out of film mode any time they change, since the changes will generally not be synchronized to the 3:2 pulldown sequence, in which case they will be indistinguishable from bad edits.

The intra-field interpolator is used to generate the missing pixels in the field when motion is detected in video mode and the pixels from the previous field cannot be interleaved. The FLI2200 uses a new diagonal interpolation algorithm, Directional Correlation Deinterlacing™, (DCDi™, patent pending) that computes and tracks the angles of edges and uses this information to optimally fill in the missing pixels. Conventional vertical interpolation algorithms work well on edges close to the horizontal and vertical directions but can completely break down as the angles of edges become more diagonal. Diagonal interpolation eliminates this problem. The operation of the FLI2200 can be forced into the intra-field diagonal interpolation mode at all times, allowing it to be used without external field memories in low-cost applications.

Finally, the results of the motion detector, film mode detector and bad edit detector are used to control the signal paths into the de-interleaving FIFOs, determining whether interpolated pixels or pixels from the previous field are used in the interleaving process.

Chroma Processing Block

The chroma processing block consists of a cross-color suppressor, chroma line-averager and the chroma line doubling FIFOs. Positioning the cross-color suppressor in the deinterlacer takes advantage of the frame buffers already required for temporal processing and eliminates the need to use a 3-D comb filter with duplicate frame buffers.

The cross-color suppressor helps to eliminate residual cross-color after the decoder. With the exception of 3-D decoders, all decoders, such as the Faroudja FLI2000, use a 2-D comb filter and/or notch filter, which leave residual cross-color under certain circumstances, such as diagonal edges, and the frame-based cross-color suppressor eliminates this in most cases, leaving the residual cross-color at a very low level. Complete suppression is only possible in the absence of motion because some conditions (diagonal edges moving diagonally at rates with certain relationships to the field rate) result in signals which are completely impossible to fully separate because the luma and chroma spectra are completely superimposed.

The chroma line averager is used to perform interpolation in the chroma path and passes the deinterlaced chroma signals into the line doubler memories.

Field Memory Interface Block

The field memory interface block formats the data and generates all the addressing required to use standard SDRAM for the field memories. The FLI2200 requires memory in a 1 Mbit x 30 configuration. This can be achieved either by using two 16 Mbit (1 Mbit x 16) SDRAMs or one 64 Mbit (2 Mbit x 32) SDRAMs. The FLI2200 was designed to operate with the Micron MT48LC1M16A1 and MT48LC2M32B2; it is also compatible with the following devices:

Vendor	16 Mbit	64 Mbit
Fujitsu	MB81F161622C	MB81F643242B
Hyundai	HY57V161610	HY57V653220
Micron	MT48LC1M16A1	MT48LC2M32B2
Samsung	K4S161622D	K4S643232C

The FLI2200 is also compatible with 1M x 32 SGRAMs.

In all cases the speed grade required is application dependent, the SDRAM interface operates at twice the input pixel rate. For NTSC/PAL inputs (13.5 Mpix/sec.) the SDRAM clock speed requirement is 54 MHz, so that the lowest speed grade devices (10 nsec./100 MHz) will easily meet these requirements.

Output Formatter Block

The output formatter block consists of two sections, the multiplexer/demultiplexer and the color space converter. The multiplexer/demultiplexer allows the signal format to be converted from the 4:2:2 Y Cb/Cr format used internally to either Y Cb Cr or Y/Cb/Cr. An optional interpolation filter then allows the signals to be converted to 4:4:4 format when the Y Cb Cr mode is selected. The color space converter further allows the Y Cb Cr 4:4:4 signals to be converted into R G B 4:4:4 format. The 4:2:2 Y Cb Cr signal can also be converted into Y Pb Pr.

Memory Map

Register Addr.	Name	7	6	5	4	3	2	1	0	Default Value
00_H	INPUT	CClmpEn	YClmpEn	SOnYG	Sync/Ref	IFmtOvr		$IFormat_{2-0}$		$D0_H$
01_H	YCLAMP				$YClamp_{7-0}$					40_H
02_H	CCLAMP				$CClamp_{7-0}$					00_H
03_H	NP	x	NPStat	$NPOp_{1-0}$		$CClamp_{9-8}$		$YClamp_{9-8}$		18_H
04_H	DELAY	$CDelay_{3-0}$				CSwapI	$YDelay_{2-0}$			$B4_H$
05_H	MODE1	Fm2430	x	Test	Test	DCDiOn	FilmOn	NMOvr	NoMem	$0C_H/8C_H$
06_H	MODE2	CSync	VITSEn	F30Hz	F30Inv	Force30	$Motion_{1-0}$		PComp	05_H
07_H	OUTPUT	CSwapO	ChrPhs	CIntDis	OBlnkEn	OFmtOvr	$OFormat_{2-0}$			10_H
08_H	IOSEL	D1Valid	CInSel	COutSel	$D1InSel_{1-0}$		$FSyncDel_{2-0}$			52_H
09_H	GAIN	x	x	x	x	x	x	YInGain	CInGain	03_H
$0A_H$	FDELAY				$BSStart_{7-0}$					$4A_H$
10_H	HSSTN				$HSStartN_{7-0}$					00_H
11_H	HSSPN				$HSStopN_{7-0}$					00_H
12_H	HRSTN				$HRStartN_{7-0}$					00_H
13_H	HRSPN				$HRStopN_{7-0}$					00_H
14_H	VMSN	$VSStartN_{5-4}$		$VSStopN_{5-4}$		$VRStartN_{5-4}$		$VRStopN_{5-4}$		00_H
15_H	VSSSN	$VSStartN_{3-0}$				$VSStopN_{3-0}$				00_H
16_H	VRSSN	$VRStartN_{3-0}$				$VRStopN_{3-0}$				00_H
17_H	VBIMSN	x	$VBStartN_4$	x	$VBStopN_4$	$VBIStartN_{5-4}$		$VBIStopN_{5-4}$		00_H
18_H	VBTN	$VBStartN_{3-0}$				$VBStopN_{3-0}$				00_H
19_H	VBITN	$VBIStartN_{3-0}$				$VBIStopN_{3-0}$				00_H
20_H	HSSTP				$HSStartP_{7-0}$					00_H
21_H	HSSPP				$HSStopP_{7-0}$					00_H
22_H	HRSTP				$HRStartP_{7-0}$					00_H
23_H	HRSPP				$HSRtopP_{7-0}$					00_H
24_H	HMSP	$HSStartP_{9-8}$		$HSStopP_{9-8}$		$HRStartP_{9-8}$		$HRStopP_{9-8}$		00_H
25_H	VSSTP				$VSStartP_{7-0}$					00_H
26_H	VSSPP				$VSStopP_{7-0}$					00_H
27_H	VRSTP				$VRStartP_{7-0}$					01_H
28_H	VRSPP				$VRStopP_{7-0}$					01_H
29_H	VBSTP				$VBStartP_{7-0}$					01_H
2A	VBSPP				$VBStopP_{7-0}$					00_H
2B	VBISTP				$VBIStartP_{7-0}$					02_H
2C	VBISPP				$VBIStopP_{7-0}$					08_H
$2E_H$	VBTP	Test	x	x	UseHSize	x	$HSize_{10-8}$			03_H
$2F_H$	HSIZE				$HSize_{7-0}$					60_H
30_H	INV1	ISyncInv	ORefInv	OSyncInv	DatBlnk	HDatBlnk	Test	Test	CCSOn	05_H
31_H	EDBL				$EdBlnkL_{7-0}$				$E0_H$	

Register Addr.	Name	7	6	5	4	3	2	1	0	Default Value
32_H	EDBR	$EdBlnkR_{7-0}$								52_H
33_H	EDBT	$EdBlnkT_{7-0}$								42_H
34_H	EDBBN	$EdBlnkBN_{7-0}$								$F4_H$
35_H	EDBBP	$EdBlnkBP_{7-0}$								58_H
36_H	EDBMS	$EdBlnkL_8$	$EdBlnkR_{9-8}$		$EdBlnkT_8$	$EdBlnkBN_{9-8}$		$EdBlnkBP_{9-8}$		66_H
37_H	FMBL	$FmBlnkL_{7-0}$								96_H
38_H	FMBR	$FmBlnkR_{7-0}$								58_H
39_H	FMBT	$FmBlnkT_{7-0}$								42_H
$3A_H$	FMBBN	$FmBlnkBN_{7-0}$								$F4_H$
$3B_H$	FMBBP	$FmBlnkBP_{7-0}$								58_H
$3C_H$	FMBMS	$FmBlnkL_8$	$FmBlnkR_{9-8}$		$FmBlnkT_8$	$FmBlnkBN_{9-8}$		$FmBlnkBP_{9-8}$		66_H
$3D_H$	TEST	$Test_{7-0}$								14_H
$3E_H$	TEST	$Test_{7-0}$								$0E_H$
$3F_H$	TEST	$Test_{7-0}$								60_H
40_H	TEST	$Test_{7-0}$								05_H
41_H	TEST	x	x	x	x	$Test_{3-0}$				$0C_H$
42_H	TEST	$Test_{7-0}$								14_H
through		See register descriptions for default values of these registers								
$4C_H$	TEST	$Test_{7-0}$								38_H
$4D_H$	TEST				$Test_{4-0}$					00_H
$4E_H$	PFILM				$Test_{3-0}$					07_H
$4F_H$	PFTHR	$Test_{7-0}$								04_H
50_H	TEST			$Test_{5-0}$						14_H
51_H	TEST	$Test_{7-0}$								18_H
52_H	TEST	$Test_{7-0}$								06_H
53_H	TEST	$Test_{7-0}$								30_H
54_H	TEST	$Test_{7-0}$								30_H
60_H	PLL0	$PLL\ MDiv_{7-0}$								18_H
61_H	PLL1	$PLL\ NDiv_{7-0}$								30_H
62_H	PLL2	Lock		Disable	PByp	PLLOvr	$PDiv_{2-0}$			$02_H/82_H$
63_H	ODIS						ROutDis	GOutDis	BOutDis	00_H
64_H	INV2	$Test_{1-0}$		InvYClk	$Test_{4-0}$					00_H
65_H	TEST	$Test_{7-0}$								00_H
66_H	SDEL				$SDel_{4-0}$					00_H
67_H	TEST	$Test_{7-0}$								08_H
71_H	TEST	$Test_{7-0}$								00_H
72_H	TEST						$Test_{2-0}$			00_H
$7E_H$	IDL	$ChipID_{7-0}$								41_H
$7F_H$	IDH	$ChipID_{15-8}$								$4B_H$

Register Details

Note: All values are binary except for those with an H suffix, which are hexadecimal. * Indicates default value

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Address 00_H: INPUT Control Register . Default value $D0_H$

The eight bits in the INPUT register control the front-end configuration, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	CClmpEn	YClmpEn	SOnYG	Sync/Ref	IFmtOvr	$IFormat_2$	$IFormat_1$	$IFormat_0$
Default value	1	1	0	1	0	0	0	0

CClmpEn: The CClmpEn bit is used to enable the chroma clamp circuit, as follows:

        0   = Chroma clamp disabled. The input clamp levels will be used

        1*   = Chroma clamp enabled. The clamp levels will be set according to the value of the CClamp data in register 02_H.

YClmpEn: The YClmpEn bit is used to enable the luma clamp circuit, as follows:

        0   = Luma clamp disabled. The input clamp level will be used

        1*   = Luma clamp enabled. The clamp level will be set according to the value of the YClamp data in register 01_H.

SOnYG: The SOnYG bit is used according to whether or not there is sync on the luma/green input, as follows:

        0*   = No sync pulses on the luma/green channel input.

        1   = Luma/green channel input contains sync pulses.

When this bit is set high the Y and Cb Cr signals will be expanded to full scale after sync removal to maximize the dynamic range of the processing operations, overriding the settings of the YInGain and CInGain bits in register 09_H. When this bit is set low the gains can be set independently with the YInGain and CInGain bits in register 09_H.

Sync/Ref: The Sync/Ref bit is used to define the input timing signals, as follows:

        0   = The FLI2200 is configured to use horizontal and vertical references as timing signals.

        1*   = The FLI2200 is configured to use horizontal and vertical sync pulses as timing signals.

IFmtOvr: The IFmtOvr bit is used to control the input format function, as follows:

        0*   = The FLI2200 is configured to use the input format defined by the $IFORMAT_{2-0}$ pins, pins 56-58. The formats defined will be same as those defined for the $IFormat_{2-0}$ bits.

        1   = The FLI2200 is configured to use the input format defined by the $IFormat_{2-0}$ bits in this register, overriding the pin settings.

$IFormat_{2-0}$:   The $IFormat_{2-0}$ bits are used to define the format of the input signals, as follows:

$IFormat_{2-0}$	Input signal format
000*	= Y Cb/Cr
001	= Y Cr Cb
010	= Y Pb/Pr
011	= Y Pr Pb
10x	= R G B
110	= Y/Cb/Cr (D1, with embedded timing)
111	= Y/Cb/Cr (D1, with external/separate syncs)

Set the InvYClk bit, bit 5 in register 62_H, high when using the D1 input modes, 11x.

The busses used for the multiplexed signals (Cb/Cr and Y/Cb/Cr) in modes 000 and 11x are determined by the settings of the CinSel and D1InSel bits in register 08_H, as shown on page 49.

Address 01$_H$: YCLAMP Control Register. Default value 40$_H$

The eight bits in the YCLAMP register set the luma clamp level, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	YClamp$_7$	YClamp$_6$	YClamp$_5$	YClamp$_4$	YClamp$_3$	YClamp$_2$	YClamp$_1$	YClamp$_0$
Default value	0	4	0	0	0	0	0	0

YClamp$_{7-0}$ These bits, in conjunction with bits 1-0 in register 03$_H$, set the clamp level for the luma signal when the YClmpEn bit is set high, as follows:

000$_H$* = Minimum clamp level 000$_H$ (0).

040$_H$* = Default clamp level 040$_H$ (64).

3FF$_H$ = Maximum clamp level, 3FF$_H$ (1023)

Address 02$_H$: CCLAMP Control Register. Default value 00$_H$

The eight bits in the CCLAMP register set the luma clamp level, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	CClamp$_7$	CClamp$_6$	CClamp$_5$	CClamp$_4$	CClamp$_3$	CClamp$_2$	CClamp$_1$	CClamp$_0$
Default value	0	0	0	0	0	0	0	0

CClamp$_{7-0}$ These bits, in conjunction with bits 3-2 in register 03$_H$, set the clamp level for the chroma signals when the CClmpEn bit is set high, as follows:

000$_H$* = Minimum clamp level 000$_H$ (0).

200$_H$* = Default clamp level 200$_H$ (512).

3FF$_H$ = Maximum clamp level, 3FF$_H$ (1023)

Address 03_H: NP (NTSC/PAL) Control Register. Default value 18_H

Seven bits in the NP register are used to control the NTSC/PAL operation and the clamp levels, as shown below. Bit 6 is Read Only.:

Bit	7	6	5	4	3	2	1	0
Mnemonic	x	NPStat	$NPOp_1$	$NPOp_0$	$CClamp_9$	$CClamp_8$	$YClamp_9$	$YClamp_8$
Default value	x	R/O	0	1	1	0	0	0

x: This bit is not used and does not exist physically.

NPStat: This bit indicates the status of the NTSC/PAL (525/625 line) detector. It is a read-only (R/O) function. This bit, as well as the NP/IN/OUT pin when it is an output, will indicate the actual line count, regardless of the settings of the $NPOvr_{1-0}$ bits in this register, as follows:

    0   = 625 line signal detected.

    1   = 525 line signal detected.

$NPOp_{1-0}$: These bits configure the operation of the FLI2200 and the N/P/IN/OUT pin, pin 62, as follows:

$NPOp_{1-0}$	Configuration	N/P/IN/OUT Function
00	= Set NTSC/PAL mode according to setting of N/P/IN/OUT pin.	Input
01*	= Auto detect signal using internal NTSC/PAL detector.	Output
10	= Force FLI2200 to NTSC operation.	Output (high)
11	= Force FLI2200 to PAL operation.	Output (low)

$CClamp_{9-8}$: These bits, in conjunction with bits 7-0 in register 02_H, set the clamp level for the chroma signals. These are the most significant bits of the 10-bit value. See description of register 02_H for details.

$YClamp_{9-8}$: These bits, in conjunction with bits 7-0 in register 01_H, set the clamp level for the luma signal. These are the most significant bits of the 10-bit value. See description of register 01_H for details.

Address 04_H: DELAY Control Register. Default value $B4_H$

The seven bits in the DELAY register set the luma and chroma delay at the front end, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$CDelay_3$	$CDelay_2$	$CDelay_1$	$CDelay_0$	CSwapI	$YDelay_2$	$YDelay_1$	$YDelay_0$
Default value	1	0	1	1	0	1	0	0

$CDelay_{3-0}$: These bits set the delay for the chroma signals, as follows:

    0_H = Minimum chroma delay, 0 pixels.

    B_H* = Default chroma delay, 11 pixels.

    F_H = Maximum chroma delay, 15 pixels.

CSwapI: This bit swaps the Cb and Cr components at the input, as follows:

    0*   = Chroma components not swapped (normal).

    1   = Chroma components swapped (reversed).

$YDelay_{3-0}$: These bits set the delay for the luma signal, as follows:

    0_H = Minimum luma delay, 0 pixels.

    4_H* = Default luma delay, 4 pixels.

    7_H = Maximum luma delay, 7 pixels.

Address 05$_H$: MODE1 Control Register. Default value 0C$_H$

The six bits in the MODE1 register control various deinterlacing functions, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Fm2430	x	Test	Test	DCDiOn	FilmOn	NMOvr	NoMem
Default value	R/O	x	0	0	1	1	0	0

Fm2430:   This read-only bit indicates the type of film mode detected, as follows:

        0   = 2:2 pulldown detected. This is the normal mode when the video source is 625 line PAL. Note that 2:2 pulldown in NTSC indicates a 30 fps film source. This mode will only be active if the F30Hz bit in register 06$_H$ is set high.

        1   = 3:2 pulldown detected. This indicates 24 fps film in NTSC. This mode is not active when the video source is 625 line PAL.

x: This bits is not used and does not physically exist.

Test: These bits turn on special test functions, as follows:

        0*   = Normal mode.

        1   = Test mode, not for normal use.

DCDiOn: This bit controls the operation of the interpolator, as follows:

        0   = DCDi OFF. Vertical interpolation is used.

        1*   = DCDi ON. Diagonal Correlation interpolation is used.

FilmOn: This bit controls the operation of the film mode detector, as follows:

        0   = Film mode detector is disabled, all signals processed as video.

        1*   = Film mode detector is enabled, film and video sourced signals are processed separately.

NMOvr: This bit controls the operation of the FLI2200, as follows:

        0*   = Operating mode is determined by the setting of the NOMEM pin, pin 52.

        1   = Operating mode is determined by the setting of the NoMem bit, overriding the setting of the NOMEM pin, pin 52..

NoMem: This bit controls the operation of the FLI2200, as follows:

        0*   = The FLI2200 is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources).

        1   = The FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement.

Address 06$_H$: MODE2 Control Register. Default value 05$_H$

The eight bits in the MODE2 register control various deinterlacing functions, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	CSync	VITSEn	F30Hz	F30Inv	Force30	Motion$_1$	Motion$_0$	PComp
Default value	0	0	0	0	0	1	0	1

CSync: This bit controls the output syncs, as follows, as follows:

    0* = Horizontal sync appears on the H/CSYNCO output and vertical sync on the VSYNC/CREFO output.

    1 = Composite sync appears on the H/CSYNCO output and composite reference on the VSYNC/CREFO output.

VITSEn: This bit controls the use of the film mode flag which sometimes appears on line 22, as follows:

    0* = Film mode flag is ignored and the internal film mode detector is operational.

    1 = Film mode flag is used to control film mode in the deinterlacer.

F30Hz: This bit controls the film mode detector when the signal comes from a 525 line (NTSC) source, as follows:

    0* = Disabled the detection of 30 fps film using 2:2 pulldown detection in 525 line NTSC. This prevents the accidental detection of this mode when the source is video, not 30 fps film. Note that this does not disable 2:2 pulldown detection in 625 line PAL.

    1 = Allow detection of 30 fps film using 2:2 pulldown detection in NTSC.

F30Inv: This bit controls the 30 fps film operation when the field flag input is used for frame detection (Force30 = 1), as follows:

    0* = FLDIN = 1 identifies first field in frame.

    1 = FLDIN = 0 identifies first field in frame.

Force30: This bit controls the 30 fps film operation, as follows:

    0* = 30 fps film mode operation controlled by internal film mode detector.

    1 = 30 fps film mode operation controlled by FLDIN signal.

Motion$_{1-0}$: These bits set the motion processing mode in the deinterlacer, as follows:

    Motion$_{1-0}$ Mode

       0x   Test mode.

       10*   Normal operation

       11   Test mode.

PComp: This bit controls the operation of the PAL line averager, as follows:

    0 = PAL line averager will be operational when 625 line (PAL) source signals are detected.

    1* = PAL line averager disabled. Improved performance can be achieved with 625 line signals which have never been encoded into composite PAL format and therefore do no require line averaging to eliminate Hannover blinds.

Address 07$_H$: OUTPUT Control Register. Default value 10$_H$

The eight bits in the OUTPUT register control the following output functions, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	CSwap	ChrPhs	CIntDis	OBlnkEn	OFmtOvr	OFormat$_2$	OFormat$_1$	OFormat$_0$
Default value	0	0	0	1	0	0	0	0

CSwap: This bit controls the sequence of the chroma outputs prior to demultiplexing at the output, as follows:

    0* = Normal mode, Cb precedes Cr in Y Cb/Cr and Y/Cb/Cr modes and Cr and Cb appear on the corresponding busses in Y Cr Cb mode.

    1 = Inverted color mode. The Cb and Cr signals will be switched. R and B will also be swapped in the R G B mode.

ChrPhs: This bit delays the chroma output in the Y/Cb/Cr mode, as follows:

    0* = Normal mode, no delay

    1 = Chroma output is delayed by two luma pixels/one chroma pixel.

CIntDis: This bit controls the chroma interpolator, as follows:

    0* = Chroma interpolator enabled. This mode is only used to generate 4:4:4 Y Cr Cb outputs.

    1 = Chroma interpolator disabled. This is the normal mode of operation and must be selected for all 4:2:2 output formats.

Note: Selecting the 4:4:4 R G B output mode automatically enables the chroma interpolator.

OBlnkEn: This bit controls the output blanking, as follows:

    0 = Output blanking disabled. The output signal will be the same as the input in the blanking regions.

    1* = Output blanking enabled. The output signal will be blanked in the blanking regions regardless of the input signal.

OFmtOvr: The OFmtOvr bit is used to control the output format function, as follows:

    0* = The FLI2200 is configured to use the output format defined by the OFORMAT$_{2-0}$ pins, pins 59-61. The formats defined will be same as those defined for the OFormat$_{2-0}$ bits.

    1 = The FLI2200 is configured to use the output format defined by the OFormat$_{2-0}$ bits in this register, overriding the pin settings.

OFormat$_{2-0}$: These bits are used to define the format of the output signals, as follows:

    OFormat$_{2-0}$ Output signal format

    000* = R G B (4:4:4)

    001 = Y Cr Cb (4:2:2)

    010 = Y Cb/Cr + Y/Cb/Cr (double rate D1, with external/separate syncs)

    011 = Y Cb/Cr + Y/Cb/Cr (double rate D1, with embedded timing)

    100 = Y Pb Pr (4:2:2)

    101 = Y Pb/Pr

    110 = Y Cb Cr (4:4:4)

    111 = Test mode

The busses used for the multiplexed signals (Cb/Cr and Y/Cb/Cr) in modes 01x and 101 are determined by the settings of the COutSel bit in register 08$_H$, as shown on page 50.

Address 08$_H$: IOSEL (IOSELect) Control Register. Default value 52$_H$

The eight bits in the IOSEL register select the busses used for multiplexed signals, and set the film sync delay in the film mode detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	D1Valid	CInSel	COutSel	D1InSel$_1$	D1InSel$_0$	FSyncDel$_2$	FSyncDel$_1$	FSyncDel$_0$
Default value	R/O	1	0	1	0	0	1	0

D1Valid: This bit indicates the validity of the input in Y/Cb/Cr (D1) mode. It is a read only function. This bit is set as follows:

    0 = The FLI2200 has not been able to lock onto the input signal.

    1 = The FLI2200 has locked onto the input signal.

CInSel: This bit selects which bus is used for the multiplexed chroma input signal in the Y Cb/Cr input mode, as follows:

    0 = Multiplexed chroma signal Cb/Cr is input on the B/CbIN bus.

    1* = Multiplexed chroma signal Cb/Cr is input on the R/CrIN bus.

COutSel: This bit selects which bus is used for the multiplexed chroma output signal in the Y Cb/Cr output mode, as follows:

    0* = Multiplexed chroma signal Cb/Cr is output on the B/CbOUT bus.

          Multiplexed pseudo-D1 signal Y/Cb/Cr is output on the R/CrOUT bus.

    1 = Multiplexed chroma signal Cb/Cr is output on the R/CrOUT bus.

          Multiplexed pseudo-D1 signal Y/Cb/Cr is output on the B/CbOUT bus.

D1InSel$_{1-0}$: These bits set the input bus used for the D1 (Y/Cb/Cr) multiplexed input signal, as follows:

D1InSel$_{1-0}$	D1 bus
00	G/Y
01	G/Y
10*	B/Cb
11	R/Cr

FSyncDel$_{3-0}$: These bits set the delay in the film mode detector, as follows:

    0$_H$ = Minimum film sync delay, zero fields.

    2$_H$* = Default film sync delay, 2 fields.

    4$_H$ = Maximum film sync delay, 4 fields.

    5-7$_H$ = Not valid.

Address 09$_H$: IGAIN (Input Gain) Control Register. Default value 03$_H$

The two bits in the IGAIN register set the gain of the input signals after sync removal, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	x	x	x	x	x	x	YInGain	CInGain
Default value	0	0	0	0	0	0	1	1

YInGain: This bit sets the gain of the luma input path, as follows:

    0   = Gain = 1. This value must be used when there is no sync on the input signal and the input signal has a full scale range.

    1*   = Gain = 1.5625. This value can be used when there is sync on the input signal, allowing the signal to be stretched to full scale range after sync removal.

CInGain: This bit sets the gain of the luma input path, as follows:

    0   = Gain = 1. This value must be used when there is no sync on the luma input signal and the input signals have a full scale range.

    1*   = Gain = 1.5625. This value can be used when there is sync on the luma input signal if the chroma signal range matches that of the luma signal.

Note that SOnYG, bit 5 in register 00$_H$, overrides these bits when it is set low, forcing the gains to 1.

Address 0A$_H$: BSStart (Blanking Sampling Start) Control Register. Default value 02$_H$

The eight bits in the BSStart register set the start of the sampling period for the horizontal blanking level detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	BSStart$_7$	BSStart$_6$	BSStart$_5$	BSStart$_4$	BSStart$_3$	BSStart$_2$	BSStart$_1$	BSStart$_0$
Default value	0	1	0	0	1	0	1	0

BSStartN$_{7-0}$: These bits set the start of the 32-pixel sampling period for the blanking level detector. The adjustment is in 1 pixel increments relative to the start of the horizontal blanking interval, as follows:

BSStartN$_{7-0}$	Timing relative to start of blanking
00$_H$	0 pixels
4A$_H$*	74 pixels
FF$_H$	+127 pixels

Care should be taken to not allow the 32-pixel period extend beyond the end of the horizontal blanking interval.

Address 10_H: HSSTN (Horizontal Sync StarT/NTSC) Control Register. Default value 00_H

The eight bits in the HSSTN register set the start of the output horizontal sync pulse when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$HSStartN_7$	$HSStartN_6$	$HSStartN_5$	$HSStartN_4$	$HSStartN_3$	$HSStartN_2$	$HSStartN_1$	$HSStartN_0$
Default value	0	0	0	0	0	0	0	0

$HSStartN_{7-0}$: These bits set the start of the output horizontal sync pulse when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

$HSStartN_{7-0}$	Timing relative to default value
80_H	–128 pixels
00_H*	Default timing
7F_H	+127 pixels

Address 11_H: HSSPN (Horizontal Sync StoP/NTSC) Control Register. Default value 00_H

The eight bits in the HSSPN register set the end of the output horizontal sync pulse when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$HSStopN_7$	$HSStopN_6$	$HSStopN_5$	$HSStopN_4$	$HSStopN_3$	$HSStopN_2$	$HSStopN_1$	$HSStopN_0$
Default value	0	0	0	0	0	0	0	0

$HSStopN_{7-0}$: These bits set the end of the output horizontal sync pulse when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

$HSStopN_{7-0}$	Timing relative to default value
80_H	–128 pixels
00_H*	Default timing
7F_H	+127 pixels

Address 12$_H$: HRSTN (Horizontal **R**eference **S**tar**T**/NTSC**) Control Register. Default value 00$_H$**

The eight bits in the HRSTN register set the start of the output horizontal reference signal when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HRStartN$_7$	HRStartN$_6$	HRStartN$_5$	HRStartN$_4$	HRStartN$_3$	HRStartN$_2$	HRStartN$_1$	HRStartN$_0$
Default value	0	0	0	0	0	0	0	0

HRStartN$_{7-0}$: These bits set the start of the output horizontal reference signal when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

HRStartN$_{7-0}$	Timing relative to default value
80$_H$	–128 pixels
00$_H$*	Default timing
7F$_H$	+127 pixels

Address 13$_H$: HRSPN (Horizontal **R**eference **S**to**P**/NTSC**) Control Register. Default value 00$_H$**

The eight bits in the HRSPN register set the end of the output horizontal reference signal when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HRStopN$_7$	HRStopN$_6$	HRStopN$_5$	HRStopN$_4$	HRStopN$_3$	HRStopN$_2$	HRStopN$_1$	HRStopN$_0$
Default value	0	0	0	0	0	0	0	0

HRStopN$_{7-0}$: These bits set the end of the output horizontal reference signal when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

HRStopN$_{7-0}$	Timing relative to default value
80$_H$	–128 pixels
00$_H$*	Default timing
7F$_H$	+127 pixels

Address 14$_H$: VMSN (Vertical timing MS bits/NTSC) Control Register. Default value 00$_H$

The eight bits in the VMSN register are the most significant bits for the vertical sync and reference timing signals when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VSStartN$_5$	VSStartN$_4$	VSStopN$_5$	VSStopN$_4$	VRStartN$_5$	VRStartN$_4$	VRStopN$_5$	VRStopN$_4$
Default value	0	0	0	0	0	0	0	0

VSStartN$_{5-4}$: These bits, in conjunction with bits 7-4 in register 15$_H$, set the start of the output vertical sync pulse when the input signal comes from a 525 line (NTSC) source. These are the most significant bits of a 6-bit value. See description of register 15$_H$ for details.

VSStopN$_{5-4}$: These bits, in conjunction with bits 3-0 in register 15$_H$, set the end of the output vertical sync pulse when the input signal comes from a 525 line (NTSC) source. These are the most significant bits of a 6-bit value. See description of register 15$_H$ for details.

VRStartN$_{5-4}$: These bits, in conjunction with bits 7-4 in register 16$_H$, set the start of the output vertical reference signal when the input signal comes from a 525 line (NTSC) source. These are the most significant bits of a 6-bit value. See description of register 16$_H$ for details.

VRStopN$_{5-4}$: These bits, in conjunction with bits 3-0 in register 16$_H$, set the end of the output vertical reference signal when the input signal comes from a 525 line (NTSC) source. These are the most significant bits of a 6-bit value. See description of register 16$_H$ for details.

Address 15$_H$: VSTN (Vertical Sync Timing/NTSC) Control Register. Default value 00$_H$

The eight bits in the VSTN register set the start and end of the output vertical sync pulse when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VSStartN$_3$	VSStartN$_2$	VSStartN$_1$	VSStartN$_0$	VSStopN$_3$	VSStopN$_2$	VSStopN$_1$	VSStopN$_0$
Default value	0	0	0	0	0	0	0	0

VSStartN$_{3-0}$: These bits, in conjunction with bits 7-6 in register 14$_H$, set the start of the output vertical sync pulse when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VSStartN$_{5-0}$	Timing relative to default value
20$_H$	–32 lines
00$_H$*	Default timing
1F$_H$	+31 lines

VSStopN$_{3-0}$: These bits, in conjunction with bits 5-4 in register 14$_H$, set the end of the output vertical sync pulse when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VSStopN$_{5-0}$	Timing relative to default value
20$_H$	–32 lines
00$_H$*	Default timing
1F$_H$	+31 lines

Address 16$_H$: VRTN (Vertical Reference Timing/NTSC) Control Register. Default value 00$_H$

The eight bits in the VRTN register set the start and end of the output vertical reference signal when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VRStartN$_3$	VRStartN$_2$	VRStartN$_1$	VRStartN$_0$	VRStopN$_3$	VRStopN$_2$	VRStopN$_1$	VRStopN$_0$
Default value	0	0	0	0	0	0	0	0

VRStartN$_{3-0}$: These bits, in conjunction with bits 7-6 in register 14$_H$, set the start of the output vertical reference signal when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VRStartN3-0	Timing relative to default value
40$_H$	–32 lines
00$_H$*	Default timing
3F$_H$	+31 lines

VRStopN$_{3-0}$: These bits, in conjunction with bits 5-4 in register 14$_H$, set the end of the output vertical reference signal when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VRStopN$_{5-0}$	Timing relative to default value
40$_H$	–32 lines
00$_H$*	Default timing
3F$_H$	+31 lines

Address 17$_H$: VBIMSN (VBI timing MS bits/NTSC) Control Register. Default value 00$_H$

The six bits in the VBIMSN register are the most significant bits for the VBI timing signals when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	x	VBStartN$_4$	x	VBStopN$_4$	VBIStartN$_5$	VBIStartN$_4$	VBIStopN$_5$	VBIStopN$_4$
Default value	x	0	x	0	0	0	0	0

VBStartN$_4$: This bit, in conjunction with bits 7-4 in register 18$_H$, set the start of the output vertical blanking signal when the input signal comes from a 525 line (NTSC) source. This is the most significant bit of a 5-bit value. See description of register 18$_H$ for details.

VBStopN$_4$: This bit, in conjunction with bits 3-0 in register 18$_H$, set the end of the output vertical blanking signal when the input signal comes from a 525 line (NTSC) source. This is the most significant bit of a 5-bit value. See description of register 18$_H$ for details.

VBIStartN$_{5-4}$: These bits, in conjunction with bits 7-4 in register 19$_H$, set the start of the output VBI data pass-through signal when the input signal comes from a 525 line (NTSC) source. These are the most significant bits of a 6-bit value. See description of register 19$_H$ for details.

VBIStopN$_{5-4}$: These bits, in conjunction with bits 3-0 in register 19$_H$, set the end of the output VBI data pass-through signal when the input signal comes from a 525 line (NTSC) source. These are the most significant bits of a 6-bit value. See description of register 19$_H$ for details.

Address 18$_H$: VBTN (Vertical **B**lanking **T**iming/NTSC**) Control Register. Default value 00$_H$**

The eight bits in the VBTN register set the start and end of the output vertical blanking signal when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VBStartN$_3$	VBStartN$_2$	VBStartN$_1$	VBStartN$_0$	VBStopN$_3$	VBStopN$_2$	VBStopN$_1$	VBStopN$_0$
Default value	0	0	0	0	0	0	0	0

VBStartN$_{3-0}$: These bits, in conjunction with bit 6 in register 17$_H$, set the start of the output vertical blanking signal when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBStartN$_{4-0}$	Timing relative to default value
10$_H$	−16 lines
00$_H$*	Default timing
0F$_H$	+15 lines

VBStopN$_{3-0}$: These bits, in conjunction with bit 4 in register 17$_H$, set the end of the output vertical blanking signal when the input signal comes from a 525 line (NTSC) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBStopN$_{5-0}$	Timing relative to default value
10$_H$	−16 lines
00$_H$*	Default timing
0F$_H$	+15 lines

Address 19$_H$: VBITN (VBI data **T**iming/**NTSC**) **Control Register. Default value 28$_H$**

The eight bits in the VBTN register set the start and end of the output VBI data pass-through signal when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VBIStartN$_3$	VBIStartN$_2$	VBIStartN$_1$	VBIStartN$_0$	VBIStopN$_3$	VBIStopN$_2$	VBIStopN$_1$	VBIStopN$_0$
Default value	0	0	1	0	1	0	0	0

VBIStartN$_{3-0}$: These bits, in conjunction with bits 3-2 in register 17$_H$, set the start of the output VBI data pass-through signal when the input signal comes from a 525 line (NTSC) source. This allows a selected contiguous group of lines during the VBI period to be unblanked to pass through the data on these lines. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBIStartN$_{4-0}$	Timing relative to default value
20$_H$	–32 lines
02$_H$*	Default timing
1F$_H$	+31 lines

VBStopN$_{3-0}$: These bits, in conjunction with bits 1-0 in register 17$_H$, set the end of the output VBI data pass-through signal when the input signal comes from a 525 line (NTSC) source. This allows a selected contiguous group of lines during the VBI period to be unblanked to pass through the data on these lines. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBStopN$_{4-0}$	Timing relative to default value
20$_H$	–32 lines
00$_H$*	Default timing
1F$_H$	+31 lines

Address 20$_H$: HSSTP (Horizontal **S**ync **S**tar**T**/**PAL**) **Control Register. Default value 00$_H$**

The eight bits in the HSSTP register set the start of the output horizontal sync pulse when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HSStartP$_7$	HSStartP$_6$	HSStartP$_5$	HSStartP$_4$	HSStartP$_3$	HSStartP$_2$	HSStartP$_1$	HSStartP$_0$
Default value	0	0	0	0	0	0	0	0

HSStartP$_{7-0}$: These bits, in conjunction with bits 7-6 in register 24$_H$, set the start of the output horizontal sync pulse when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

HSStartP$_{9-0}$	Timing relative to default value
200$_H$	–512 pixels
000$_H$*	Default timing
1FF$_H$	+511 pixels

Address 21$_H$: HSSPP (Horizontal **S**ync **S**to**P**/PAL) **Control Register. Default value 00$_H$**

The eight bits in the HSSPP register set the end of the output horizontal sync pulse when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HSStopP$_7$	HSStopP$_6$	HSStopP$_5$	HSStopP$_4$	HSStopP$_3$	HSStopP$_2$	HSStopP$_1$	HSStopP$_0$
Default value	0	0	0	0	0	0	0	0

HSStopP$_{7-0}$:   These bits, in conjunction with bits 5-4 in register 24$_H$, set the end of the output horizontal sync pulse when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

HSStopP$_{7-0}$	Timing relative to default value
200$_H$	–512 pixels
000$_H$*	Default timing
1FF$_H$	+511 pixels

Address 22$_H$: HRSTP (Horizontal **R**eference **S**tar**T**/PAL) **Control Register. Default value 00$_H$**

The eight bits in the HRSTP register set the start of the output horizontal reference signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HRStartP$_7$	HRStartP$_6$	HRStartP$_5$	HRStartP$_4$	HRStartP$_3$	HRStartP$_2$	HRStartP$_1$	HRStartP$_0$
Default value	0	0	0	0	0	0	0	0

HRStartP$_{7-0}$:   These bits, in conjunction with bits 3-2 in register 24$_H$, set the start of the output horizontal reference signal when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

HRStartP$_{7-0}$	Timing relative to default value
200$_H$	–512 pixels
000$_H$*	Default timing
1FF$_H$	+511 pixels

Address 23$_H$: HRSPP (Horizontal **R**eference **S**to**P**/PAL) **Control Register. Default value 00$_H$**

The eight bits in the HRSPP register set the end of the output horizontal reference signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HRStopP$_7$	HRStopP$_6$	HRStopP$_5$	HRStopP$_4$	HRStopP$_3$	HRStopP$_2$	HRStopP$_1$	HRStopP$_0$
Default value	0	0	0	0	0	0	0	0

HRStopP$_{7-0}$:   These bits, in conjunction with bits 1-0 in register 24$_H$, set the end of the output horizontal reference signal when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

HRStopP$_{7-0}$	Timing relative to default value
200$_H$	–512 pixels
000$_H$*	Default timing
1FF$_H$	+511 pixels

Address 24$_H$: HMSP (Horizontal timing **MS** bits**/PAL) Control Register. Default value 00$_H$**

The eight bits in the HMSP register are the most significant bits for the vertical sync and reference timing signals when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HSStartP$_9$	HSStartP$_8$	HSStopP$_9$	HSStopP$_8$	HRStartP$_9$	HRStartP$_8$	HRStopP$_9$	HRStopP$_8$
Default value	0	0	0	0	0	0	0	0

HSStartP$_{9\text{-}8}$:   These bits, in conjunction with bits 7-0 in register 20$_H$, set the start of the output vertical sync pulse when the input signal comes from a 625 line (PAL) source. These are the most significant bits of a 10-bit value. See description of register 20$_H$ for details.

HSStopP$_{9\text{-}8}$:   These bits, in conjunction with bits 7-0 in register 21$_H$, set the end of the output vertical sync pulse when the input signal comes from a 625 line (PAL) source. These are the most significant bits of a 10-bit value. See description of register 21$_H$ for details.

HRStartP$_{9\text{-}8}$:   These bits, in conjunction with bits 7-0 in register 22$_H$, set the start of the output vertical reference signal when the input signal comes from a 625 line (PAL) source. These are the most significant bits of a 10-bit value. See description of register 22$_H$ for details.

HRStopP$_{9\text{-}8}$:   These bits, in conjunction with bits 7-0 in register 23$_H$, set the end of the output vertical reference signal when the input signal comes from a 625 line (PAL) source. These are the most significant bits of a 10-bit value. See description of register 23$_H$ for details.

Address 25$_H$: VSSTP (Vertical **S**ync Star**T/PAL) Control Register. Default value 00$_H$**

The eight bits in the VSTP register set the start of the output vertical sync pulse when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VSStartP$_7$	VSStartP$_6$	VSStartP$_5$	VSStartP$_4$	VSStartP$_3$	VSStartP$_2$	VSStartP$_1$	VSStartP$_0$
Default value	0	0	0	0	0	0	0	0

VSStartP$_{7\text{-}0}$:   These bits set the start of the output vertical sync pulse when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VSStartP$_{7\text{-}0}$	Timing relative to default value
80$_H$	–128 lines
00$_H$*	Default timing
7F$_H$	+127 lines

Address 26$_H$: VSSPP (Vertical Sync StoP/PAL) Control Register. Default value 00$_H$

The eight bits in the VSSPP register set the end of the output vertical sync pulse when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VSStopP$_7$	VSStopP$_6$	VSStopP$_5$	VSStopP$_4$	VSStopP$_3$	VSStopP$_2$	VSStopP$_1$	VSStopP$_0$
Default value	0	0	0	0	0	0	0	0

VSStopP$_{7-0}$: These bits set the end of the output vertical sync pulse when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VSStopP$_{7-0}$	Timing relative to default value
80$_H$	–128 lines
00$_H$*	Default timing
7F$_H$	+127 lines

Address 27$_H$: VRSTP (Vertical Reference StarT/PAL) Control Register. Default value 01$_H$

The eight bits in the VRSTP register set the start of the output vertical reference signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VRStartP$_7$	VRStartP$_6$	VRStartP$_5$	VRStartP$_4$	VRStopP$_3$	VRStopP$_2$	VRStopP$_1$	VRStopP$_0$
Default value	0	0	0	0	0	0	0	1

VRStartP$_{7-0}$: These bits set the start of the output vertical reference signal when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VRStartP$_{7-0}$	Timing relative to default value
80$_H$	–129 lines
01$_H$*	Default timing
7F$_H$	+126 lines

Address 28$_H$: VRSPP (Vertical Reference StoP/PAL) Control Register. Default value 01$_H$

The eight bits in the VRSPP register set the end of the output vertical reference signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VRStopP$_7$	VRStopP$_6$	VRStopP$_5$	VRStopP$_4$	VRStopP$_3$	VRStopP$_2$	VRStopP$_1$	VRStopP$_0$
Default value	0	0	0	0	0	0	0	1

VRStopP$_{7-0}$: These bits set the end of the output vertical reference signal when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VRStopP$_{7-0}$	Timing relative to default value
80$_H$	–129 lines
01$_H$*	Default timing
7F$_H$	+126 lines

Address 29$_H$: VBSTP (Vertical **B**lanking **S**tar**T/PAL) Control Register. Default value 01$_H$**

The eight bits in the VBSTP register set the start of the output vertical blanking signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VBStartP$_7$	VBStartP$_6$	VBStartP$_5$	VBStartP$_4$	VBStartP$_3$	VBStartP$_2$	VBStartP$_1$	VBStartP$_0$
Default value	0	0	0	0	0	0	0	1

VBStartP$_{7-0}$: These bits set the start of the output vertical blanking signal when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBStartP$_{7-0}$	Timing relative to default value
80$_H$	–129 lines
01$_H$*	Default timing
7F$_H$	+126 lines

Address 2A$_H$: VBSPP (Vertical **B**lanking **S**to**P/PAL) Control Register. Default value 00$_H$**

The eight bits in the VBSTP register set the end of the output vertical blanking signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VBStopP$_7$	VBStopP$_6$	VBStopP$_5$	VBStopP$_4$	VBStopP$_3$	VBStopP$_2$	VBStopP$_1$	VBStopP$_0$
Default value	0	0	0	0	0	0	0	0

VBStopP$_{7-0}$: These bits set the end of the output vertical blanking signal when the input signal comes from a 625 line (PAL) source. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBStopP$_{7-0}$	Timing relative to default value
80$_H$	–128 lines
00$_H$*	Default timing
7F$_H$	+127 lines

Address 2B$_H$: VBISTP (VBI data **StarT/PAL) Control Register. Default value 02$_H$**

The eight bits in the VBISTP register set the start of the output VBI data pass-through signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VBIStartP$_7$	VBIStartP$_6$	VBIStartP$_5$	VBIStartP$_4$	VBIStartP$_3$	VBIStartP$_2$	VBIStartP$_1$	VBIStartP$_0$
Default value	0	0	0	0	0	0	1	0

VBIStartP$_{7-0}$: These bits set the start of the output VBI data pass-through signal when the input signal comes from a 625 line (PAL) source. This allows a selected contiguous group of lines during the VBI period to be unblanked to pass through the data on these lines. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBIStartP$_{7-0}$	Timing relative to default value
80$_H$	−130 lines
02$_H$*	Default timing
7F$_H$	+125 lines

Address 2C$_H$: VBISPP (VBI data **StoP/PAL) Control Register. Default value 08$_H$**

The eight bits in the VBISPP register set the end of the output VBI data pass-through signal when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	VBIStartP$_3$	VBIStartP$_2$	VBIStartP$_1$	VBIStartP$_0$	VBIStopP$_3$	VBIStopP$_2$	VBIStopP$_1$	VBIStopP$_0$
Default value	0	0	0	0	1	0	0	0

VBIStopP$_{7-0}$: These bits set the end of the output VBI data pass-through signal when the input signal comes from a 625 line (PAL) source. This allows a selected contiguous group of lines during the VBI period to be unblanked to pass through the data on these lines. The number is a signed, two's complement value. The adjustment is in 1 line increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

VBStopP$_{7-0}$	Timing relative to default value
80$_H$	−136 lines
08$_H$*	Default timing
7F$_H$	+119 lines

Address 2E$_H$: HOVR (Horizontal **O**verride**) Control Register. Default value 04$_H$**

The four bits in the HOVR register control the horizontal line length, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Test	x	x	HSizeOvr	x	HSize$_{10}$	HSize$_9$	HSize$_8$
Default value	0	x	x	0	x	1	0	0

Test: This bit is used to put the device into a special test mode, as follows:

0* = Normal operating mode.

1 = Test mode, not normally used.

x: This bit is not used and does not exist physically.

HSizeOvr: This bit controls the horizontal line length, as follows:

0* = Line length is set automatically set according to ITU-R BT656 and the video standard, i.e., 858 pixels for 525 line (NTSC) signals and 864 pixels for 625 line (PAL) signals. When the device is used with external memory for fully adaptive deinterlacing this bit must be set low, i.e., the NOMEM pin is tied low or the NMOvr bit is set high and the NoMem bit is set low.

1 = Line length is set by the number of clock cycles in each horizontal period, as determined by the horizontal sync or reference input signal. In this mode the HSize register must be programmed to match this number for correct operation. This mode can only be used when the FLI2200 is configured in the stand-alone mode with no external memory (intra-field deinterlacing only), i.e., the NOMEM pin is tied high or the NMOvr and NoMem bits are set high. When the device is used with external memory for fully adaptive deinterlacing HSizeOvr must be set low..

HSize$_{10-8}$: These bits, in conjunction with bits 7-0 in register 2F$_H$, set the total line length when the HSizeOvr bit is set high . See description of register 2F$_H$ for details.

Address 2F$_H$: HSIZE (Horizontal **Size) Control Register. Default value 4C$_H$**

The eight bits in the HSIZE register control the horizontal line length, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	HSize$_7$	HSize$_6$	HSize$_5$	HSize$_4$	HSize$_3$	HSize$_2$	HSize$_1$	HSize$_0$
Default value	0	1	0	0	1	1	0	0

HSize$_{7-0}$: These bits, in conjunction with bits 3-0 in register 2E$_H$, set the total line length when the HSizeOvr bit is set high . HSize$_{10-0}$ must be programmed to be equal to the total number of pixels. The maximum allowable number is 1104 and the default value is 1100.

Address 30$_H$: INV1 (Invert) Control Register. Default value 05$_H$

The eight bits in the INV1 register control the polarities of some signals and other related functions, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	ISyncInv	ORefInv	OSyncInv	DatBlnk	HDatBlnk	Test	IMode	CCSOn
Default value	0	0	0	0	0	1	0	1

ISyncInv: This bit is set according to the polarity of the sync inputs, as follows:

    0*   = Normal sync inputs (active high).

    1   = Inverted sync inputs (active low).

ORefInv: This controls the polarity of the H and V reference outputs, as follows:

    0*   = Normal reference outputs (active high).

    1   = Inverted reference outputs (active low).

OSyncInv: This controls the polarity of the sync outputs, as follows:

    0*   = Normal sync outputs (active high).

    1   = Inverted sync outputs (active low).

DatBlnk: This controls the passing of ancillary data, as follows:

    0*   = Ancillary data in the vertical blanking interval is not passed.

    1   = Ancillary data in the vertical blanking interval is passed according to the settings of the HBStartN/P$_{4-0}$/HBStopN/P$_{5-0}$ and VBStartN/P$_{4-0}$/VBStopN/P$_{5-0}$ bits in registers 17$_H$-19$_H$ (NTSC) or 27$_H$-29$_H$ (PAL).

HDatBlnk: This controls the passing of ancillary data in the horizontal blanking interval, as follows:

    0*   = Ancillary data in the horizontal blanking interval is not passed.

    1   = Ancillary data in the horizontal blanking interval is passed. Note that when the deinterlacer is operating in interpolation mode, either adaptively or in stand-alone (NoMem) mode, no horizontal data will appear on the interpolated lines, only on the direct lines..

Test: This controls the operation of the deinterlacer, as follows:

    0   = Test mode.

    1*   = Normal operating mode.

Test: This controls the operation of the deinterlacer, as follows:

    0*   = Normal operating mode.

    1   = Test mode.

CCSOn: This controls the operation of the Cross Color Suppressor function, as follows:

    0   = Cross Color suppressor disabled. This primarily a test mode.

    1*   = Cross Color suppressor enabled. This is the normal operating mode.

Address 31$_H$: EDBL (EDit Blank Left) Control Register. Default value E0$_H$

The eight bits in the EDBL register control the position of the left hand side of the area of the image used in the Bad Edit Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkL$_7$	EdBlnkL$_6$	EdBlnkL$_5$	EdBlnkL$_4$	EdBlnkL$_3$	EdBlnkL$_2$	EdBlnkL$_1$	EdBlnkL$_0$
Default value	1	1	1	0	0	0	0	0

EdBlkL$_{7-0}$: These bits, in conjunction with bit 7 in register 36$_H$, set the position of the left hand side of the area of the image used in the Bad Edit Detector. The value is the number of pixels from the start of active video.

Address 32$_H$: EDBR (EDit Blank Right) Control Register. Default value 52$_H$

The eight bits in the EDBR register control the position of the right hand side of the area of the image used in the Bad Edit Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkR$_7$	EdBlnkR$_6$	EdBlnkR$_5$	EdBlnkR$_4$	EdBlnkR$_3$	EdBlnkR$_2$	EdBlnkR$_1$	EdBlnkR$_0$
Default value	0	1	0	1	0	0	1	0

EdBlkR$_{7-0}$: These bits, in conjunction with bits 6 and 5 in register 36$_H$, set the position of the right hand side of the area of the image used in the Bad Edit Detector. The value is the number of pixels from the start of active video.

Address 33$_H$: EDBT (EDit Blank Top) Control Register. Default value 42$_H$

The eight bits in the EDBT register control the position of the top of the area of the image used in the Bad Edit Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkT$_7$	EdBlnkT$_6$	EdBlnkT$_5$	EdBlnkT$_4$	EdBlnkT$_3$	EdBlnkT$_2$	EdBlnkT$_1$	EdBlnkT$_0$
Default value	0	1	0	0	0	0	1	0

EdBlkT$_{7-0}$: These bits, in conjunction with bit 4 in register 36$_H$, set the position of the top of the area of the image used in the Bad Edit Detector. The value is the number of pixels from the start of active video.

Address 34$_H$: EDBBN (EDit Blank Bottom/NTSC) Control Register. Default value F4$_H$

The eight bits in the EDBBN register control the position of the bottom of the area of the image used in the Bad Edit Detector when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	EdBlnkT$_7$	EdBlnkT$_6$	EdBlnkT$_5$	EdBlnkT$_4$	EdBlnkT$_3$	EdBlnkT$_2$	EdBlnkT$_1$	EdBlnkT$_0$
Default value	1	1	1	1	0	1	0	0

EdBlkBN$_{7-0}$: These bits, in conjunction with bits 3 and 2 in register 36$_H$, set the position of the bottom of the area of the image used in the Bad Edit Detector when the input signal comes from a 525 line (NTSC) source. The value is the number of lines from the start of active video.

Address 35_H: EDBBP (EDit Blank Bottom/PAL) Control Register. Default value 58_H

The eight bits in the EDBBP register control the position of the bottom of the area of the image used in the Bad Edit Detector when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$EdBlnkT_7$	$EdBlnkT_6$	$EdBlnkT_5$	$EdBlnkT_4$	$EdBlnkT_3$	$EdBlnkT_2$	$EdBlnkT_1$	$EdBlnkT_0$
Default value	0	1	0	1	1	0	0	0

$EdBlkBN_{7-0}$: These bits, in conjunction with bits 3 and 2 in register 36_H, set the position of the bottom of the area of the image used in the Bad Edit Detector when the input signal comes from a 625 line (PAL) source. The value is the number of lines from the start of active video.

Address 36_H: EDBMS (EDit Blank Most significant bits) Control Register. Default value 66_H

The eight bits in the EDBMS register control the position of the area of the image used in the Bad Edit Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$EdBlnkL_8$	$EdBlnkR_9$	$EdBlnkR_8$	$EdBlnkT_8$	$EdBlnkBN_9$	$EdBlnkBN_8$	$EdBlnkBP_9$	$EdBlnkBP_8$
Default value	0	1	1	0	0	1	1	0

$EdBlkL_8$: This bit, in conjunction with bits 7-0 in register 31_H, sets the position of the left hand side of the area of the image used in the Bad Edit Detector. See description of register 31_H for details.

$EdBlkR_{9-8}$: These bits, in conjunction with bits 7-0 in register 32_H, set the position of the right hand side of the area of the image used in the Bad Edit Detector. See description of register 32_H for details.

$EdBlkT_8$: This bit, in conjunction with bits 7-0 in register 33_H, sets the position of the top of the area of the image used in the Bad Edit Detector. See description of register 33_H for details.

$EdBlkBN_{9-8}$: These bits, in conjunction with bits 7-0 in register 34_H, set the position of the bottom of the area of the image used in the Bad Edit Detector when the input signal comes from a 625 line (PAL) source. See description of register 34_H for details.

$EdBlkBP_{9-8}$: These bits, in conjunction with bits 7-0 in register 35_H, set the position of the bottom of the area of the image used in the Bad Edit Detector when the input signal comes from a 625 line (PAL) source. See description of register 35_H for details.

Address 37_H: FMBL (FilM Blank Left) Control Register. Default value $E0_H$

The eight bits in the FMBL register control the position of the left hand side of the area of the image used in the Film Mode Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	$FmBlnkL_7$	$FmBlnkL_6$	$FmBlnkL_5$	$FmBlnkL_4$	$FmBlnkL_3$	$FmBlnkL_2$	$FmBlnkL_1$	$FmBlnkL_0$
Default value	1	1	1	0	0	0	0	0

$FmBlkL_{7-0}$: These bits, in conjunction with bit 7 in register $3C_H$, set the position of the left hand side of the area of the image used in the Film Mode Detector. The value is the number of pixels from the start of active video.

Address 38$_H$: FMBR (FilM Blank Right) Control Register. Default value 58$_H$

The eight bits in the FMBR register control the position of the right hand side of the area of the image used in the Film Mode Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	FmBlnkR$_7$	FmBlnkR$_6$	FmBlnkR$_5$	FmBlnkR$_4$	FmBlnkR$_3$	FmBlnkR$_2$	FmBlnkR$_1$	FmBlnkR$_0$
Default value	0	1	0	1	1	0	0	0

FmBlkR$_{7-0}$:　These bits, in conjunction with bits 6 and 5 in register 3C$_H$, set the position of the right hand side of the area of the image used in the Film Mode Detector. The value is the number of pixels from the start of active video.

Address 39$_H$: FMBT (FilM Blank Top) Control Register. Default value 42$_H$

The eight bits in the FMBT register control the position of the top of the area of the image used in the Film Mode Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	FmBlnkT$_7$	FmBlnkT$_6$	FmBlnkT$_5$	FmBlnkT$_4$	FmBlnkT$_3$	FmBlnkT$_2$	FmBlnkT$_1$	FmBlnkT$_0$
Default value	0	1	0	0	0	0	1	0

FmBlkT$_{7-0}$:　These bits, in conjunction with bit 4 in register 3C$_H$, set the position of the top of the area of the image used in the Film Mode Detector. The value is the number of pixels from the start of active video.

Address 3A$_H$: FMBBN (FilM Blank Bottom/NTSC) Control Register. Default value F4$_H$

The eight bits in the FMBBN register control the position of the bottom of the area of the image used in the Film Mode Detector when the input signal comes from a 525 line (NTSC) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	FmBlnkT$_7$	FmBlnkT$_6$	FmBlnkT$_5$	FmBlnkT$_4$	FmBlnkT$_3$	FmBlnkT$_2$	FmBlnkT$_1$	FmBlnkT$_0$
Default value	1	1	1	1	0	1	0	0

FmBlkBN$_{7-0}$:　These bits, in conjunction with bits 3 and 2 in register 3C$_H$, set the position of the top of the area of the image used in the Film Mode Detector when the input signal comes from a 525 line (NTSC) source. The value is the number of lines from the start of active video.

Address 3B$_H$: FMBBP (FilM Blank Bottom/PAL) Control Register. Default value 58$_H$

The eight bits in the FMBBP register control the position of the bottom of the area of the image used in the Film Mode Detector when the input signal comes from a 625 line (PAL) source, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	FmBlnkT$_7$	FmBlnkT$_6$	FmBlnkT$_5$	FmBlnkT$_4$	FmBlnkT$_3$	FmBlnkT$_2$	FmBlnkT$_1$	FmBlnkT$_0$
Default value	0	1	0	1	1	0	0	0

FmBlkBN$_{7-0}$:　These bits, in conjunction with bits 1 and 0 in register 3C$_H$, set the position of the top of the area of the image used in the Film Mode Detector when the input signal comes from a 625 line (PAL) source. The value is the number of lines from the start of active video.

Address 3C$_H$: FMBMS (**F**ilm **B**lank **M**ost **S**ignificant bits) **Control Register. Default value 66$_H$**

The eight bits in the FMBMS register control the position of the area of the image used in the Film Mode Detector, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	FmBlnkL$_8$	FmBlnkR$_9$	FmBlnkR$_8$	FmBlnkT$_8$	FmBlnkBN$_9$	FmBlnkBN$_8$	FmBlnkBP$_9$	FmBlnkBP$_8$
Default value	0	1	1	0	0	1	1	0

EdBlkL$_8$: This bit, in conjunction with bits 7-0 in register 31$_H$, sets the position of the left hand side of the area of the image used in the Film Mode Detector. See description of register 31$_H$ for details.

EdBlkR$_{9-8}$: These bits, in conjunction with bits 7-0 in register 32$_H$, set the position of the right hand side of the area of the image used in the Film Mode Detector. See description of register 32$_H$ for details.

EdBlkT$_8$: This bit, in conjunction with bits 7-0 in register 33$_H$, sets the position of the top of the area of the image used in the Film Mode Detector. See description of register 33$_H$ for details.

EdBlkBN$_{9-8}$: These bits, in conjunction with bits 7-0 in register 34$_H$, set the position of the bottom of the area of the image used in the Film Mode Detector when the input signal comes from a 625 line (PAL) source. See description of register 34$_H$ for details.

EdBlkBP$_{9-8}$: These bits, in conjunction with bits 7-0 in register 35$_H$, set the position of the bottom of the area of the image used in the Film Mode Detector when the input signal comes from a 625 line (PAL) source. See description of register 35$_H$ for details.

Address 3D$_H$ through Address 54$_H$: Test Registers

These 24 registers are used purely for test purposes and should not be changed at any time for normal operation. The default values are listed below for reference only.

Address	Default value	Address	Default value
3D$_H$	14$_H$	49$_H$	37$_H$
3E$_H$	0E$_H$	4A$_H$	1C$_H$
3F$_H$	60$_H$	4B$_H$	58$_H$
40$_H$	05$_H$	4C$_H$	38$_H$
41$_H$	0C$_H$	4D$_H$	00$_H$
42$_H$	14$_H$	4E$_H$	07$_H$
43$_H$	D5$_H$	4F$_H$	04$_H$
44$_H$	28$_H$	50$_H$	14$_H$
45$_H$	64$_H$	51$_H$	18$_H$
46$_H$	08$_H$	52$_H$	06$_H$
47$_H$	70$_H$	53$_H$	30$_H$
48$_H$	C0$_H$	54$_H$	30$_H$

Address 60$_H$: PLL Control Register 0. Default value 18$_H$

The eight bits in the PLL0 register set the pre-divider factor M in the PLL, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	MDiv$_7$	MDiv$_6$	MDiv$_5$	MDiv$_4$	MDiv$_3$	MDiv$_2$	MDiv$_1$	MDiv$_0$
Default value	0	0	0	1	1	0	0	0

MDiv$_{7-0}$: The pre-divider divides the input pixel clock by the factor M. The requirement is that these bits be used to set the M pre-divider factor in the PLL according to the input pixel clock frequency, so that $1 \text{ MHz} \leq f_{CLKIN}/M \leq 2 \text{ MHz}$. PDiv should then be set so that $2^{(6-PDiv)} = MDiv$. The values will be:

f$_{CLKIN}$	MDiv	NDiv	PDiv
8 to 16 MHz	08$_H$	08$_H$	3$_H$
16 to 32 MHz	10$_H$	10$_H$	2$_H$
32 to 54 MHz	20$_H$	20$_H$	1$_H$

Note that these registers will be programmed automatically if the PLLOvr bit, bit 3 in register 62$_H$, is set low.

Address 61$_H$: PLL Control Register 1. Default value 30$_H$

The eight bits in the PLL1 register set the divider factor N in the PLL, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	NDiv$_7$	NDiv$_6$	NDiv$_5$	NDiv$_4$	NDiv$_3$	NDiv$_2$	NDiv$_1$	NDiv$_0$
Default value	0	0	1	1	0	0	0	0

NDiv$_{7-0}$: These bits set the feedback division factor N in the PLL. This allows the clocks in the FLI2200 to be set up independently for test purposes. For normal operation, NDiv should always be set to be the same as MDiv. See description of register 60$_H$ for more details.

Address 62$_H$: PLL Control Register 2. Default value 02$_H$

The MSB is a read-only bit and the other seven bits in the PLL2 register control the operation of the clock generation PLL, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Lock	x	Disable	PByp	PLLOvr	PDiv$_2$	PDiv$_1$	PDiv$_0$
Default value	R/O	x	0	0	0	0	1	0

Lock
This bit indicates the lock status of the PLL, as shown below. It is a read-only (R/O) function.

    0 = PLL not locked.

    1 = PLL locked.

x:
This bit is not used and does not exist physically.

Disable:
This bit allows the PLL to be disabled for test purposes, as follows:

    0* = PLL is enabled. This is the normal mode of operation.

    1 = PLL is disabled for test purposes.

PByp:
This bit allows the PLL to be bypassed for test purposes, as follows:

    0* = PLL is not bypassed. This is the normal mode of operation.

    1 = PLL is bypassed.

PLLOvr:
This bit controls the programming of the PLL, as follows:

    0* = PLL registers are automatically programmed according to the input signal format selected. It will be programmed for a 13.5 MHz input clock frequency (PDiv = 2, NDiv = 30$_H$, MDiv = 0C$_H$) unless the D1 (Y/Cb/Cr) input format is selected, in which case it will be programmed for a 27 MHz clock (PDiv = 2, NDiv = 30$_H$, MDiv = 18$_H$).

    1 = PLL registers at addresses 60$_H$ - 62$_H$ must be programmed manually.

PDiv$_{2-0}$:
These bits set the post-divider factor P in the PLL, determining the clock frequency. PDiv should be set as shown in the description of the PLL1 register above, such that $2^{(6-PDiv)}$ = MDiv. This will double the clock, as required. See description of register 60$_H$ for more details.

Address 63$_H$: OUTPUT Control Register 2. Default value 00$_H$

The OUTPUT control register controls some of the output functions, as follows:

Bit	7	6	5	4	3	2	1	0
Mnemonic	x	x	x	x	x	ROutDis	GOutDis	BOutDis
Default value	x	x	x	x	x	0	0	0

x:
These bits are not used and do not exist physically.

R/CrOutDis:
G/YOutDis: } These bits are used to control the R/Cr, G/Y and B/Cb output busses, as follows:
B/CbOutDis:

    0 = Corresponding bus is Active

    1 = Corresponding bus is Disabled (set low). This can be used to reduce noise and power consumption when an output bus is not being used in YCb/Cr or Y/Cb/Cr modes.

Address 64$_H$: Clock Control Register 2. Default value 00$_H$

The MSB is a read-only bit and the other seven bits in the PLL2 register control the operation of the clock generation PLL, as shown below:

Bit	7	6	5	4	3	2	1	0
Mnemonic	Test	Test	InvYClk	Test	Test	Test	Test	Test
Default value	0	0	0	0	0	0	0	0

Test: These bits all put the FLI2200 into special test modes and should always be set low for normal operation.

InvYClk: This bit controls the phase of the internal 27 MHz sampling clock used in the IFormat = 11x modes, as follows:

> 0* = Sampling clock has same phase as PIXCLK, samples on falling edgesof PIXCLK
>
> 1 = Sampling clock is inverted relative to PIXCLK, samples on rising edges of PIXCLK
>
> It is recommended that this setting be used in the IFormat = 11x modes

Address 65$_H$: Test Register

This register is used purely for test purposes and should not be changed at any time for normal operation. The default value is 00$_H$ (for reference only).

Address 66$_H$: Input HSync Delay Control Register. Default value 00$_H$

The Input HSync Delay control register controls the input horizontal sync timing, as follows:

Bit	7	6	5	4	3	2	1	0
Mnemonic	x	x	x	IHSyncDel$_4$	IHSyncDel$_3$	IHSyncDel$_2$	IHSyncDel$_1$	IHSyncDel$_0$
Default value	x	x	x	0	0	0	0	0

x: These bits are not used and do not exist physically.

IHSyncDel$_{4-0}$: These bits set the input horizontal sync timing. The number is a signed, two's complement value. The adjustment is in 1 pixel increments relative to the default standard timing of this signal as shown in the timing diagrams, as follows:

ISyncDel$_{4-0}$	Timing relative to default value
10$_H$	–16 pixels
00$_H$*	Default timing
0F$_H$	+15 pixels

Address 67$_H$: Test. Default value 08$_H$

This register is used purely for test purposes and should not be changed at any time for normal operation. The default values is 08$_H$ (for reference only).

Address 71$_H$ and Address 72$_H$: Test Registers. Default values 00$_H$

These 2 registers are used purely for test purposes and should not be changed at any time for normal operation. The default values are all 00$_H$ (for reference only).

Address 7E and Address 7F$_H$: Chip Identification Registers. Default values: 7E$_H$ = 41$_H$, 7F$_H$ = 4B$_H$ (Read Only)

The eight bits in the IDL and IDH registers contain the 16-bit chip identification information. Register 7E$_H$ contains the lower byte and register 7F$_H$ contains the upper byte, so that the chip identification number is 4B41$_H$.

Control Bus Operation and Control Protocol

When the MODE pin (pin 46) is set low the FLI2200 operates as a slave device, responding to commands from a master controlling the bus. The protocol is generally I^2C compatible. Between operations the master sets the bus into the idle state, during which the master releases both the clock (SCL) and data (SDA) lines so that they both go high. All operations commence with a **S**TART (**S**) command from the master; this is indicated by the master setting the SDA line low while the clock is in the high state, as shown in Fig. 1. The clock then goes low and an operation begins. All write operations consist of 8-bit (byte) transfers either from or to the master, after which the receiving slave responds with an **A**cknowledge (**A**) by setting the SDA line low for one clock cycle. In the read operation process is similar but the receiver (the master in this case) omits the acknowledge after the data byte is read from the FLI2200. During the course of all operations the SDA line will only change while the SCL line is low, and should remain stable while SCL is high. The master indicates the end of an operation or set of operations with a STO**P** (**P**) command, indicated a rising edge on SDA while SCL is high. Sets of multiple operations can be executed by means of further **S**TART commands at the end of each operation with or without a STO**P**.

In all cases, the first byte is always the Slave Address byte, sent from the master to select the desired device. The settings of the $ADDR_{1-0}$ pins allow the device address of the FLI2200 to be programmed to prevent conflict with the other devices connected to the bus. The slave address can be set to any of the following values, as follows:

$ADDR_{1-0}$	Device Address
0 0	$C0/C1_H$
0 1	$C2/C3_H$
1 0	$E0/E1_H$
1 1	$E2/E3_H$

The seven MSBs of the Slave Address byte are the Slave Address itself and the LSB is the Read/Write bit. When the R/W bit is set low (write mode) it indicates that the master is going to transfer more bytes, as shown in Fig. 2. The minimum write operation consists of two more bytes, the Register Address (which selects the register to be written) followed by the Data Byte for that address. The FLI2200 will respond with an Acknowledge after each byte. The master follows these with a STO**P** command, terminating the operation. Multiple registers can also be written sequentially using the Auto Increment capability of the FLI2200. By sending further bytes of data before the STO**P** command, as shown in Fig. 3, the address is automatically incremented as each sequential byte is written. This is followed by a STO**P** bit, as before, to terminate the operation.

When the R/W bit is set high (read mode) it indicates that the master intends the Slave to respond with a data byte from the specified register address. The register address must first be set by writing a Register Address byte to the FLI2200 (with R/W set high) without an accompanying Data Byte. The FLI2200 then responds by sending the contents of that register, as shown in Fig. 4. The master should terminate the operation at this point by **N**ot (**N**) issuing an Acknowledge, followed by a STO**P** command. The FLI2200 only has one register containing a read-only bit, the PAL status bit, bit 7 in register 07_H. Consequently, multiple byte read with auto increment is not supported in the FLI2200.

In addition, although it is technically legal under I^2C protocol to abort a sequence after issuing a **S**TART followed by a device address, the FLI2200 will not release the bus unless it receives a STO**P** before another **S**TART is issued once it is addressed in this way.

When the MODE pin is set high the FLI2200 will self program from an I^2C compatible serial memory by reading 128 bytes of data after it is reset. The memory must first be pre-programmed with the necessary programming information.
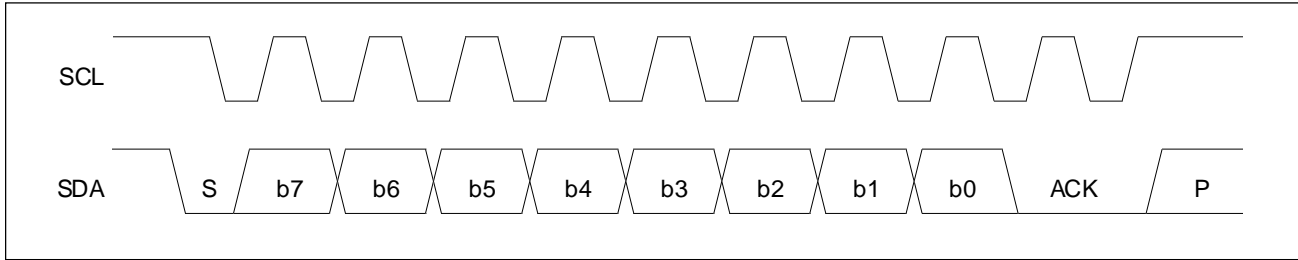
Control Bus Timing

Figure 1. Control Interface Timing
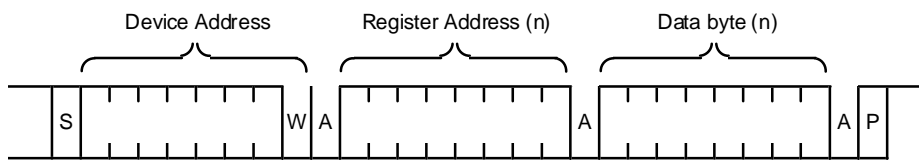
Control Bus Operation and Control Protocol
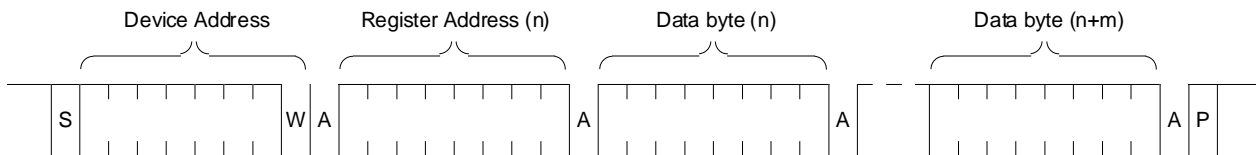

Figure 2. Write Mode: Single Byte Write

Figure 3. Write Mode: Multiple Byte Write Using Auto Incrementing

Figure 4. Read Mode: Single Byte Read

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ambient temperature under bias (T_A).. –40 to +85° C

Storage temperature (T_{ST}).. – 65 to +150° C

Voltage on V_{DD33} pins with respect to ground (V_{SS})... –0.5 to + V

Voltage on V_{DD25} pins with respect to ground (V_{SS})... –0.5 to + V

Voltage on any pin with respect to ground (V_{SS}).. –0.3 to +3.6 V

Input current on any pin during overload condition.. –10 to +10 mA

Absolute sum of all input currents during overload condition.. 100 mA

Power dissipation.. 1.75 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN} >V_{DD} or V_{IN} <V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

D.C. Characteristics

Unless otherwise noted, limits printed in **bold** characters are electrical testing limits at V_{DD33} =3.3 volts, V_{DD25} =2.5 volts and T_A = 25° C. All other limits are design goals for V_{DD33} = 3.3 volts ±5%, V_{DD25} = 2.5 volts ±5% and T_A = 0° to 70° C. This data sheet is preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact Faroudja Laboratories for the most current product information.

Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
Input low voltage	V_{IL}	–0.3		0.8	Volts	
Input high voltage	V_{IH}	2.0		V_{DD33} +0.3	Volts	
Output low voltage	V_{OL}			0.4	Volts	See note
Output high voltage	V_{OH}	0.85·V_{DD33}		V_{DD33}	Volts	See note
Input leakage current	I_L			±10	µA	$0 < V_{IN} < V_{DD}$
Pullup resistor value	R_{PU}	50		250	kΩ	$TEST_{2-0}$ only
Digital input pin capacitance	C_I			4	pF	f_{TEST} = 1 MHz
Digital output pin capacitance	C_O			8	pF	f_{TEST} = 1 MHz
Bidirectional pin capacitance	C_B			2	pF	f_{TEST} = 1 MHz
Power supply current	I_{DD33}		45		mA	V_{DD33} =3.3 volts
			50		mA	V_{DD33} =3.6 volts
						f_{CLKIN} = 13.5 MHz, RESET = V_{SS}
	I_{DD25}		350		mA	V_{DD25} =2.5 volts
			375		mA	V_{DD25} =2.65 volts
						f_{CLKIN} = 13.5 MHz, RESET = V_{SS}

Input Signal Timing
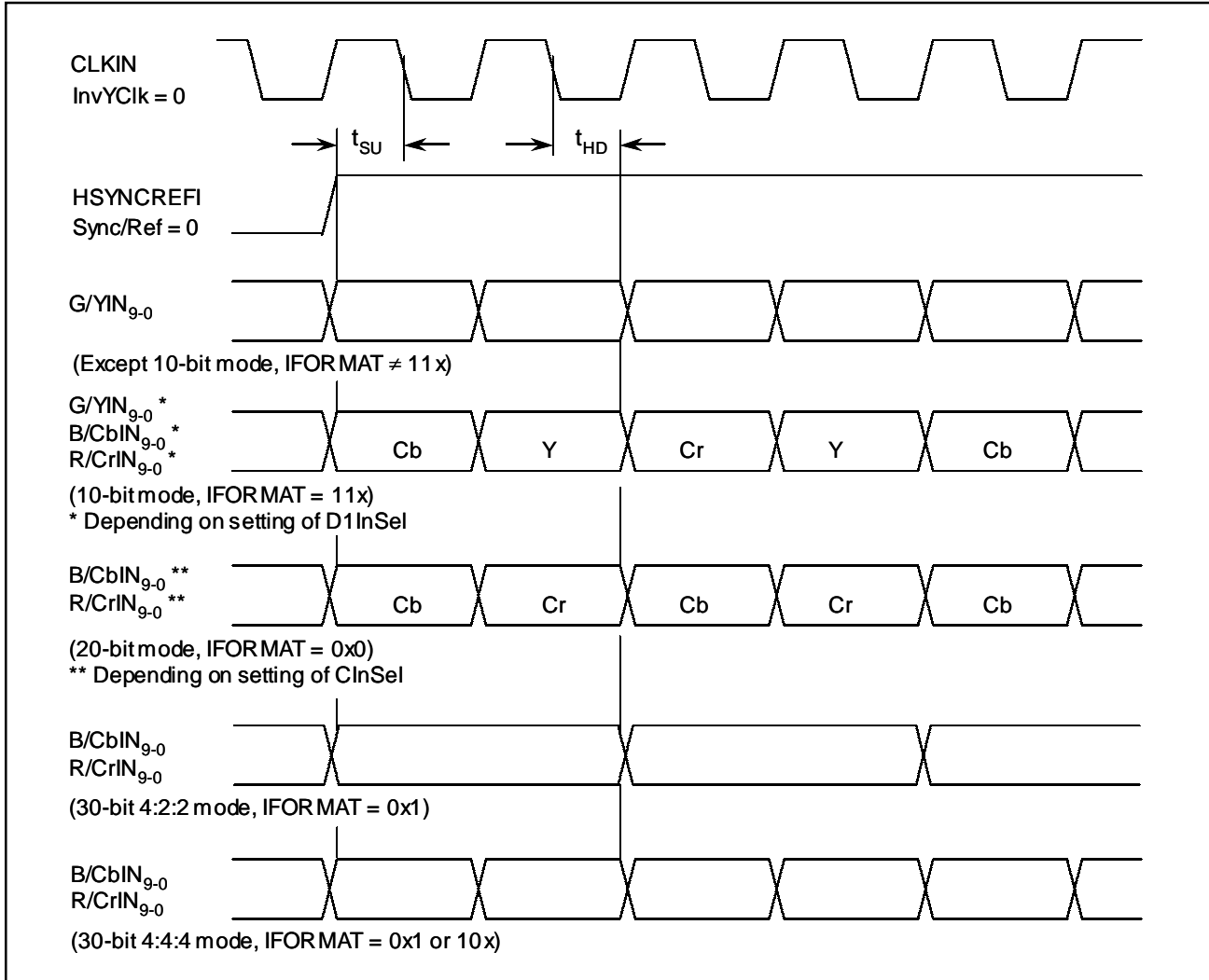
Input Signal Timing

Symbol	Description	Min.	Max.	Units	Conditions
f_{PIXCLK}	Input clock frequency		13.5	MHz	IFormat ≠ 11x, NOMEM = 0 **or** NMOvr = 1 NoMem = 0
			27	MHz	IFormat = 11x, NOMEM = 0 **or** NMOvr = 1 NoMem = 0
			37.5	MHz	IFormat ≠ 11x, NOMEM = 1 **or** NMOvr = 1 NoMem = 1
			75	MHz	IFormat = 11x, NOMEM = 1 **or** NMOvr = 1 NoMem = 1
t_{SU}	Input to clock setup	0		nsec.	
t_{HD}	Input to clock hold	0		nsec.	

Output Signal Timing
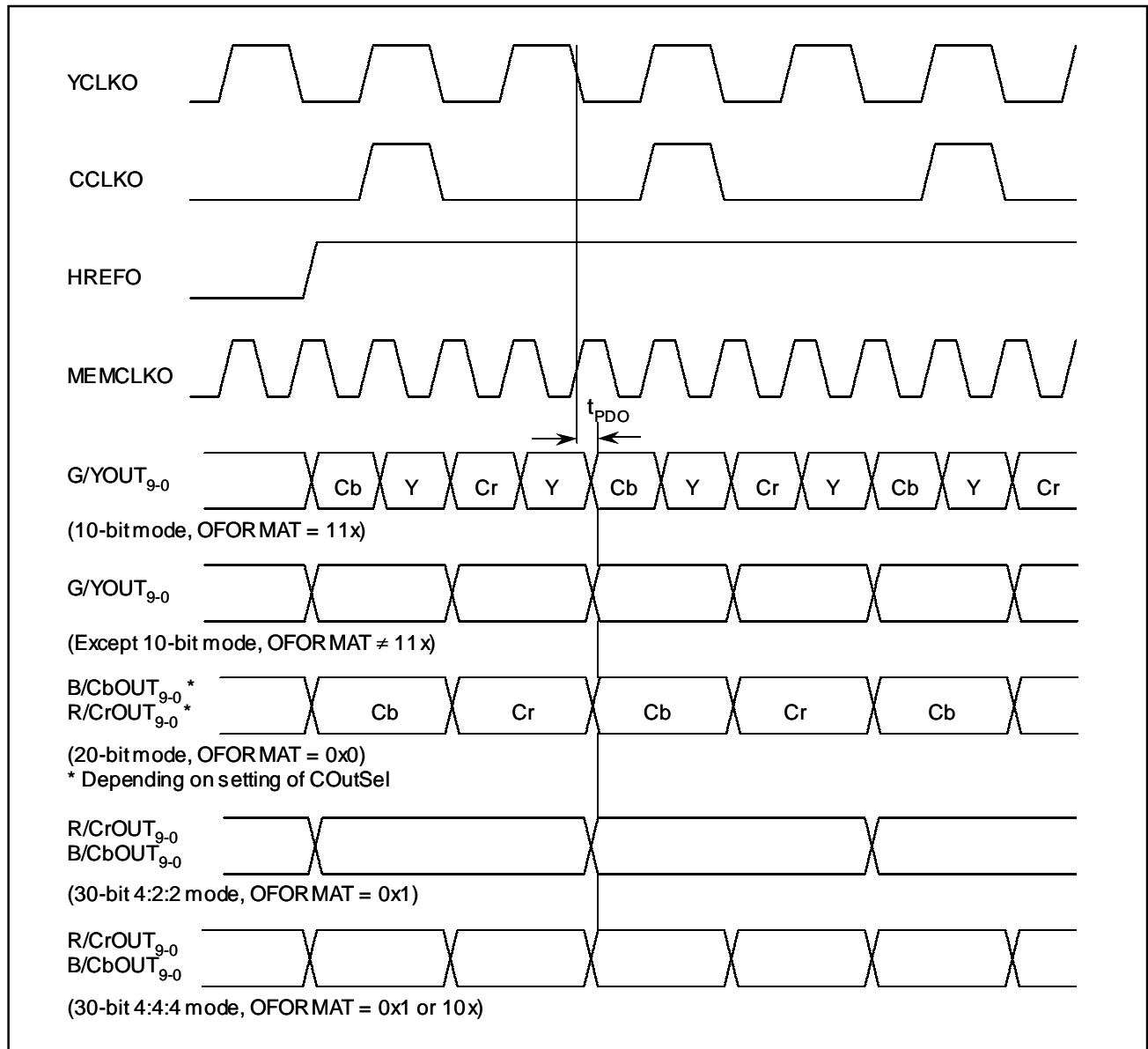
Output Signal Timing

Symbol	Description	Min.	Nom.	Max.	Units	Conditions
$f_{YCLKOUT}$	Output luma clock frequency			75	MHz	
t_{PDO}	Clock to output delay	–3		+3	nsec.	

Applications Information

Deinterlacing video signals: Optimal solutions for optimal images under different conditions

There are several different conditions that exist in video signals that require different approaches to deinterlacing. The first and most obvious is a moving image (or portion of an image) versus a still image (or portion of an image). It is fairly obvious that still images can be deinterlaced simply by interleaving the odd and even fields, i.e., forming a full frame of 525 (in the case of NTSC) lines by taking the 262.5 lines from the odd field 1, 3, 5, etc. and interleaving them with the 262.5 lines from the even field (2, 4, 6, etc.) to form a complete frame of 525 lines (1, 2, 3, 4, etc.) and displaying it at the field rate, i.e., 59.94 Hz. However, if anything in the image moves between the odd and even fields the results will be disastrous! An example is shown in Fig. A1, below, where the car is moving from left to right. If the car is moving at 60 mph it will have moved 1.5 feet between the frames.
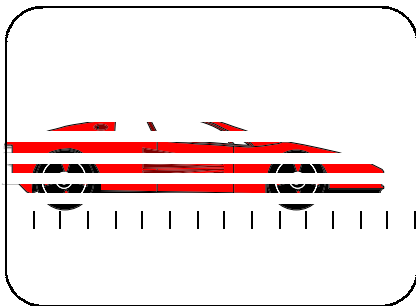
(a) Odd field: time = t
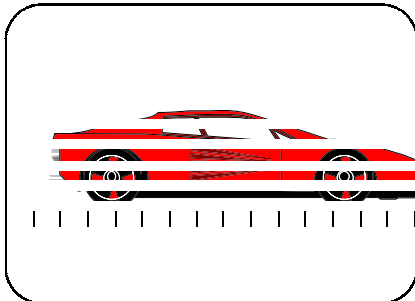
(a) Even field: time = t + $^1/_{60}$ sec.
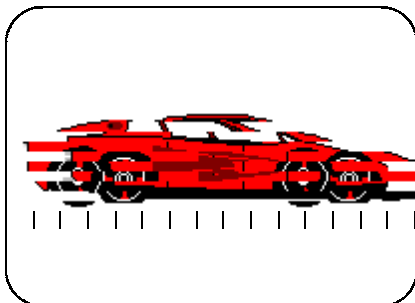
(c) Odd and even fields interleaved

Fig. A1. The result of interleaving fields containing motion.

The way to deal with a moving image is to deal with the fields independently and generate the missing lines in each field by interpolation. There are several way in which this can be done, the easiest being to assume that the image is always going to be in motion, and interpolate all the time. This, of course, results in an image which appears to very soft when (and where) there is no motion as a result of the fact that the true vertical resolution has been reduced, relative to the original image.

The second method is to use a motion detector of some kind to detect whether anything has moved from frame to frame and to use this to control the system: interpolate when motion is detected, interleave when no motion is detected. Although it is possible to implement a motion detector simply by computing a metric for each field and comparing it with that for the same field from the previous frame, this only allows the choice of interleave versus interpolate to be made on a field by field basis. In addition, unless a field memory (delay) is used, the metric for the current field cannot be computed until the field has already been displayed. This is an extremely undesirable condition since the motion/no motion condition on a per field basis changes continuously. Even when the field delay is used, this method is far from optimum because any motion anywhere in the image will cause the system to switch into interpolate mode, resulting in soft images in areas of the picture containing no motion, a very common condition.

A much better way is to compute a motion metric on a pixel by pixel basis, and this is the method used in the FLI2200. The motion detector is frame based and compares the luma value of the current pixel and the same pixel in the previous frame. This is done in both the odd and even fields to generate a motion vector which is then used to switch the signal processing between field interleave and interpolation modes on a pixel by pixel basis. In this way, non-moving parts of the picture, where sharpness is readily detected by the viewer, will not be interpolated and will have maximum sharpness. Conversely, moving parts of the picture, where sharpness is not easily detected by the viewer, will be interpolated to avoid motion artifacts.

The most common method of implementing the interpolation function is to use a 2-line memory and generate the interpolated pixels from the pixel above (previous line) and the pixel below (next line). This implementation can be improved by using more "previous" and "next" lines to implement a higher order interpolating filter, giving slightly sharper images. However, no matter how complex the interpolating filter is, it always operates on the basis that the current pixel is

related to the pixels above and below it, which is completely untrue of diagonal edges. Whenever an edge is not vertical, the current pixel is related to those diagonally above and below it in a relationship which depends on the angle of the edge, e.g., if the angle is 45°, the relationship is "one up and one across" and "one down and one across". With other angles becomes more complex and will involve non-integer relationships. Consequently, it is extremely difficult to implement such a "diagonal interpolation" algorithm, but this has been achieved in the FLI2200. This new algorithm (patent pending) computes and tracks the angles of edges and uses this information to optimally fill in the missing pixels. It greatly improves the quality of moving images, particularly those in fairly slow motion, such as the waving flag shown in Fig. A2 below, by eliminating the "jaggies" conventionally generated by interpolation.

Fig. A2. Conventional vertical interpolation on diagonal edges (L) versus diagonal interpolation (R)

Deinterlacing images which originated from progressive scan sources, including film

Whenever an interlaced image is generated from a progressively scanned image (where the original frame rate equals the field rate after interlacing) the resulting odd and even field pairs will originate from the same frame and, by definition, there will be no motion between them since the images occurred at the same point in time.

A special instance of this is the conversion of film to video in a teleciné machine. There are two types of teleciné machines. The first is the one used to convert 24 fps film to 60 field/sec. (30 fps) video, i.e., NTSC. Since it is not practical to run a 24 fps film at 30 fps the technique used is called "3:2 pulldown", in which each film frame is alternately mapped into three video fields and two video fields. The resulting ratio of two film frames to five video fields matches the rate of the film precisely to the 59.94 fields/sec. rate of the video when the film is run at 23.976 fps. The mapping sequence is shown in Fig. A3, below. Note that there are alternating consecutive pairs of odd fields and even fields originating from the same film frame. This makes it possible for a frame based motion detector to synchronize a state machine to this sequence (US patent 4,982,280) and match the odd and even fields originating from the same frame. In this way the video can be deinterlaced by interleaving these fields at all times, regardless of motion, resulting in the ultimate image quality.

The second type of teleciné is the "one film frame to one pair of video fields" type (sometimes referred to as "2:2 pulldown"). This type is primarily used to convert conventional 24 frame/sec. (fps) film to 50 field/sec. video, i.e., PAL. In this case the film is actually run at 25 fps. The 4% speed increase is not noticeable in the video, but those with the sense of "perfect pitch" can detect the raised pitch of the sound track. This type of teleciné is also used to convert 30 fps film to NTSC video. Although there are no pairs of the same field (odd or even) originating form the same film frame in the resulting video it is still possible to detect the sequence by using a field based motion detector and use this to match pairs of fields originating from the same film frame, allowing them to be interleaved, again resulting in the ultimate image quality.

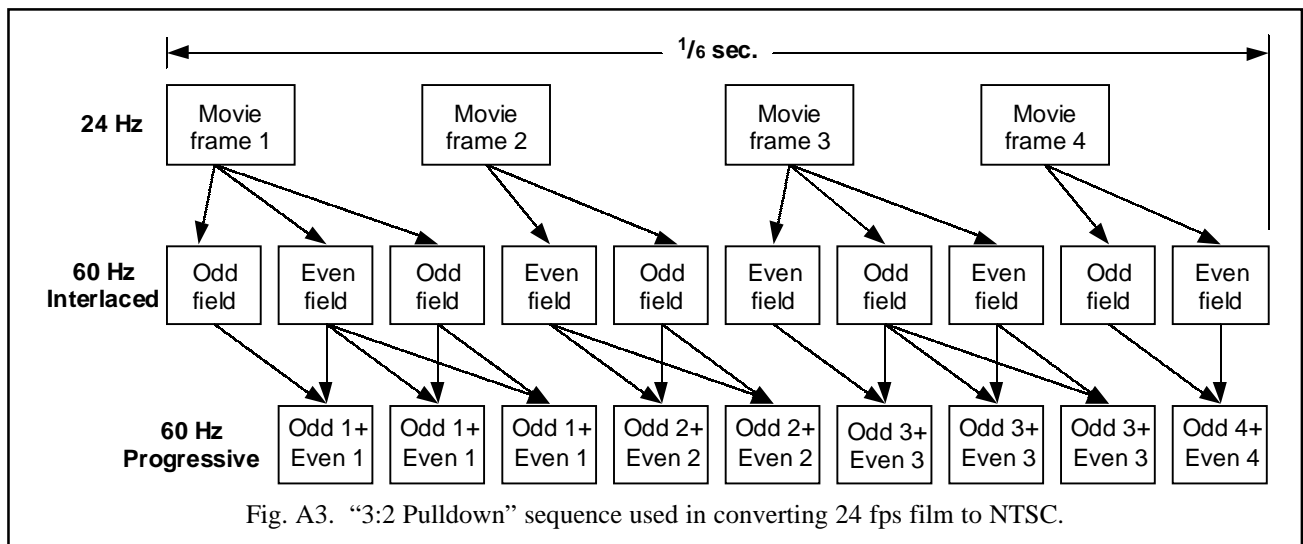| 24 Hz		Movie frame 1		Movie frame 2			Movie frame 3			Movie frame 4	
60 Hz Interlaced	Odd field	Even field	Odd field	Even field	Odd field	Even field	Odd field	Even field	Odd field	Even field	
60 Hz Progressive	Odd 1+ Even 1	Odd 1+ Even 1	Odd 1+ Even 1	Odd 2+ Even 2	Odd 2+ Even 2	Odd 3+ Even 3	Odd 3+ Even 3	Odd 3+ Even 3	Odd 4+ Even 4		

¹/₆ sec.

Fig. A3. "3:2 Pulldown" sequence used in converting 24 fps film to NTSC.

The video resulting from both types of teleciné machines has one problem: if the video is edited, it is possible for the sequence to be broken. In the 2:2 pulldown case there are four possibilities:

1. Good cut (at video frame start)

2. Bad cut (mid frame, between odd and even fields)

3. Good restart (at frame start)

4. Bad restart (mid frame)

Both the good cut/good restart and bad cut/bad restart combinations will result in the preservation of the sequence, although the bad cut/bad restart combination will result in a single bad frame (odd and even fields did not originate from the same film frame). Both the good cut/bad restart and bad cut/good restart combinations will break the sequence and result in bad video until the "film mode detect" state machine is resequenced, which typically takes up to 12 frames. Note that if the editor is frame based, only the good cut/good restart combination will occur.

The situation with 3:2 pulldown derived video is significantly worse. Even with a frame based editor there are 25 possible cases since the transfer sequence repeats over a period of five video frames, resulting in five possible cut points and five possible restart points. Only two of these will result in good edits, the other 23 resulting in the "film mode detect" state machine going out of sync and having to be resequenced. Thus it is virtually guaranteed that a video edit in NTSC will cause the system to lose sync, resulting in very bad deinterlacing artifacts until it is resequenced.

To minimize the consequences of bad edits, the FLI2200 incorporates a bad edit detector. This will detect even the single bad frame resulting from the bad/bad combination in PAL and, since it operates in a "look forward" mode, will cause the system to switch out of film mode before even a single bad field is displayed. The resulting lower quality video mode is preferable to the alternative, given the pixel by pixel motion handling and the high quality of the diagonal interpolation, even in the single bad frame case.

Interfacing the FLI2200 to video and MPEG decoders with ITU-R BT656 outputs
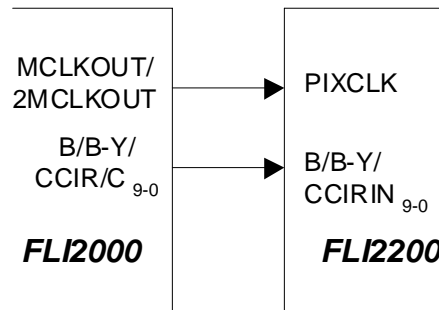

Fig. A4. Interfacing the FLI2200 to the FLI2000 NTSC/PAL decoder using the ITU-R BT656 (D1) format.

Interfacing the FLI2200 to an 8- or 10-bit parallel ITU-R BT656 (D1) signal source, suchas the FLI2000, is very simple since the FLI2200 can decode these signals. Since these signals include timing information in the horizontal and vertical banking intervals, no other syncs are required, so that the only interconnections required are the 10-bit data and the clock, as shown in Fig. A4. The input signal format can be controlled by means of the IFORMAT$_{2-0}$

pins (pins 56-58). The correct setting for the ITU-R BT656 input mode is 110. This setting can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the control bus if preferred. Please refer to the description of register 00_H for details. It is recommended that the interconnections be kept short since the operating speed in this mode is 27 MHz.

Input modes and busses

The FLI2200 has very flexible input and output controls that make it very easy to use in all applpications. The input formats and modes are summarized in the table below. For reference, the signals are as follows:

$IFORMAT_{2-0}$ pins are pins 56-58

$IFormat_{2-0}$ are bits 2-0 in register 00_H

IFmtOvr is bit 3 in register 00_H

CInSel is bit 6 in register 08_H

$D1InSel_{1-0}$ are bits 4-3 in register 08_H

| $IFORMAT_{2-0}$ | IFmtOvr | $IFormat_{2-0}$ | CInSel | $D1InSel_{1-0}$ | Input signals on busses | | | Clock rate/mode |
					G/YIN	B/CbIN	R/CrIN	
0 0 0	0	x	0	x	Y	Cb/Cr	x	(13.5 MHz, 4:2:2)
0 0 0	0	x	1	x	Y	x	Cb/Cr	(13.5 MHz, 4:2:2)
0 0 1	0	x	x	x	Y	Cb	Cr	(13.5/6.75 MHz, 4:2:2)
0 1 0	0	x	0	x	Y	Pb/Pr	x	(13.5 MHz, 4:2:2)
0 1 0	0	x	1	x	Y	x	Pb/Pr	(13.5 MHz, 4:2:2)
0 1 1	0	x	x	x	Y	Pb	Pr	(13.5/6.75 MHz, 4:2:2)
1 0 0	0	x	x	x	G	B	R	(13.5 MHz, 4:4:4)
1 0 1	0	x	x	x	G	B	R	(13.5 MHz, 4:4:4)
1 1 0	0	x	x	0 0	Y/Cb/Cr	x	x	(27 MHz, embedded timing)
1 1 0	0	x	x	0 1	Y/Cb/Cr	x	x	(27 MHz, embedded timing)
1 1 0	0	x	x	1 0	x	Y/Cb/Cr		(27 MHz, embedded timing)
1 1 0	0	x	x	1 1	x	x	Y/Cb/Cr	(27 MHz, embedded timing)
1 1 1	0	x	x	0 0	Y/Cb/Cr	x	x	(27 MHz, separate timing/syncs)
1 1 1	0	x	x	0 1	Y/Cb/Cr	x	x	(27 MHz, separate timing/syncs)
1 1 1	0	x	x	1 0	x	Y/Cb/Cr	x	(27 MHz, separate timing/syncs)
1 1 1	0	x	x	1 1	x	x	Y/Cb/Cr	(27 MHz, separate timing/syncs)
x	1	0 0 0	0	x	Y	Cb/Cr	x	(13.5 MHz, 4:2:2)
x	1	0 0 0	1	x	Y	x	Cb/Cr	(13.5 MHz, 4:2:2)
x	1	0 0 1	x	x	Y	Cb	Cr	(13.5/6.75 MHz, 4:2:2)
x	1	0 0 1	0	x	Y	Pb/Pr	x	(13.5 MHz, 4:2:2)
x	1	0 1 0	1	x	Y	x	Pb/Pr	(13.5 MHz, 4:2:2)
x	1	0 1 1	x	x	Y	Pb	Pr	(13.5/6.75 MHz, 4:2:2)
x	1	1 0 0	x	x	G	B	R	(13.5 MHz, 4:4:4)
x	1	1 0 1	x	x	G	B	R	(13.5 MHz, 4:4:4)
x	1	1 1 0	x	0 0	Y/Cb/Cr	x	x	(27 MHz, embedded timing)
x	1	1 1 0	x	0 1	Y/Cb/Cr	x	x	(27 MHz, embedded timing)
x	1	1 1 0	x	1 0	x	Y/Cb/Cr		(27 MHz, embedded timing)
x	1	1 1 0	x	1 1	x	x	Y/Cb/Cr	(27 MHz, embedded timing)
x	1	1 1 1	x	0 0	Y/Cb/Cr	x	x	(27 MHz, separate timing/syncs)
x	1	1 1 1	x	0 1	Y/Cb/Cr	x	x	(27 MHz, separate timing/syncs)
x	1	1 1 1	x	1 0	x	Y/Cb/Cr	x	(27 MHz, separate timing/syncs)
x	0	1 1 1	x	1 1	x	x	Y/Cb/Cr	(27 MHz, separate timing/syncs)

Output modes and busses

The FLI2200 has very flexible input and output controls that make it very easy to use in all applications. The output formats and modes are summarized in the table below. For reference, the signals are as follows:

OFORMAT$_{2-0}$ pins are pins 59-61

OFormat$_{2-0}$ are bits 2-0 in register 07_H

OFmtOvr is bit 3 in register 07_H

COutSel is bit 5 in register 08_H

| OFORMAT$_{2-0}$ | OFmtOvr | OFormat$_{2-0}$ | COutSel | Input signals on busses | | | Clock rate/mode |
				G/YOUT	B/CbOUT	R/CrOUT	
0 0 0	0	x	x	G	B	R	(27 MHz, 4:4:4)
0 0 1	0	x	x	Y	Cb	Cr	(27/13.5 MHz, 4:2:2)
0 1 0	0	x	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)
0 1 0	0	x	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)
0 1 1	0	x	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)
0 1 1	0	x	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)
1 0 0	0	x	x	Y	Pb	Pr	(27/13.5 MHz, 4:2:2)
1 0 1	0	x	0	Y	Pb/Pr	x	(27 MHz, 4:2:2)
1 0 1	0	x	1	Y	x	Pb/Pr	(27 MHz, 4:2:2)
1 1 0	0	x	x	Y	Cb	Cr	(27 MHz, 4:4:4)
1 1 1	0	x	x	x	x	x	Test mode only
x	1	0 0 0	x	G	B	R	(27 MHz, 4:4:4)
x	1	0 0 1	x	Y	Cb	Cr	(27/13.5 MHz, 4:2:2)
x	1	0 1 0	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)
x	1	0 1 0	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, separate timing/syncs)
x	1	0 1 1	0	Y	Cb/Cr	Y/Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)
x	1	0 1 1	1	Y	Y/Cb/Cr	Cb/Cr	(27/54 MHz, 4:2:2, embedded timing)
x	1	1 0 0	x	Y	Pb	Pr	(27/13.5 MHz, 4:2:2)
x	1	1 0 1	0	Y	Pb/Pr	x	(27 MHz, 4:2:2)
x	1	1 0 1	1	Y	x	Pb/Pr	(27 MHz, 4:2:2)
x	1	1 1 0	x	Y	Cb	Cr	(27 MHz, 4:4:4)
x	1	1 1 1	x	x	x	x	Test mode only

Package Dimensions
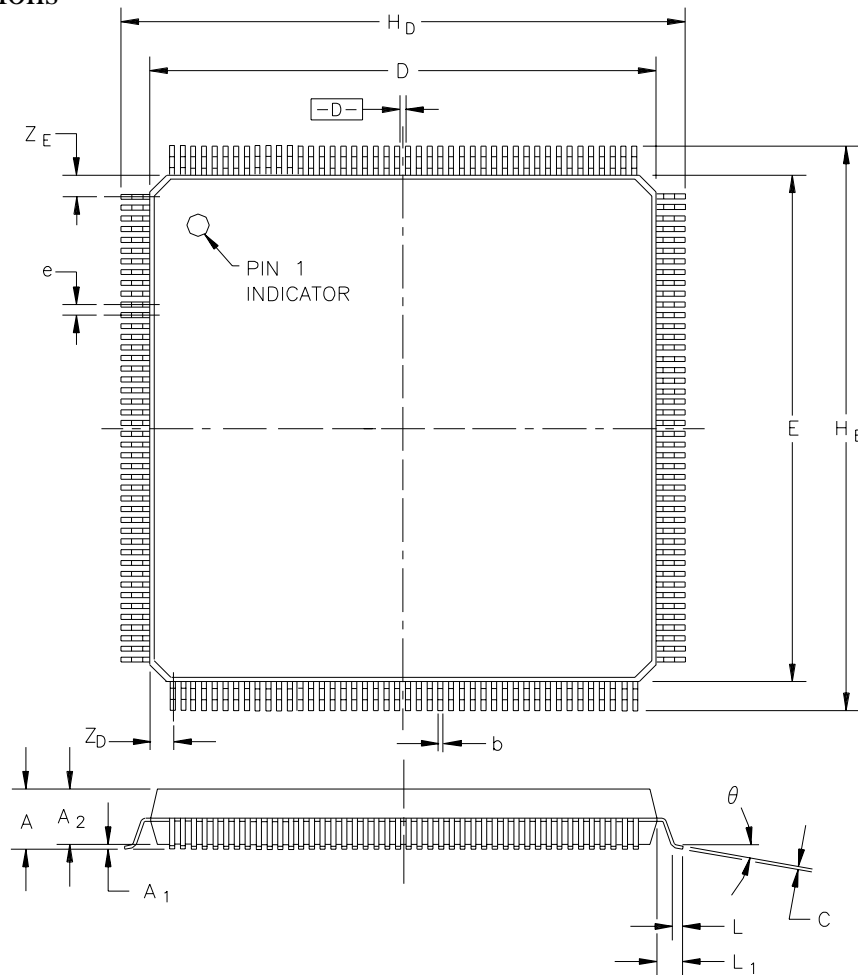
| | Millimeters | | | Inches | | |
Ref.	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.40		1.60	0.055		0.063
A1	0.05		0.15	0.002		0.006
A2	1.35		1.45	0.053		0.057
b	0.17		0.27	0.007		0.011
C	0.09		0.20	0.003		0.008
D		24.0			0.945	
E		24.0			0.945	
e		0.50			0.020	
H_D		26.0			1.024	
H_E		26.0			1.024	
L	0.45	0.60	0.75	0.018	0.024	0.029
L1		1.00			0.039	
Z_D		1.25			0.05	
Z_E		1.25			0.05	
θ	0°		7°	0°		7°

Note: Inch dimensions are derived from the original metric dimensions and may be approximate.

For more information, write or call:
Faroudja Laboratories, a Division of Sage, Inc.,
750 Palomar Avenue, Sunnyvale, CA 94086
Phone: (408) 735-1492 Fax: (408) 735-1571
http://www.faroudja.com