FM1185B
Low-Power Voice Processor
Datasheet v1.37
December 2007

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Revision History

Revision	Date	Comment
V1.0	12/28/05	Created
V1.1	1/26/06	1. Updated SNR Spec 2. Updated Package Dimension Spec
V1.2	1/27/06	1. Updated section 7.3.4 (Accessing UART Examples); 2. Updated section 6.5 (Serial Port)
V1.3	4/24/06	1. Updated Section 5 (Pin Description and Powerdown I/O Status) 2. Updated Section 7 (Functional Description) with new detailed description and diagrams 3. Added Serial Port Status to Section 6.5 4. Updated SHI max speed in Section 6.3 5. Added PGA Gain Information in Section 8.4 6. Added shipment method to Section 12 (Ordering Information)
V1.33	5/7/2007	1. Update all 1185 to 1185B per PCN CY06-004A
V1.34	5/15/2007	1. Add marking
V1.35	5/30/2007	1. Add marking description
V1.36	11/20/2007	1. Remove digital rise and fall time 2. Update power on/off sequence figure
V1.37	2/27/2008	1. Change crystal circuitry information

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1. Introduction

The FM1185B voice processor from Fortemedia is the ultimate high-performance, low-power single chip solution for echo cancellation and noise suppression. Providing SAM (small array microphone) technology with beam-forming capability at only 35mW of power consumption, FM1185B is ideal for any portable application with stringent requirements for battery life and power consumption. Offered in a small 5x5mm BGA package, FM1185B is ideally suited for applications including portable handhelds such as 3G phones, PDAs, smart phones, notebook computers & Tablet PCs, and VoIP phones.

To achieve the lowest power consumption, FM1185B features an integrated hardware accelerator to speed up voice related applications. This new device is designed to achieve the lowest power while providing the highest performance. With an enhanced CODEC, FM1185B provides high SNR for the best voice quality. FM1185B provides excellent noise suppression and full duplex capabilities, including non-linear echo cancellation and side tone cancellation.
For more details on Fortemedia technology, please refer to the *Fortemedia Technology White Paper*.

2. Key Features

- Highly integrated single chip solution
  - 16-bit DSP w/ Hardware Accelerator (Up to 40 MIPs)
  - 3 ADC (Analog to Digital Converter)
  - 2 DAC (Digital to Analog Converter)
  - RAM, ROM
  - On-chip microphone amplifier
  - SHI, UART interface to external controller
  - Serial port interface supports 16-bit & 13-bit PCM format
- Extreme low power consumption (35mW)
- High performance
  - Powerful AEC (acoustic echo cancellation) (60dB)
  - Superior full-duplex
  - Supports 1 & 2 microphone modes
  - Run-time microphone select mode
    - Select Mic0 or Mic1 as the main microphone (when using small array microphone with beam-forming)
  - Differential I/O to reduce RF interference and increase noise immunity
  - Dynamic range control (DRC) to increase voice intelligibility
  - Side tone cancellation of 25 to 35dB
  - Acoustic echo tail length coverage: 64 to 100ms
  - Mic_in, Line_in, Line_out, & Spk_out PGA (programmable gain amplification)
- Supports 2 clock inputs: 4.096MHz or 13MHz
- Available in 48-pin BGA package

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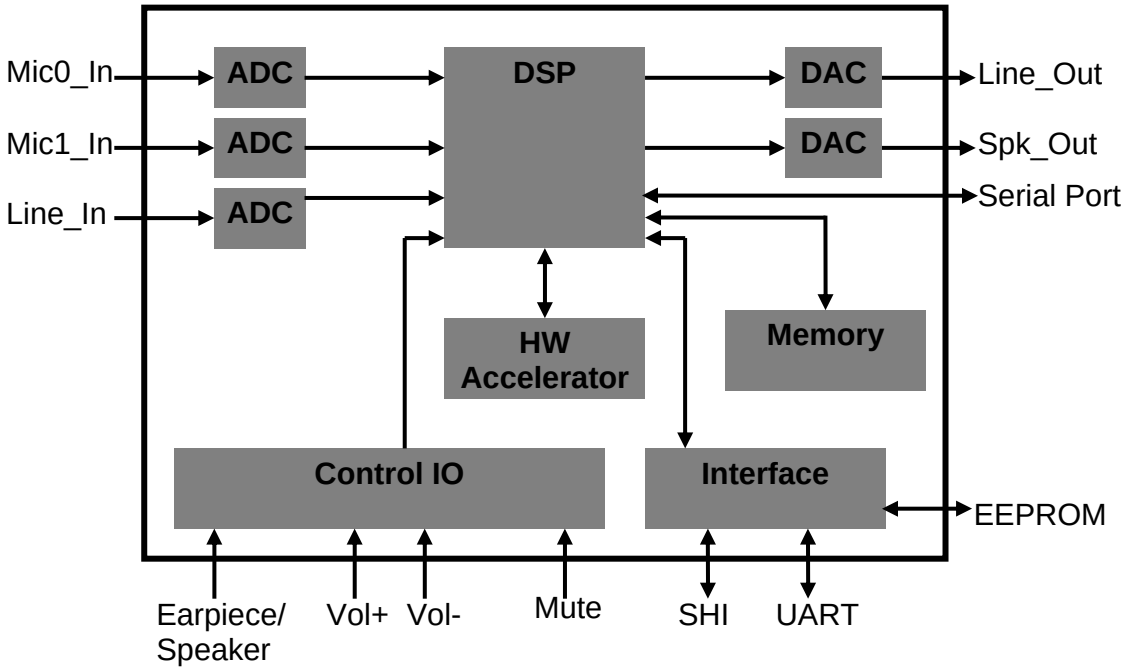
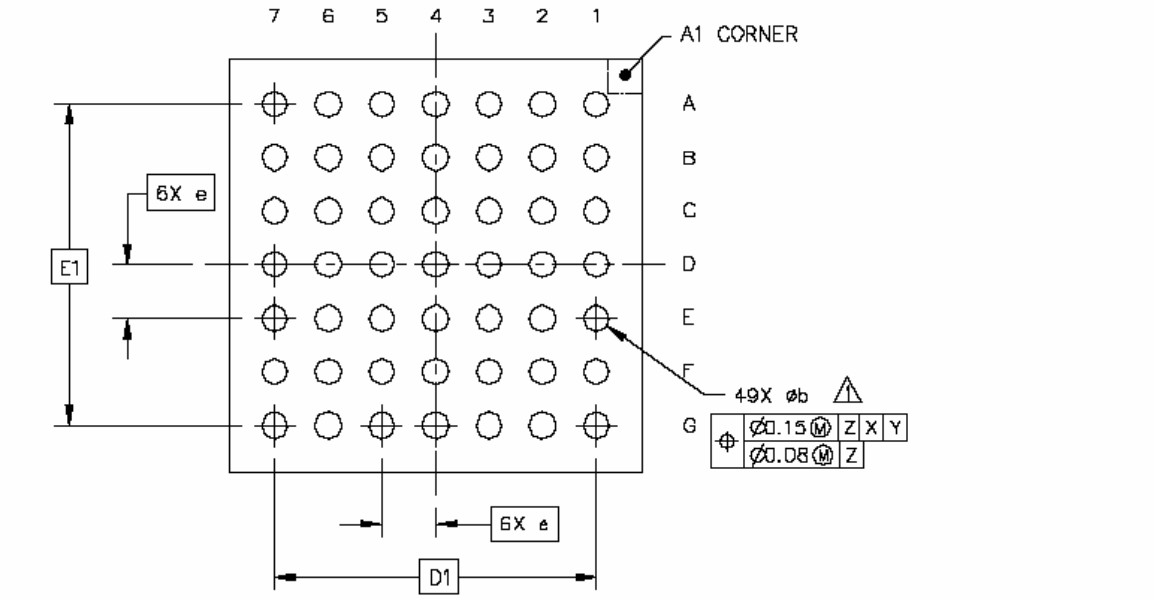
3. IC Block Diagram

Figure 1. FM1185B Block Diagram



4. Pin Configuration

Figure 2. FM1185B BGA Pin Configuration (Bottom View)



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5. Pin Description

Table 1. FM1185B Pin Description

Pin #	BGA Ball #	Pin Name	I/O Type	PD Status[5]	Pin Description
1	E3	NC	NC	NC	No connect
2	G2	NC	NC	NC	No connect
3	G1	SPK_OUT_N	Out	Tri-State	Speaker output (-)
4	F3	NC	NC	NC	No connect
5	G3	NC	NC	NC	No connect
6	F4	NC	NC	NC	No connect
7	E4	VSS_D	GND	GND	Digital ground
8	G4	BCLK	In/Out	In	BCLK signal for Serial Port
9	G5	FSYNC	In/Out	In	Frame sync signal for Serial Port
10	F5	PCM_OUT	In/Out	In	During power up, used as strap option (section 7.2); after power up, transmits voice data to Serial Port
11	G6	PCM_IN	In	In	Receive voice data from Serial Port
12	G7	UART_RX	In	In	Serial commands from UART port
13	F6	UART_TX	In/Out	In	During power up, used as strap option (section 7.2); after power up, transmits serial commands to UART port
14	E5	ANA_COM	In	In	For analog communications mode, which will bypass DSP [1]
15	F7	SDA_EE	In/Out	In	Serial data access for EEPROM
16	E6	SCL _EE	In/Out	In	Serial clock for EEPROM
17	E7	GPIO7	In/Out	In	Mode select strap option (section 7.2)
18	D4	VSS_D	GND	GND	Digital ground
19	D7	VDD_D	VDD	VDD	Digital power [2]
20	D6	STRAP0	In/Out	In	During power up, used as strap option (section 2); not used during normal operation
21	C7	MUTE_OUT	In/Out	In	During power up, used as strap option (section 2); after power up, serves as output LED to indicate microphone

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					"mute" status
22	D5	VAD_LED	In/Out	In	Must pull low using weak 100K resistor to select XTAL_IN as PLL clock source; after power up, serves as LED output to indicate internal status for VAD (Voice Activity Detection) tuning
23	B7	SCL	In/Out	In	Serial clock for SHI interface, if selected; if SHI is not selected, serves as input pin to select "earpiece" mode where the speaker output gain will be reduced to support earpiece function [(3)] ; if not used, pull high using weak 100K resistor to be in speaker-phone mode
24	C6	SDA/MUTE_IN	In/Out	In	Serial data access for SHI interface, if selected; if SHI is not selected, serves as input pin to select "mute" function on the microphone [(4)] ; if not used, pull low using weak 100K resistor
25	A7	Vol-	In/Out	In	Volume Down input pin (level triggered, active high); if not used, pull low using weak 100K resistor
26	B6	Vol+	In/Out	In	Volume Up input pin (level triggered, active high); if not used, pull low using weak 100K resistor
27	A6	XTAL_IN	In	In	Crystal input
28	A5	XTAL_OUT	Out	Out	Crystal output
29	C5	GND_D	GND	GND	Digital ground
30	B5	PWD_	In	In	Powerdown pin, active low
31	A4	RST_	In	In	Reset pin, active low
32	C4	TEST1	In	In	Connect a 100K ohm resistor to ground
33	A3	V10	VDD	VDD	connect a 1uF capacitor to ground and connect a ferrite bead to VDD_S

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34	B4	NC	NC	NC	No Connect
35	A2	VDD_S	VDD	VDD	Power supply
36	B3	NC	NC	NC	No Connect
37	A1	VREF	VDD	Tri-state	connect a 1uF capacitor to ground
38	C3	VSS_A	GND	GND	Analog Ground for CODEC
39	B1	MIC0_P	In	In	Mic0 (+) input
40	B2	MIC0_N	In	In	Mic0 (-) input
41	C1	MIC1_P	In	In	Mic1 (+) input
42	C2	MIC1_N	In	In	Mic1 (-) input
43	D1	LINE_IN_P	In	In	Line_in (+) input
44	D2	LINE_IN_N	In	In	Line_in (-) input
45	E1	VSS_REF	GND	GND	Connect to ground
46	E2	BG_REF	In/Out	Tri-state	Connect a 1uF capacitor to ground
47	F1	LINE_OUT	Out	Tri-state	Analog output
48	F2	SPK_OUT_P	Out	Tri-state	Speaker output (+)
n/a	D3	NC	NC	NC	No Connect

Notes:

(1) active high; when "high," DSP will be in idle state; DSP will restart on high to low transition

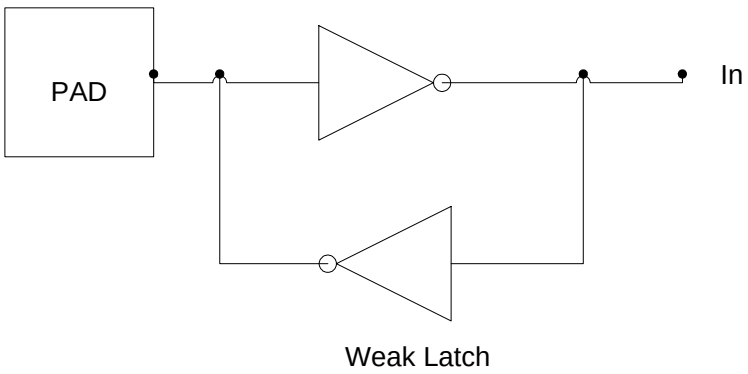
(2) this separate voltage source is designed to adapt to the level of the digital interface voltage level; it can either be 1.8V or 3.3V, depending on the interface logic level

(3) edge triggered, with falling edge to "earpiece" and rising edge to "speaker" mode

(4) level triggered with active high, and it will toggle between "mute" and "not mute"; the default after reset is always "not mute"

(5) PD status = powerdown status

Figure 3. PAD_IN Symbol for Digital Input Pins



Note: The pin status of the pins on power-up will depend on the external pull up or pull down connection. If there is no external connection, pin status on power-up is unknown.

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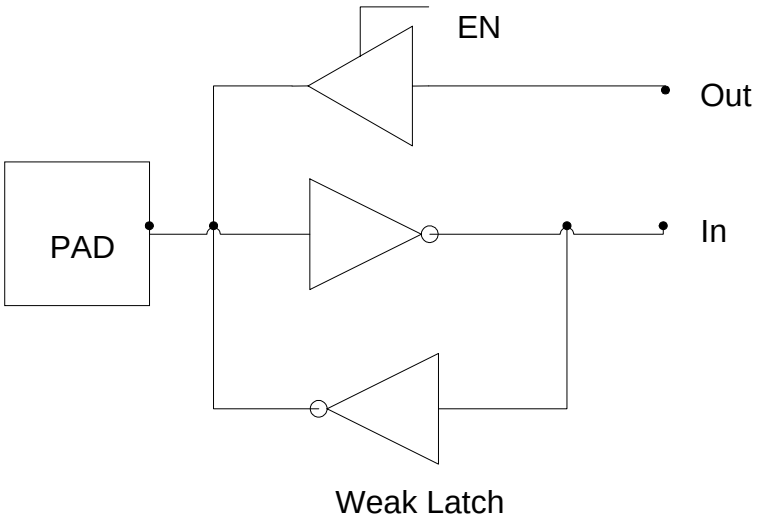
Figure 4. PAD_BI Symbol for Digital Input/Output Pins



Note: The pin status of the pins on power-up will depend on the external pull up or pull down connection. If there is no external connection, pin status on power-up is unknown.

6. Major Blocks Description

6.1 Serial EEPROM Interface (Pins 15, 16)

FM1185B supports a serial interface to an optional external EEPROM. It supports 256 bytes (small sized) and 1Kbytes (large sized) EEPROM. Most of the internal variables can be accessed through this EEPROM interface. See section 7.4 for more details.

6.2 UART Interface (Pins 12, 13)

FM1185B has one UART port, which is used to transmit and receive control commands. Each transfer will have one command byte, one or two address bytes, and up to two data bytes. UART needs a sync word “FCF3” to sync up each transfer. See section 7.4 for more details.

The UART port is recommended as the standard interface to access FM1185B.

Figure 5. UART Interface: 8-bit/character, 1 stop-bit protocol

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8-bit/character 1 stop-bit protocol

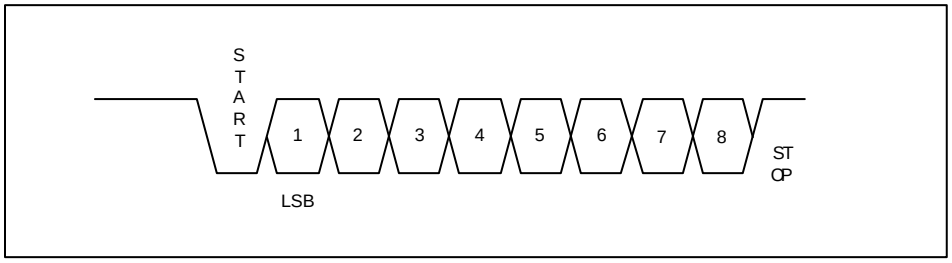

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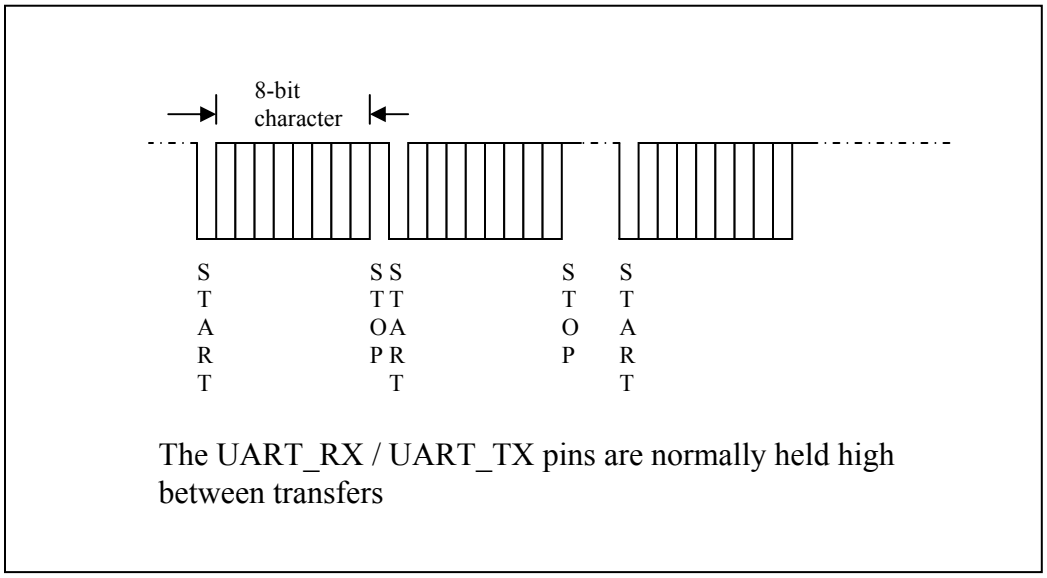
Figure 6. UART Transfers (TX & RX)



6.3 SHI (Serial Host Interface) (Pins 23, 24)

The SHI block is the interface to an external micro-controller, which can initialize FM1185B through this interface. SHI supports slave mode with 8 bit address mode. The maximum clock speed that the SHI interface can support is 100 KHz. Each transfer will have one command byte, one or two address bytes, and up to two data bytes. SHI needs a sync word "FCF3" to sync up each transfer. Please note that SHI is used for transferring parameters during power-up, and is off after the DSP is in normal operation mode. Refer to section 7.4 and *AN: FM1185 SHI Implementation* for more details.

Figure 7. SHI Start, Restart, & Stop

S: start, Sr: restart, P: stop, Ack: acknowledge

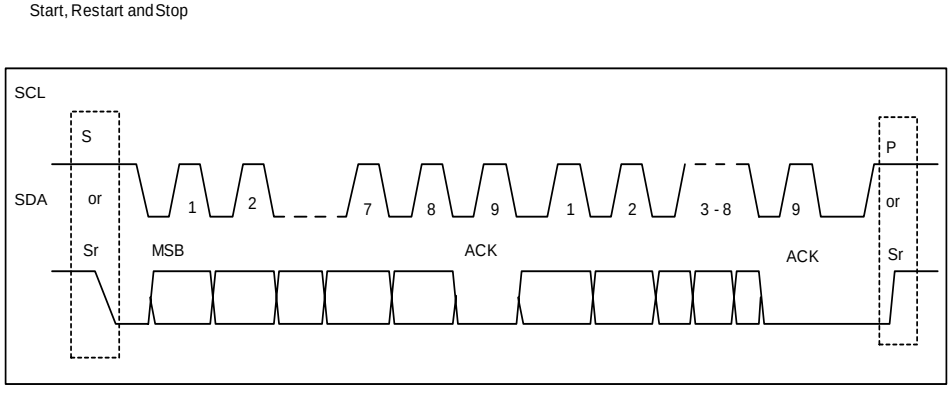


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Figure 8. SHI Burst write (on SDA)

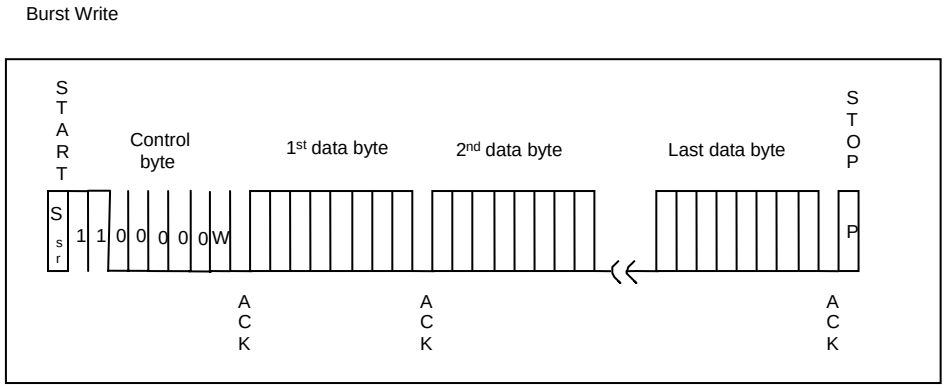
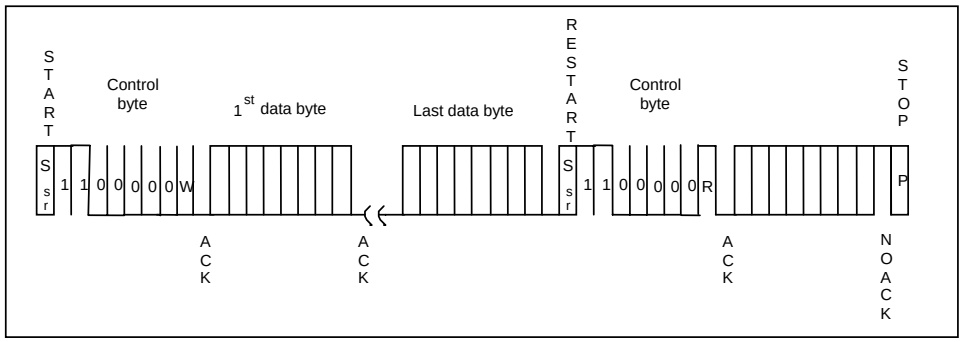


Figure 9. SHI Read (on SDA)



6.5 Serial Port (Pins 8, 9, 10, 11)

The serial port provides an interface to an existing host (micro-controller) for digital voice data transfer. Both the master and the slave modes support either an internal or external clock source for the BCLK signal. While operating with the internal clock, “FSYNC” runs at 8KHz.

The serial port data format can be 16-bit or 13-bit linear pulse code modulation (linear PCM). The default setting is to run 16-bit linear PCM mode. The format can be selected by EEPROM or an external controller.

In slave mode, FM1185B supports both short (one clock delay) and long (zero clock delay) “FSYNC”. In master mode, FM1185B drives short “FSYNC”. Table 2 below shows the status of the serial port output pins during different modes.

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Table 2. Status of Serial Port Output Pins

	Master Mode			Slave Mode		
	Power-down	**Serial Port Enabled (1)**	**Analog Mode (2)**	**Power-down**	**Serial Port Enabled (1)**	**Analog Mode (2)**
BCLK	Tri-state	Normal	"0"	n/a	n/a	"0"
FSYNC	Tri-state	Normal	"0"	n/a	n/a	"0"
PCM_OUT	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state

Notes:

(1) CHI_EN (bit2 of 0x3fe1) set to "0" (Refer to FM1185 Parameter Tuning Guide)

(2) ANA_COM asserted during reset; otherwise, asserting ANA_COM will turn off all digital clocks and leave states unknown

Figure 10. Serial Port: One clock delay

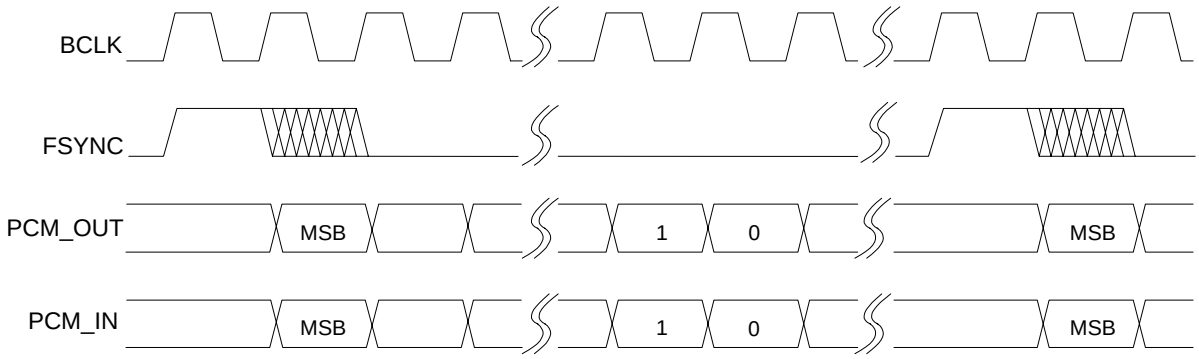
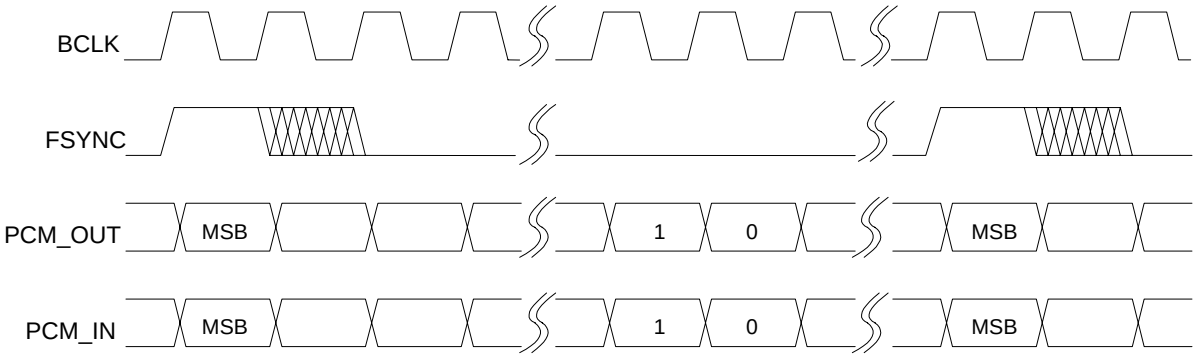


Figure 11. Serial Port: Zero clock delay



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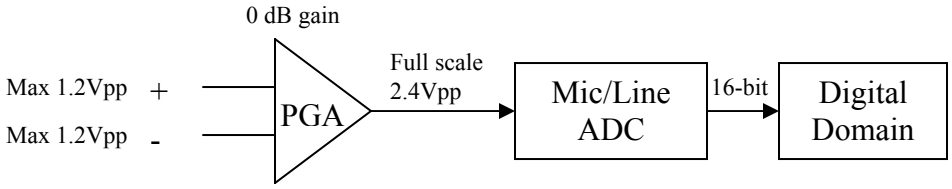
6.6 ADC (Pins 39, 40, 41, 42, 43, 44)

FM1185B includes 3 analog-to-digital converters (ADC). The converters are at 16-bit precision and 8k sampling rate with sigma-delta architecture. All 3 converters are differential; they are used for 2 microphone inputs with built-in microphone pre-amplifier and 1 line level input. The full scale of the input is 2.4Vpp. See Figure 12 for details.

For more information on how to program the attenuation/gains for the ADC and DAC blocks (6.7), please refer to the *FM1185 Parameter Tuning Guide*.

Figure 12. FM1185B ADC Details

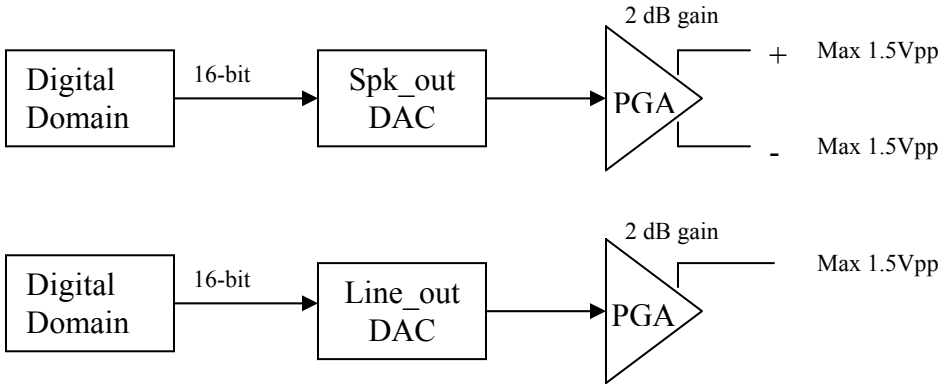


6.7 DAC (Pins 3, 47, 48)

FM1185B includes two digital-to-analog converters (DAC). The converters are at 16-bit precision and 8k sampling rate with sigma-delta architecture. One of the converters (differential) is used to feed into an external power amplifier to drive the speaker (Spk_out). The other converter (single-ended) provides programmable attenuations/gains that can be connected to a PC's analog input (Line_out). See Figure 13 for more details.

For more information on how to program the attenuation/gains for the ADC (6.6) and DAC blocks, please refer to the *FM1185 Parameter Tuning Guide*.

Figure 13. FM1185B DAC Details



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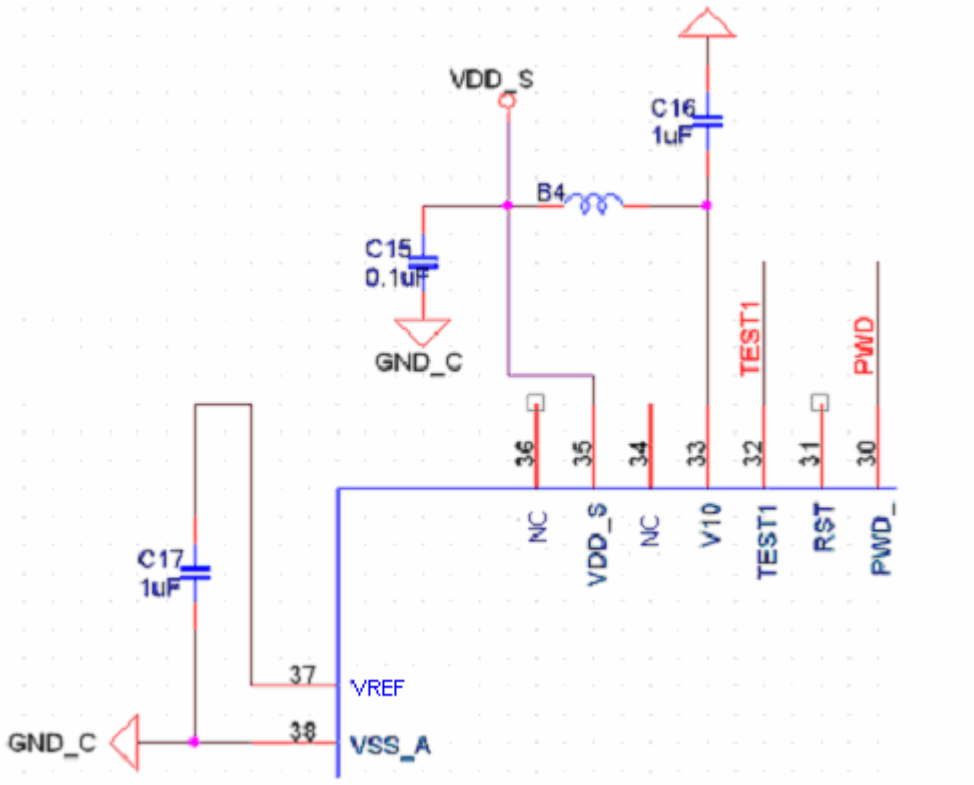
6.8 FM1185B Power Circuitry

FM1185B requires an external voltage supply of 1.8V for VDD_S. Please see Figure 14 below for suggested circuitry.

Figure 14. Suggested Power Circuitry for FM1185B



7. System Functional Description

7.1 Modes of Operation

At any moment, the FM1185B chip may operate in one of the following 4 modes:

Hardware Reset Mode

Whenever power is applied, the chip will enter this mode and remain until 10ms after the RST_ pin is pulled high. In this mode, the chip samples the strap-options (section 7.2), adjusts the clock source, and waits for the external clock (XTAL_IN or BCLK) and internal PLL to become stable. After the 10ms, the chip enters the Software Reset Mode. The chip re-enters the Hardware Reset Mode whenever the RST_ pin is pulled low externally.

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Software Reset Mode

In this mode, the embedded DSP software reads the strap-options (section 7.2), determines where the parameters will be coming from, and then either waits passively for the download from an external host (UART, SHI) or actively reads the parameters from an external EEPROM. The chip exits this mode when parameter at 1E3A becomes 0 (handled by embedded DSP when parameter configuration is done). Except when RST_ is pulled low, the chip moves to the Operational Mode after the Software Reset Mode.

Operational Mode

In this mode, software will set up hardware MMREGs according to the parameter configuration, followed by a nominal 70 msec for initialization. This is the mode where the chip samples its input and delivers its outputs through the analog/digital interfaces. After that, the chip may enter the Power Down Mode if the PWD_ pin is pulled low.

Power Down Mode

The chip enters the Power Down Mode 10ms after the PWD_ pin is pulled low. During the Power Down Mode, because the on-chip PLL is turned off, the PLL source clock can be also be turned off. After the Power Down Mode, the chip may move to either the Software Reset Mode or the Operational Mode (depending on the setting of the pwrdwn_set parameter, 1E51). In order for the chip to exit the Power Down Mode correctly, the external PLL source clock must resume 10ms before PWD_ is pulled high. After that, the chip will need another 13ms for house-cleaning work before it can take the new round of parameter download, or resume to the Operational Mode.

The following figures show the state transition diagram and the timing chart when the FM1185B chip moves between these 4 states.

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Figure 15. State Transition Diagram

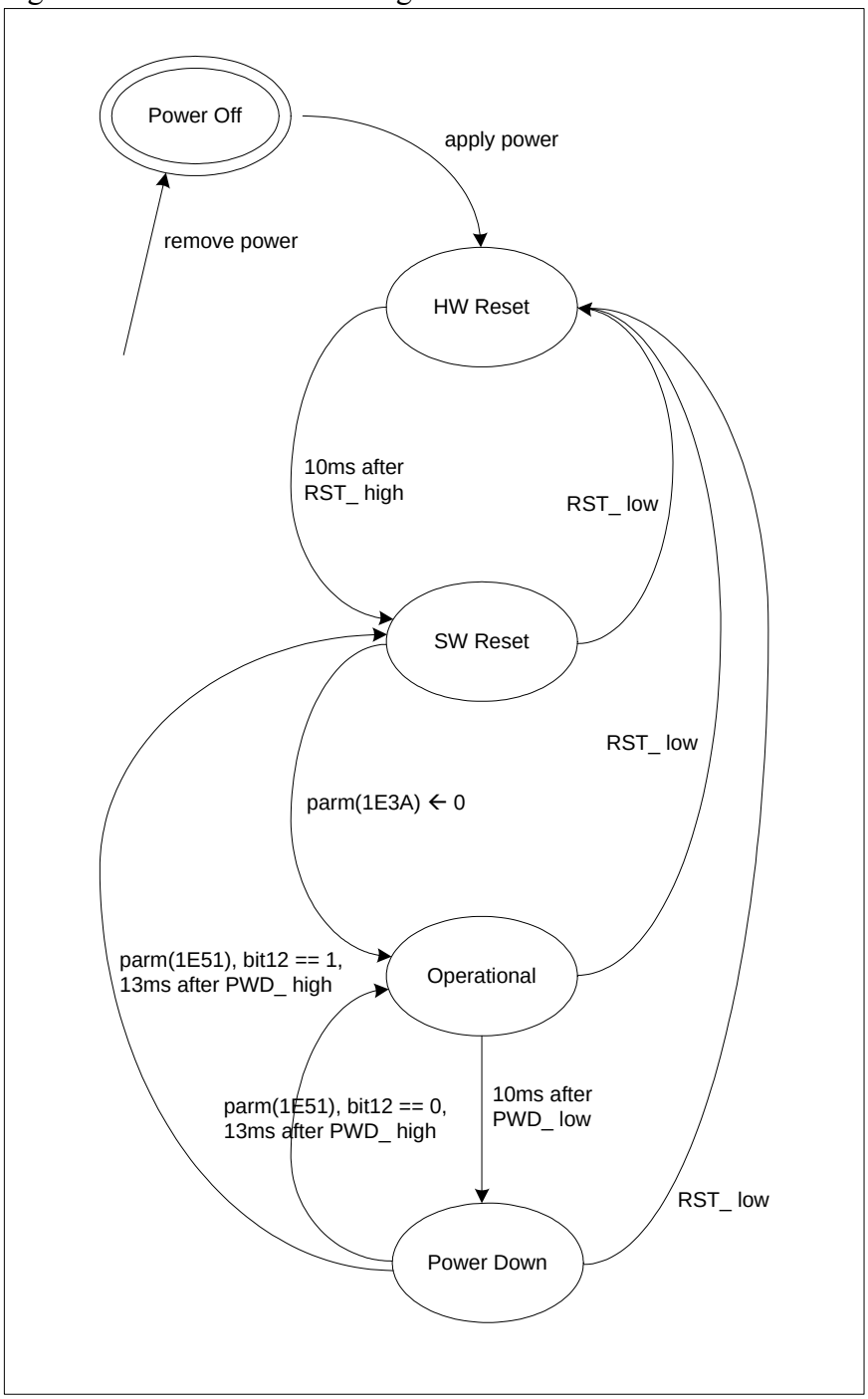

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Figure 16. Timing Chart of State Transitions

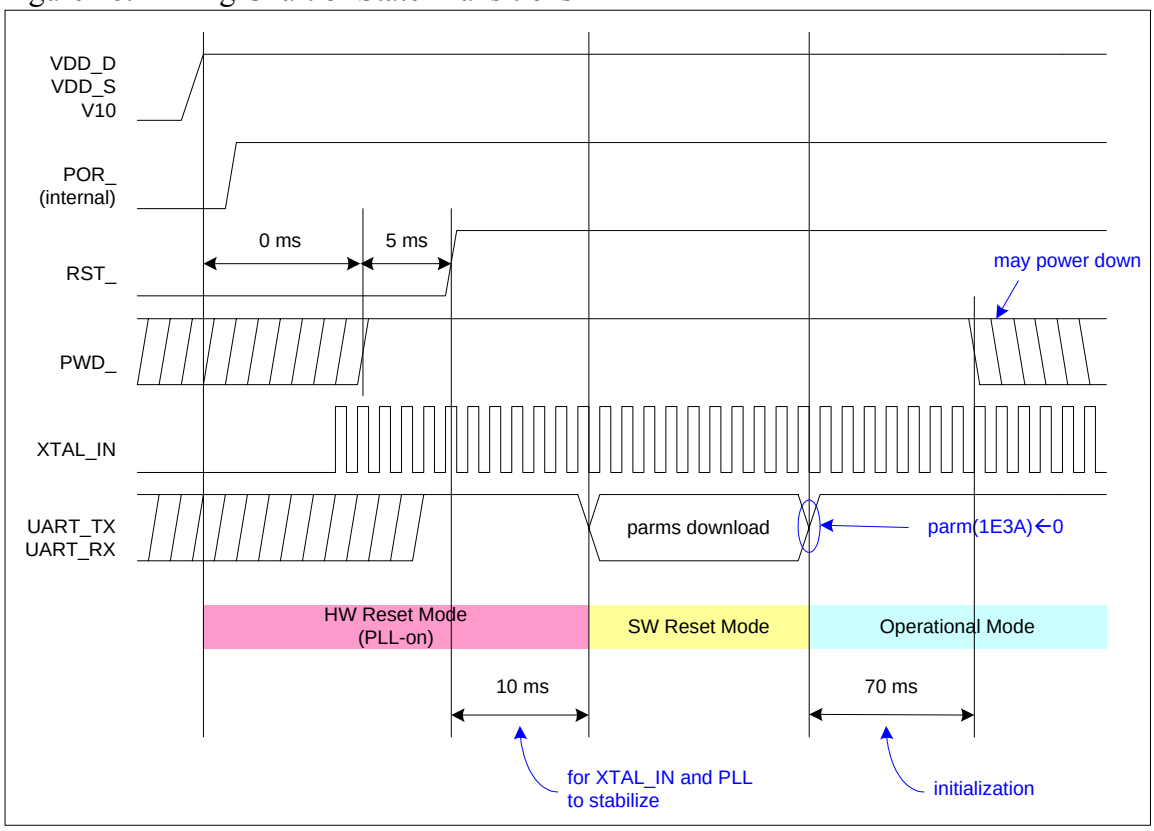

Figure 17. Timing Chart of Power Down Transition

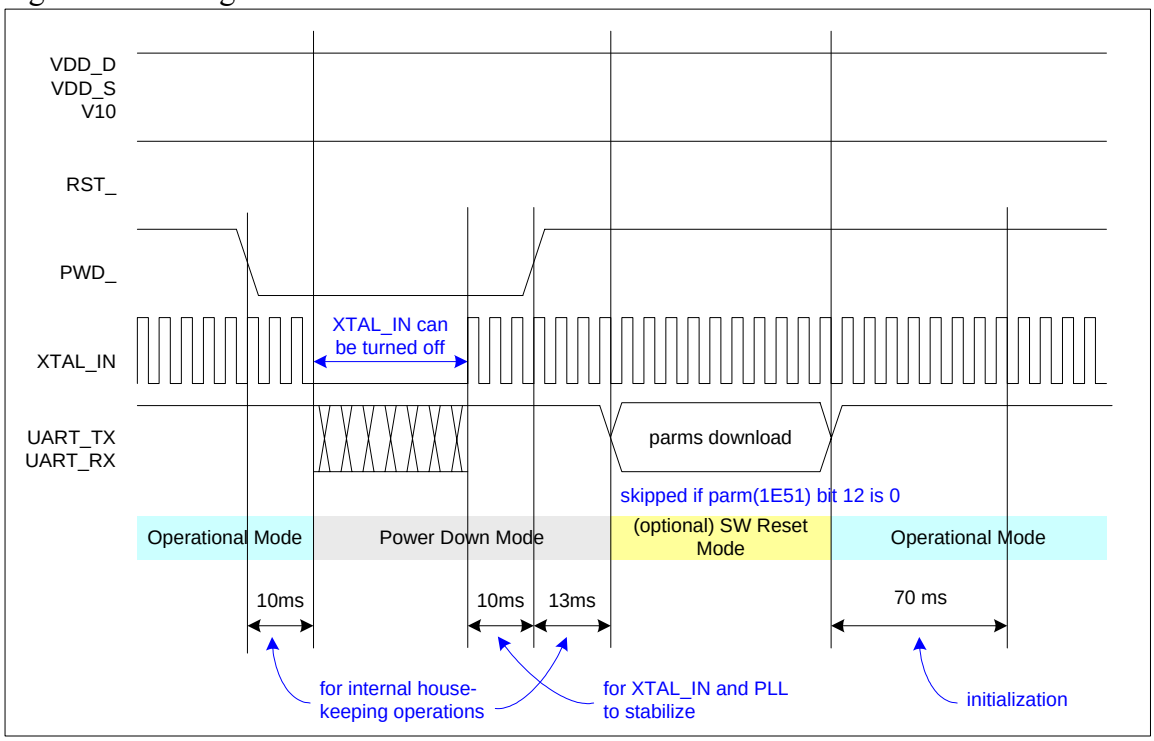

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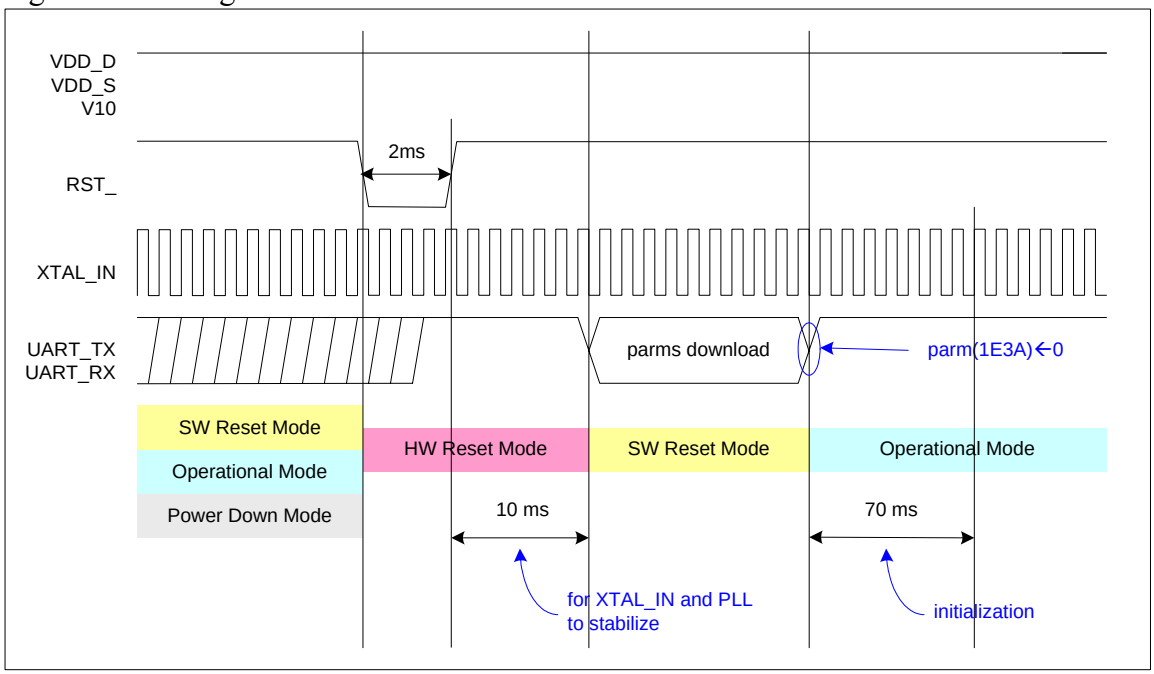
Figure 18. Timing Chart of External Reset



7.2 Power-Up Option Pins (Strap Options)

Strap options are used by the chip to determine the desired operation of the chip. All the strap options mentioned below must be pulled high or low using a weak 100k resistor. If left floating, the status will be unknown.

In the software reset mode, the chip samples 5 different strap options to determine desired operation, such as where the chip will load its parameters from (through an external EEPROM or from an external uP through the UART or SHI interface).

Table 3. Strap Option Pins to Select Desired Operation

Mode	**Pin 17 (GPIO7)**	**Pin 20 (STRAP0)**	**Pin 21 (MUTE_OUT)**
Internal(1)	0	0	X
Reserved	0	1	X
Small EEPROM (256 Byte)	1	0	0
Large EEPROM (1 KByte)	1	1	0
SHI	1	0	1
UART	1	1	1

Notes:
(1) Uses pre-defined parameters; please refer to Appendix section 13.2 for more details

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If one of the EEPROM modes is selected, use the strap option pins shown in the table below to select which section of the EEPROM to load parameters from.

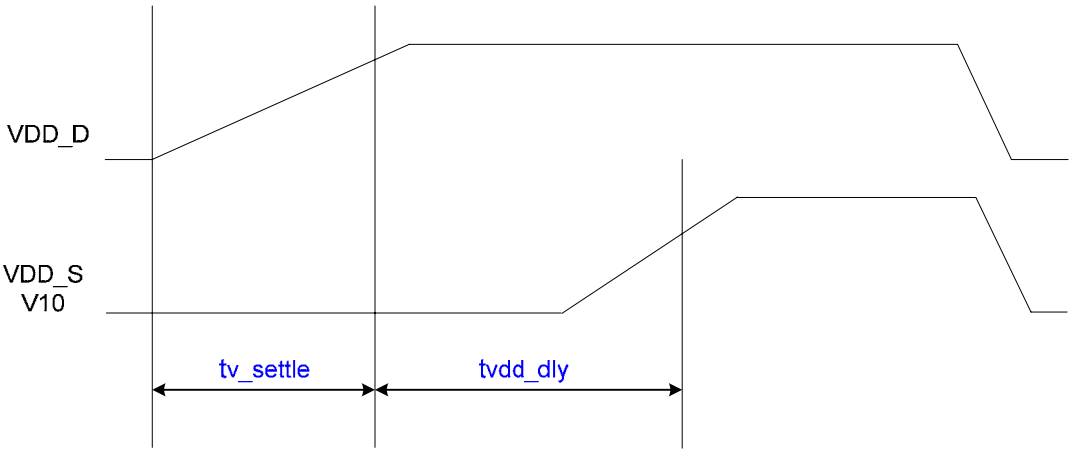
Table 4. Strap Option Pins for EEPROM

Starting Address			Pin 10 (PCM_OUT)	Pin 13 (UART_TX)
Segment	**Small (256 Byte)**	**Large (1 KByte)**		
0	0x00	0x000	0	0
1	0x40	0x100	0	1
2	0x80	0x200	1	0
3	0xC0	0x300	1	1

7.3 Power On/Off Timing

The following timing chart shows the power on sequence of 3 power pins, namely VDD_D, VDD_S and V10. The power off sequence is just the reverse order of power on.

Figure 19. Timing Chart of Power On/Off Sequence



VDD_S : for analog circuits, including PLL, CODEC, etc.
VDD_D : for digital pads.
VDD_D : for digital core.
tv_settle : Time for voltage to settle within 5% of the final voltage; 20µs < tv_settle < 10ms
tvdd_dly : Delay from VDD_D settle to VDD_S/V10 settle; 100µs < tvdd_dly.

Note:
1. To avoid voltage leakage between VDD_S and V10, these two suppy pins should be supplied together with a ferret bead separating them similar to the configuration provided in the reference board design.
2. The 100us t_{vdd_dly} is recommended to guarantee proper power-on reset. However, if the pull-high of the RST_ is delayed sufficiently long (> 5ms) after the VDD_S/V10 settle, this delay can be ignored.

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7.4 Accessing FM1185B Through EEPROM, UART, SHI

Users can read or write to registers in FM1185B (ex: to update parameters) through one of 3 interfaces: EEPROM, UART, or SHI. To access the registers in FM1185B, designers must use a pre-defined command entry pattern. The UART or SHI interfaces are used if applications require control through an external host (SHI is off after DSP is in normal operation mode).

Figure 20. Command Entry Data Pattern

Command Byte	Address Byte(s)	Data Byte(s)

The table below shows the available command entries and the associated number of bytes required for each entry.

Table 5. Command Entries

Command Entry	**Available for Interface**	**Command Byte**	**No. of Address Bytes**	**No. of Data Bytes**	**Total No. of Bytes**
Mem_write	UART, SHI, EEPROM	3B	2	2	5
Mem_read	UART, SHI	37	2	0	3
Short_reg_write	UART	68	1	1	3
Long_reg_write	UART	6A	1	2	4
reg_read	UART, SHI	60	1	0	2

7.4.1 Accessing Through EEPROM

Users can have a maximum of 4 different sets of parameters in the same EEPROM. Every time a reset is initiated, the user can select which set of parameters to access (see Table 3 in section 7.1). For a large size EEPROM (1 KByte), the absolute maximum number of bytes is 256 in each section.

When the EEPROM mode is selected to be the source to initialize the parameters after reset, the EEPROM access is set to burst mode up to 256 bytes. FM1185B will retrieve data continuously in burst mode until the end of transfer byte, “F0,” is detected. Then FM1185B will enter the normal operation mode.

7.4.2 Examples of Accessing Through EEPROM

The table below provides a few examples of how to update parameters in FM1185B through the EEPROM interface. For more details, please refer to the *FM1185 Parameter Tuning Guide*.

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Table 6. Examples of Accessing Through EEPROM

a. setup speaker volume 3b 1E 3E 02 00
b. set microphone PGA 3b 1E 34 00 33
c. set mic_in volume 3b 1E 3D 08 00
d. terminate EEPROM transfer 3b 1E 3A 00 00 F0 -- end of EEPROM initial read command (required)

7.4.3 Accessing Through UART

UART serves as an interface between the FM1185B and a host PC or controller, which can send commands to program the chip's parameters. UART is an asynchronous bi-directional serial interface; the protocol is determined by a start bit, number of character bits, a parity bit and a stop bit. The transfer speed is determined by the baud rate, which can be programmed internally. There is no clock signal between the transmitter and receiver.

There are 5 different types of command entries for the FM1185B UART interface. A sync word, "FCF3," is required before each command entry. Since the speed of the UART interface is much slower than the internal clock of FM1185B, it is safe to continue a write transfer without checking the status of the data transfer.

There are two access modes: mem_read and reg_read. Mem_read is used to read the memory contents and save them in registers 25 and 26 of FM1185B. Reg_read then transfers the register contents to the UART interface output pin TXD. The micro-controller host will then receive the register contents by monitoring the TXD pin.

No partial command entry is allowed. A partial command entry may cause system mal-function.

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7.4.4 Examples of Accessing Through UART

The table below provides a few examples of how to update parameters in FM1185B through the UART interface. For more details, please refer to the *FM1185 Parameter Tuning Guide*.

Table 7. Examples of Accessing Through UART

a. mem_write transfer `FC F3 3B 1E 34 00 55  -- write memory 1E34 with 0055`
b. mem_read `FC F3 37 1E 34  -- read memory contents of 1E34`
c. long_reg_write `FC F3 6A 2A 00 30  -- software reset of DSP`
d. reg_read `FC F3 60 25  -- read register 25`

e. read out contents of memory location 1E34
`FC F3 37 1E 34`
`FC F3 60 26  -- MSB of 1E34 will transmit through TXD`
`FC F3 60 25  -- LSB of 1E34 will transmit through TXD`

7.5 Miscellaneous Functions

Speaker Volume Control (Pins 25, 26)

The speaker volume of FM1185B can be controlled by the Vol- (pin 25) and Vol+ (pin 26) pins. These input signals are level triggered and active high. The DSP will increase/decrease the volume by one step once it senses a high signal on either pin (minimum length of active state is 80ms). If either pin is held high continuously, the DSP will increase/decrease the volume by 4 steps in 1 second. The step-size and maximum volume is programmable (see *FM1185 Parameter Tuning Guide*).

If these pins are not used, they must be pulled low using a weak 100K resistor.

Microphone Mute (Pins 21, 24)

A user can mute the microphone input of FM1185B by using mute_in (pin 24). This signal is level triggered and active high. The default setting after reset is the “no mute” mode, and will toggle between “no mute” and “mute” every time the signal is active (minimum length of the active state is 80ms). Please note that the mute function is not available in SHI mode, as pin 24 serves as the SDA pin of the SHI bus. The mute_out

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(pin 21) signal is active high and is a status indication of the “mute” mode. It will output a “high” if in “mute” mode.

If this pin is not used, it must be pulled low using a weak 100K resistor.

Earpiece and Speaker Mode (Pin 23)
This input signal is edge triggered. On the falling edge, FM1185B will switch to the “earpiece” mode, which has a lower internal power amplifier gain. On the rising edge, FM1185B will switch to the “speaker” mode, which has the standard internal power amplifier gain. If the built-in power amplifier is not used, the speaker PGA will be changed accordingly. Please note that this feature is not available in SHI mode, as pin 23 serves as the SCL pin of the SHI bus.

If this pin is not used, it must be pulled high with a weak 100K resistor to be in speakerphone mode.

7.6 System Clock

A user can apply a clock source (crystal or oscillator) of either 4.096MHz or 13MHz to pin 27 (XTAL_IN). A crystal applied to pins 27(XTAL_IN) and 28(XTAL_OUT) will also work. For more information on crystal specifications, please refer to section 10.

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8. Electrical & Timing Specification

8.1 Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VDD_S	-	2.0	V
Digital Input Voltage	VIN	-	3.6	V
Digital Output Voltage	VOUT	-	3.6	V
Storage Temperature	T_{stg}	-	-40 to 150	^{0}C

8.2 Recommended Operating Conditions

Table 9. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ESD Protection		HBM			2	kV
Power Supply Voltage(1)	VDD_S	-	1.62	1.8	2.0	V
I/O Supply Voltage	VDD_D		1.62	1.8 or 3.3	3.6	V
Operating Temperature	T_{amb}	-	-20	25	70	°C
Input High Voltage	V_{IH}		0.7*VDD_D		VDD_D	V
Input Low Voltage	V_{IL}		0		0.3*VDD_D	V
Master Clock Frequency	f_{mck}	XTAL_IN		4.096, 13		MHz
Master Clock Duty Ratio	D_{mck}	XTAL_IN	40	50	60	%
Bit Clock Frequency	f_{bck}	BCLK (Master Mode)	128	256	1,024	kHz
Bit Clock Frequency	f_{bck}	BCLK (Slave Mode)	128	256	4,096	kHz
Bit Clock Duty Cycle	D_{bck}	BCLK	40	50	60	%
Sync Signal Frequency	f_{sync}	FSYNC		8		kHz

Notes: The power ripple (AC element) has to be limited within 100mV

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8.3 DC Characteristics

Table 10. DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply for Core	V10		1.62	1.8	2.0	V
Power Supply Current	I_{SU}	Operating, Analog + Digital	-	17	19	mA
Power Down Current	I_{PD}	PWD_ is low	-	-	40*	uA
Input Leakage Current	I_{IH}	V_I = VDD_D	-	-	10	uA
	I_{IL}	V_I = 0 V	-	-	10	uA
High Level Digital Output Voltage	V_{OH}		0.9*VDD_D	-	VDD_D	V
Low Level Digital Output Voltage	V_{OL}		0	-	0.1*VDD_D	V
Digital Output Leakage Current	I_O		-	-	10	uA
Input Capacitance	C_{IN}		-	10	-	pF
Power Dissipation	P_{SYS}	V10 =1.8V, T_{amb}=25°C	-	30.6	34.2	mW

Notes:

° I_{PD} is only for V10. VDD_D and VDD_S leakage current may be up to additional 20 uA.

8.4 AC Characteristics

Table 11. AC Characteristics (room temperature, gain set to 0dB)

Parameter	Condition	Min	Typ	Max	Unit
Mic0 & Mic1 Input Range (differential)	Reference as 0dB full scale		2.4		Vpp
Line_in Input Range (differential)	Reference as 0dB full scale		2.4		Vpp
Spk_out Full Scale Output (differential)	Reference as 0dB full scale		2.4		Vpp
Line_out Full Scale Output (single-ended)	Typ is @ 0dB PGA gain; Max is @ 2dB PGA gain		1.2	1.5	Vpp
SNR for Line_in (digital or			84		dB

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analog) to Spk_out Path					
SNR for Mic0 & Mic1 to Digital Line_out Path			84		dB
SNR for Mic0 & Mic1 to Analog Line_out Path		70	76		dB
CODEC Sampling Frequency			8		KHz
Input Impedance for Mic/Line_in	Reference as 0dB full scale		25		kΩ
Load impedance for Line_out / Spk_out		600			Ω

Table 11a. ADC PGA Gain (Mic0, Mic1, Line_in)

Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Gain Range		-2	-	26	dB
Step Size	Range: -2dB to 0dB	-	1	-	dB
Step Size	Range: 0dB to 26dB	-	2	-	dB
Step Size Error	Range: -2dB to 0dB	-0.5		0.5	dB
Step Size Error	Range: 0dB to 26dB	-1	-	1	dB

Note:
(1) Please refer to the FM1185B Input High Pass Filter Design App Note for more information regarding use of the ADC PGA Gain

Table 11b. DAC PGA Gain (Line_out, Spk_out)

Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Gain Range		-29	-	2	dB
Step Size	Range: -29dB to 2dB	-	1	-	dB
Step Size Error	Range: -29dB to 2dB	-0.5	-	0.5	dB

8.5 DSP Performance Details

Table 12. DSP Performance Details

Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Acoustic Echo Cancellation	2-mic mode	-	-	60	dB
Stationary Noise Suppression	For Mic0, Mic1		12		dB
Non-stationary Noise Suppression	For Mic0 & Mic1 Beam-forming		20		dB
Beam-forming angle	Using SAM (small array microphone)			120	Deg
Side Tone Cancellation		25	-	35	dB
Acoustic Echo Tail Length		64	-	100	ms
Echo Convergence	2-mic mode	-	30	-	ms

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Noise Convergence	2-mic mode	-	1.5	-	s

8.6 Timing Characteristics

Table 13. Timing Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-down to power-up time	t_{pdu}		100	-	-	us
Set parameter timing after reset	t_{param}		4	-	-	ms
Data delay after parameter setting	t_{data}		-	70	-	ms
Speaker out delay after parameter setting	t_{spk}		-	75	-	ms
Mic to Line_out delay	t_{mlo}	2 mic mode	-	54	-	ms
Bit clock frequency	f_{bclk}	Output Mode	128	256	1,024	kHz
FSYNC Setup Time	t_{fs}		10	-	-	ns
FSYNC Hold Time	t_{fh}		10	-	-	ns
Input Setup Time	t_{ds}		10	-	-	ns
Input Hold Time	t_{dh}		10	-	-	ns
Digital Output Delay Time	t_{dd}	Output Mode	-	-	30	ns
FSYNC Output Delay Time	t_{fd}	Output Mode	-	-	30	ns

Figure 21. Power-down to Speaker-out Timing

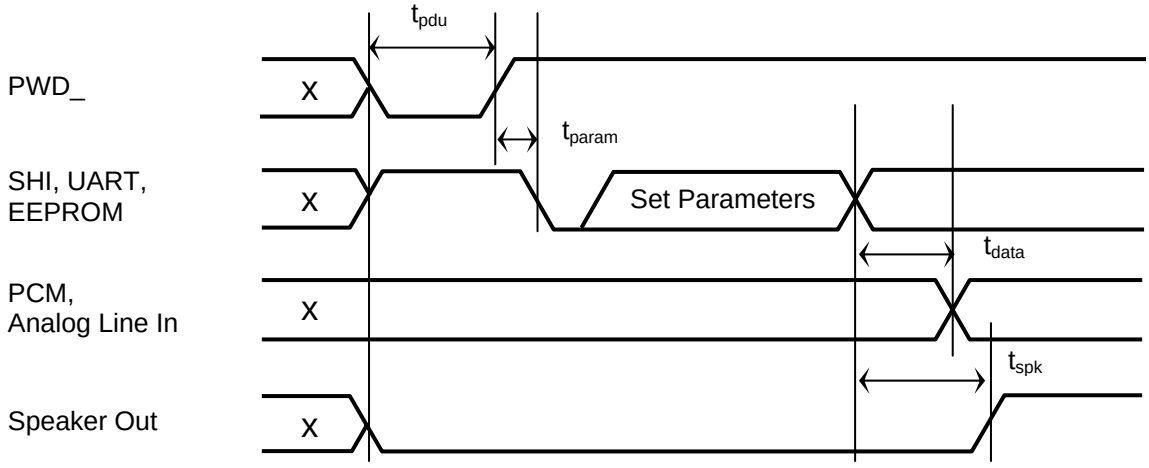

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Figure 22. Digital Input Timing (No Clock Delay)

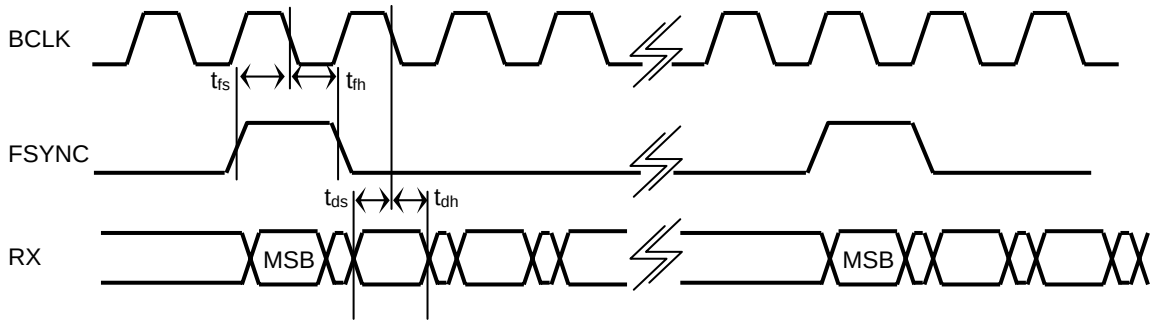

Figure 23. Digital Input Timing (One Clock Delay)

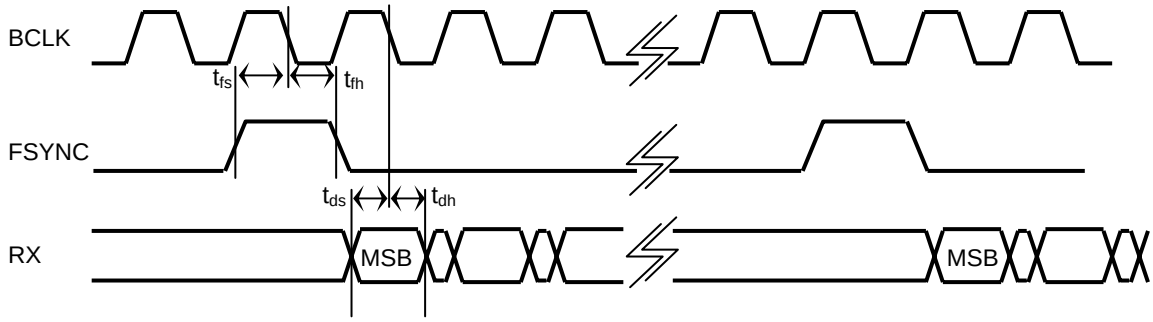

Figure 24. Digital Output Timing (No Clock Delay)

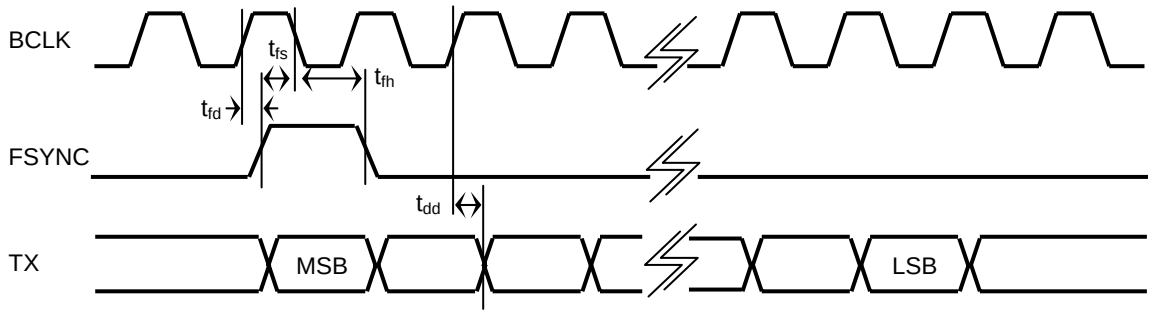

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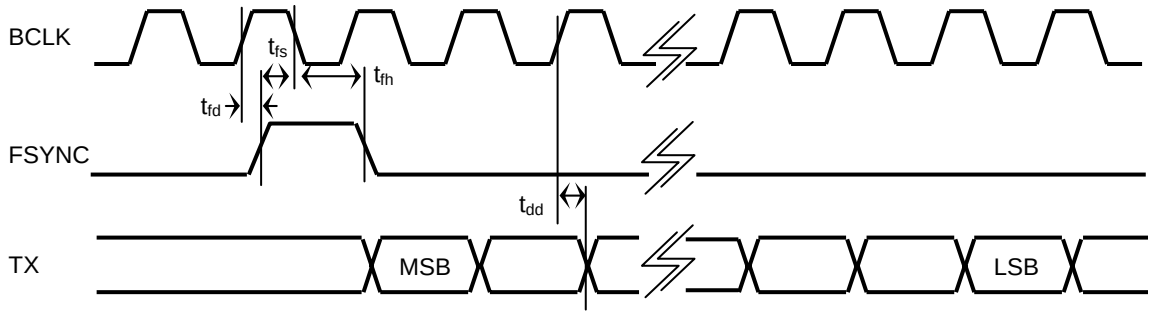
Figure 25. Digital Output Timing (One Clock Delay)



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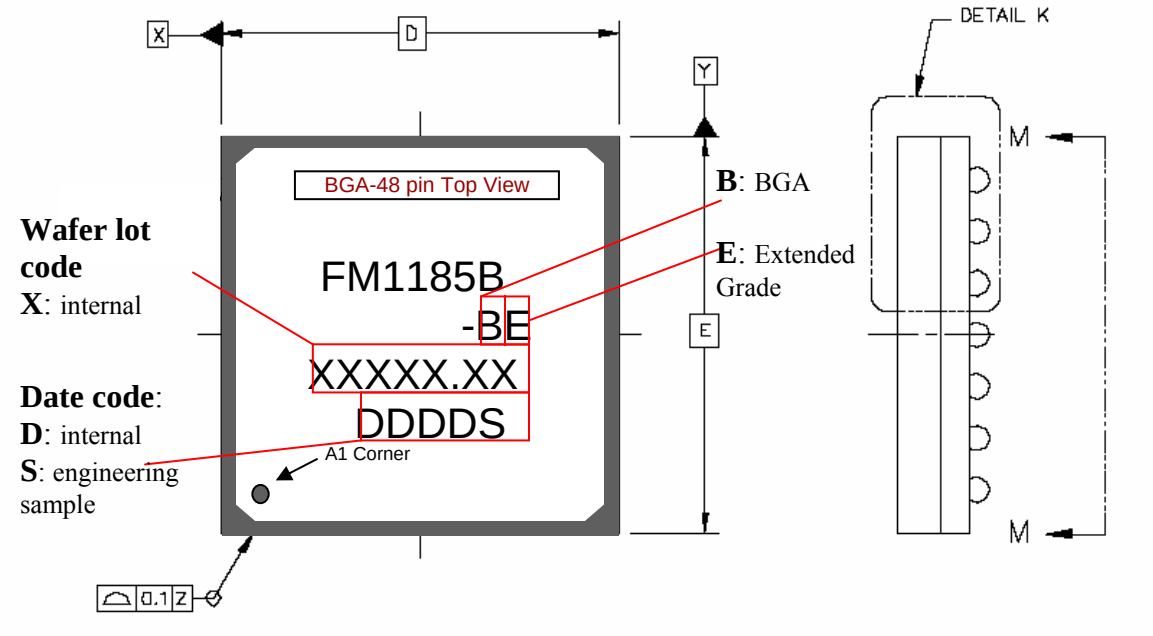
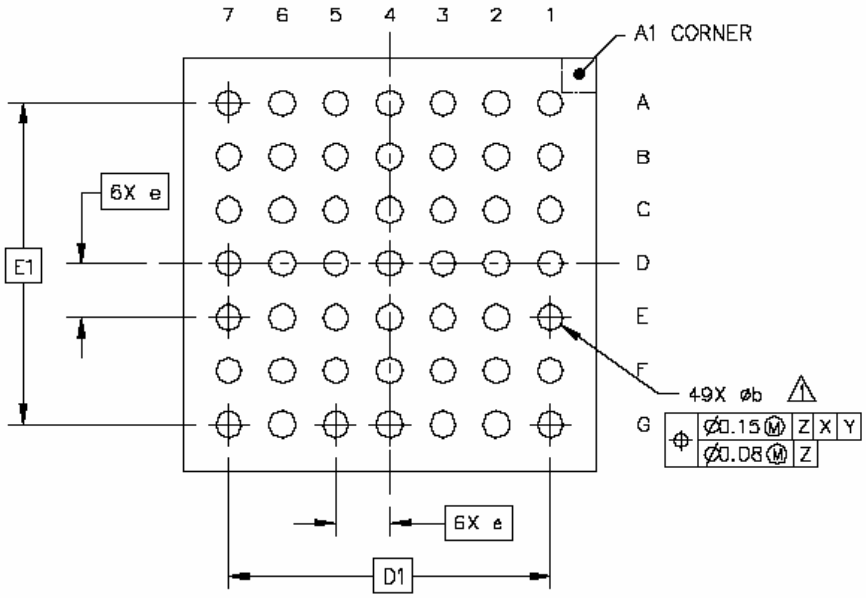
9. Package Dimensions (LQFP & BGA)

Figure 26. 48-pin BGA Package Drawing and Dimensions

Top and Side View



Bottom View



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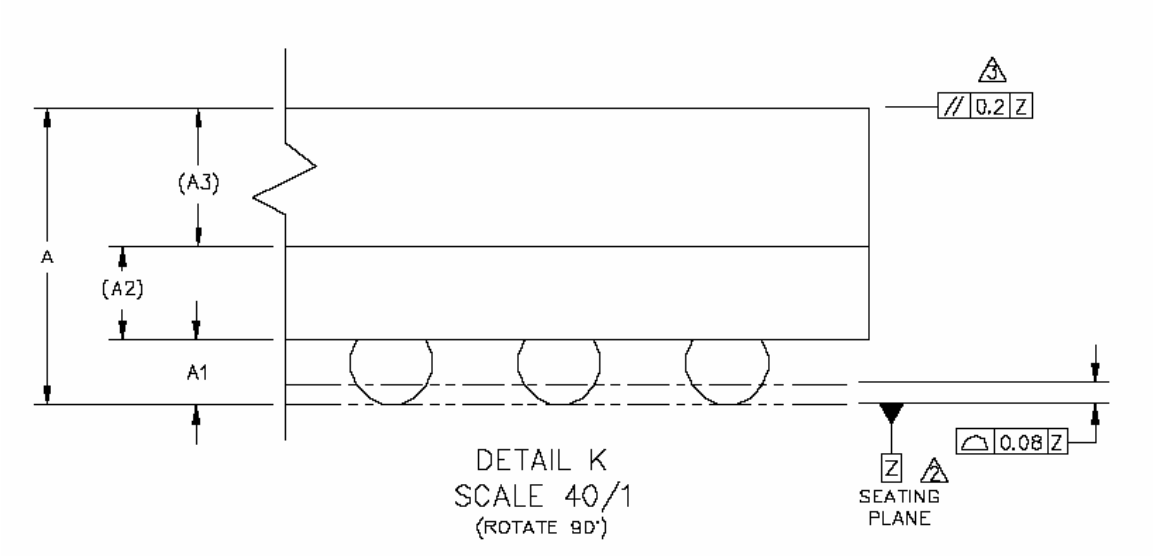

Notes: 1 Dimension b is measured at the maximum solder ball diameter, parallel to datum plan Z.

2 Datum Z (seating plane) is defined by the spherical crowns of the solder balls.

3 Parallelism measurement shall exclude any effect of mark on top surface of package.

Dimension	MIN	NOR	MAX	Unit
A	--		1.2	mm
A1	0.16		0.26	mm
A2		0.36 REF		mm
A3		0.54 REF		mm
b	0.27		0.37	mm
D	4.9	5 BSC	5.1	mm
E	4.9	5 BSC	5.1	mm
e	0.575	0.65 BSC	0.725	mm
D1	3.75	3.9 BSC	4.05	mm
E1	3.75	3.9 BSC	4.05	mm

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10. Required External Components for Operation

Microphone

Type:	Electret Condenser Microphone
Sensitivity:	-44 ~ -47 dB (1V/PA)
Operating Voltage:	2V (standard)
Impedance:	2.2k ohm maximum

Speaker

Amplifier with 20k ohm input impedance is preferred.

Crystal/Oscillator (see section 7.5 for more details)

Table 14. General Crystal Recommendations

Parameter	**Value**
Table Operating Frequency	4.096 MHz or 13 MHz
Resonant Mode	Parallel
Frequency Tolerance	+/- 30 PPM
Aging per Year	+/- 5 PPM / Yr
Operating Mode	Fundamental Mode
Crystal Co	< 10 pF
Crystal Rs (ESR)	< 150 Ω
R_S (external)	330 Ω
CL (external load capacitance)	16 pF
Drive Level	500 uW

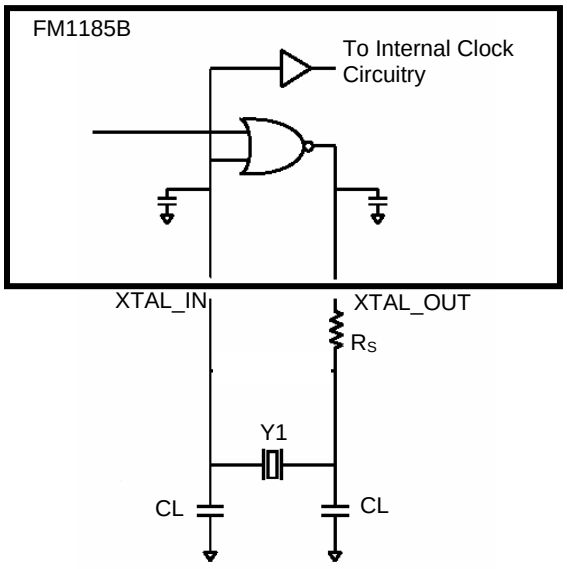

Figure 27. External XTAL_IN Clock Source

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Serial EEPROM (optional)

Fortemedia recommends using a 1.8V serial EEPROM such as 24AA02 (256Byte – small size) or 24AA08 (1KByte – large size).

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11. Audio Measurement System

Settings
PC microphone: -45dB sensitivity
Speaker: 8W

Table 15. Echo Cancellation Measurement

Parameter	Condition	Typical
Acoustic Echo Cancellation	Voice band	50 to 60dB

Figure 29. Echo Cancellation Test Setup

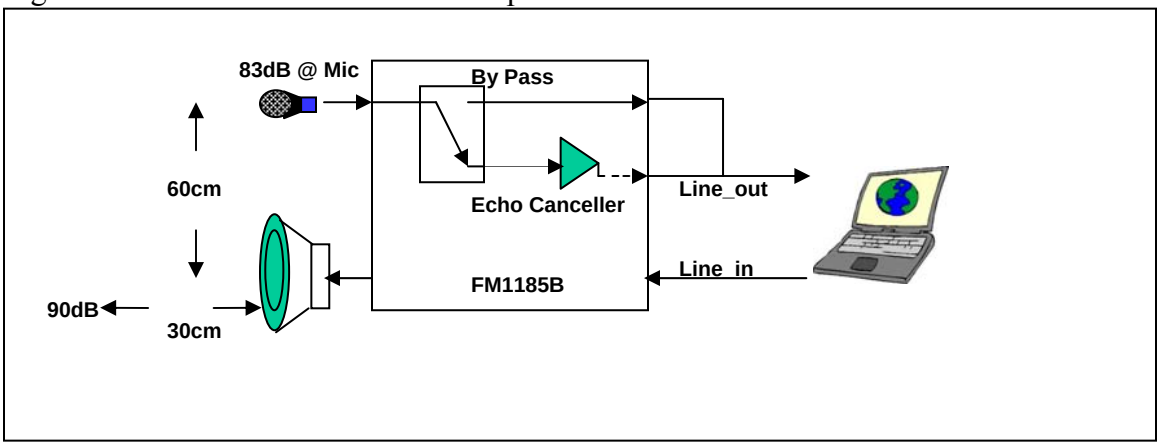
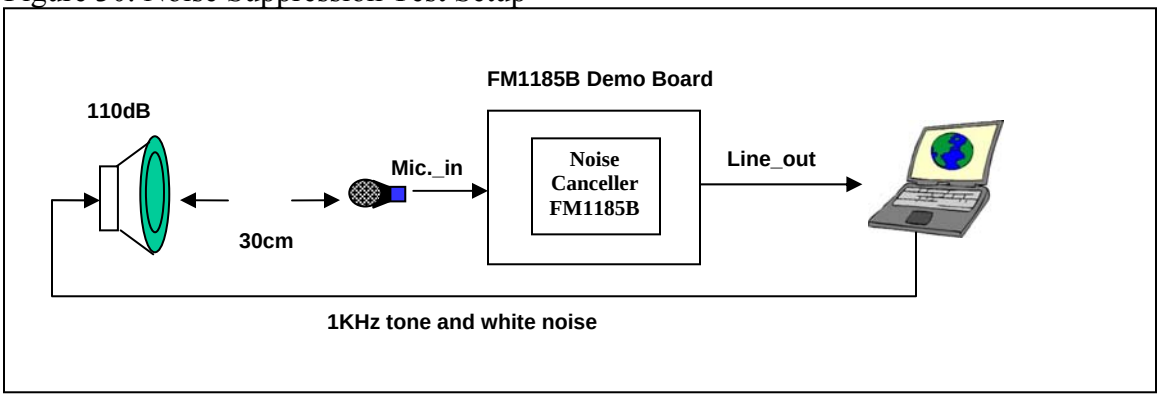


Table 16. Noise Suppression Measurement

Parameter	Condition	Typical
Stationary Noise Suppression	1KHz tone and white noise	12dB

Note: Adaptive time is between 1 to 2 seconds

Figure 30. Noise Suppression Test Setup



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12. Ordering Information

Table 17. Available Devices

Package	Green	Temperature Grade	Ordering Code	Shipment Method
48-pin BGA	Yes	Extended	FM1185B-BE	Tape & Reel

Note: Consumer = 0 to 70 degrees C
Extended = -20 to 70 degrees C
Auto = -40 to 85 degrees C

Fortemedia recommends consuming the devices within 192 hours after opening of the vacuum seal. Devices still on the reel, which cannot withstand high temperatures, are not recommended for re-baking. For more information, please refer to the "Handling Precautions" document.

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13. Appendix

13.1 Related Documents

1. Fortemedia Technology White Paper
2. AN: FM1185 SHI Implementation
3. FM1185 Parameter Tuning Guide

13.2 Pre-defined Settings for Operation in Internal Mode

Table 18. Strap Pin Settings for Default Internal Mode Profiles

Profile	**Pin 13**	**Pin 21**
1-mic (uni), analog	0	0
1-mic (omni), analog	0	1
Uni-omni (default), analog	1	0
Omni-omni, analog	1	1

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