fortémedia

FM1188
Low-Power Voice Processor

Preliminary Data Sheet V1.25
April 2009

PRELIMINARY INFORMATION

TABLE OF CONTENT

FIGURES

TABLES

Revision History

Revision	Description	Date
0.7	Initial Release	Dec. 2007
0.71	Include software update	Jan. 2008
0.72	Make it consistent with other 118x family	Jan. 2008
0.73	Initial outbound advanced release	Jan. 2008
0.74	Change the crystal circuitry information, line_in to spk_out bypass, power consumption	Apr. 2008
0.75	Correct noise convergence time and echo tail length	May 2008
1.0	Preliminary DS coinciding with release to manufacturing accompanied by bench characterization data.	July 2008
1.1	Change in AC Design Parameter	Dec 2008
1.2	Correct missing section 2.1 header. Other wording edits. No technical change.	Jan 2009
1.2	Add Sidetone Cancellation tail length on Tab. 16. (incorrrectly refered to as the "LEC" block in tuning tools).	Apr 2009

1. Introduction

FM1188 is the newest member of Fortemedia's SAM (Small Array Microphone) technology SoC (System on Chip). It delivers improved noise suppression for both stationary noise and non-stationary noise with better voice quality and superior full duplex capability. With two microphones only 10mm apart, SAM technology surpasses conventional array microphone which requires significant distance between microphones in order to utilize the information due to different positions. The conventional requirement limits the flexibility of the application of array microphone for embedded applications. Fortemedia's breakthrough array microphone technology can avoid such spacing between microphones by customizing algorithm with characteristics of both unidirectional and Omni-directional microphones.

1.1 Overview

The FM1188 voice processor has the latest Fortemedia voice quality improvement in one ultimate high-performance, low-power single chip solution for echo cancellation and noise suppression. Providing SAM (small array microphone) technology with beam-forming capability at only 35mW of power consumption, FM1188 is ideal for any portable application with stringent requirements for battery life and power consumption. Offered in a small 5x5mm BGA package, FM1188 is ideally suited for applications including portable hands-free car kits (HFCK), PNDs, notebook computers, Tablet PCs, and VoIP phones.

To achieve the lowest possible power consumption, FM1188 features an integrated hardware accelerator to speed up voice related applications. This new device is designed to achieve the lowest power while providing the highest performance. With an enhanced CODEC, FM1188 provides high SNR for the best voice quality. FM1188 provides excellent noise suppression and full duplex capabilities, including non-linear echo cancellation and side tone cancellation.

FM1188 is pin compatible with FM1182E but lacks USB support..

For more details on Fortemedia technology, please refer to the *Fortemedia FM1188 Tuning Guide*.

1.2 Key Features
- Highly integrated single chip solution
    - Voice processor with Hardware Accelerator
    - 3 ADC (Analog to Digital Converter)
    - 2 DAC (Digital to Analog Converter)
    - RAM, ROM
    - On-chip microphone amplifier
    - SHI, UART interface to external controller
- Low power consumption (typically 30mW with all signal processing features on)
- High performance
    - Powerful AEC (acoustic echo cancellation) (65dB)
    - Superior full-duplex
    - Supports 1 & 2 microphone modes
    - Differential I/O to reduce RF interference and increase noise immunity
    - Dynamic range control (DRC) to increase voice intelligibility
    - Side tone cancellation of 25 to 35dB
    - Acoustic echo tail length coverage: 64 to 100ms
    - Mic_in & Line_in PGA (programmable gain amplification) range from -2dB to +26dB
    - Line_out & Spk_out PGA range from -29dB to +2dB
    - On the fly switching between various bypass mode to voice processing mode Extended bypass modes support, configurable main and reference microphone (MIC0 or MIC1)
        - Main mic to LINE_OUT, LINE_IN to SPK_OUT, no gain or configurable gain
        - Reference mic to LINE_OUT, LINE_IN to SPK_OUT, no gain or configurable gain
        - Main mic to SPK_OUT, LINE_IN to LINE_OUT, no gain (Self-loop back)

    o   Mic_in and Line-in AGC
    o   Speaker equalization and volume enhancement in noisy environment
- Supports 2 types of clock inputs: 4.096MHz or 13MHz
- Available in 48-pin BGA and 48-pin LQFP packages

1.3 Pin Configuration
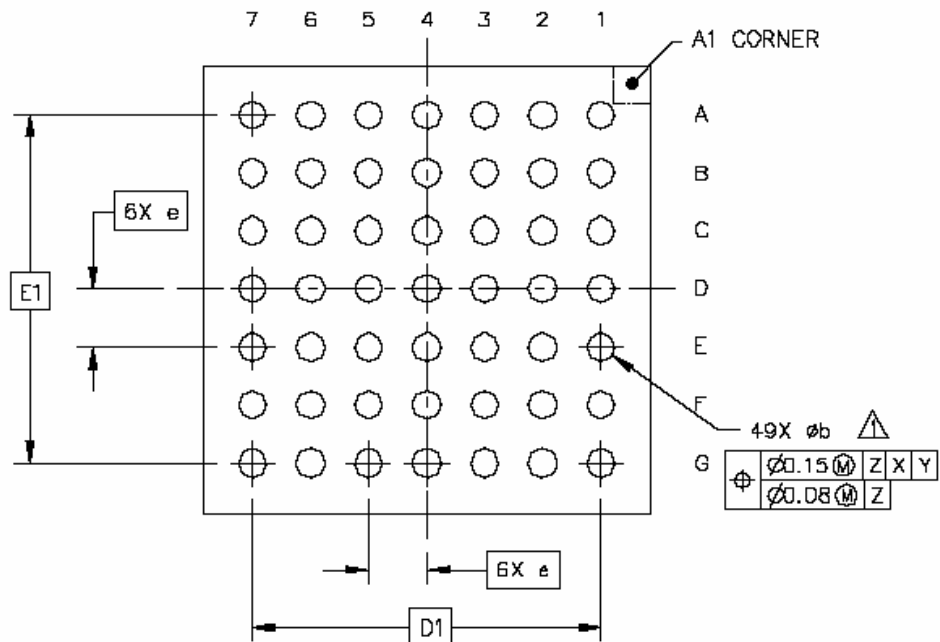
Figure 1: BGA Pin Configuration (Bottom View)
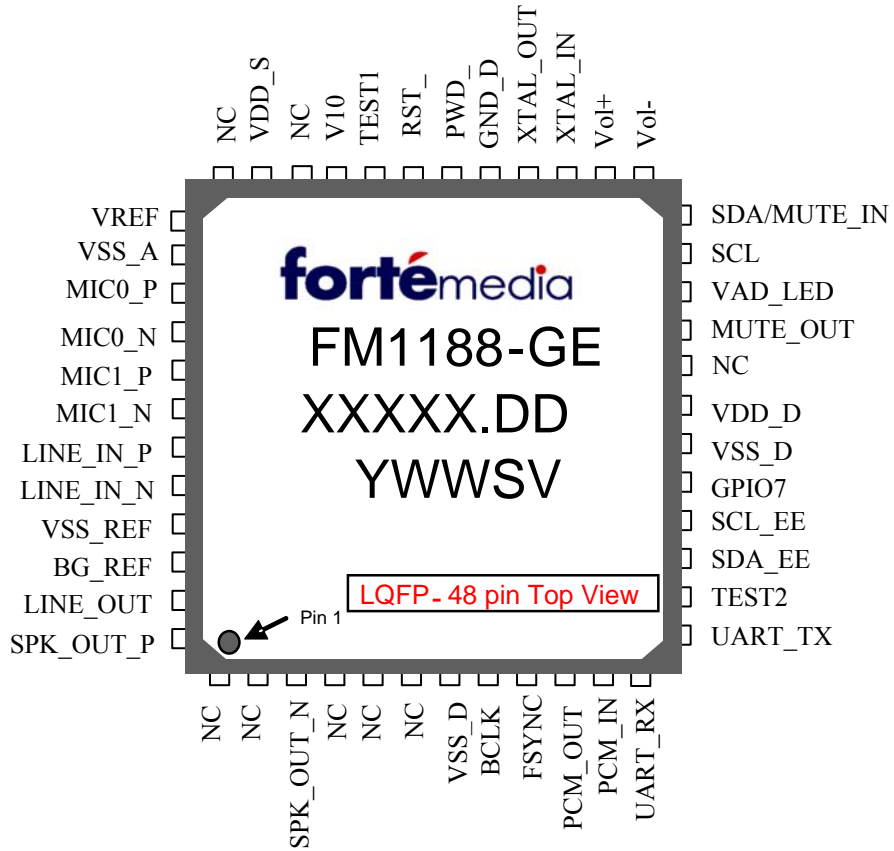
Figure 2: LQFP Pin Configuration (Top View)

1.4 Internal Hardware Block Diagram
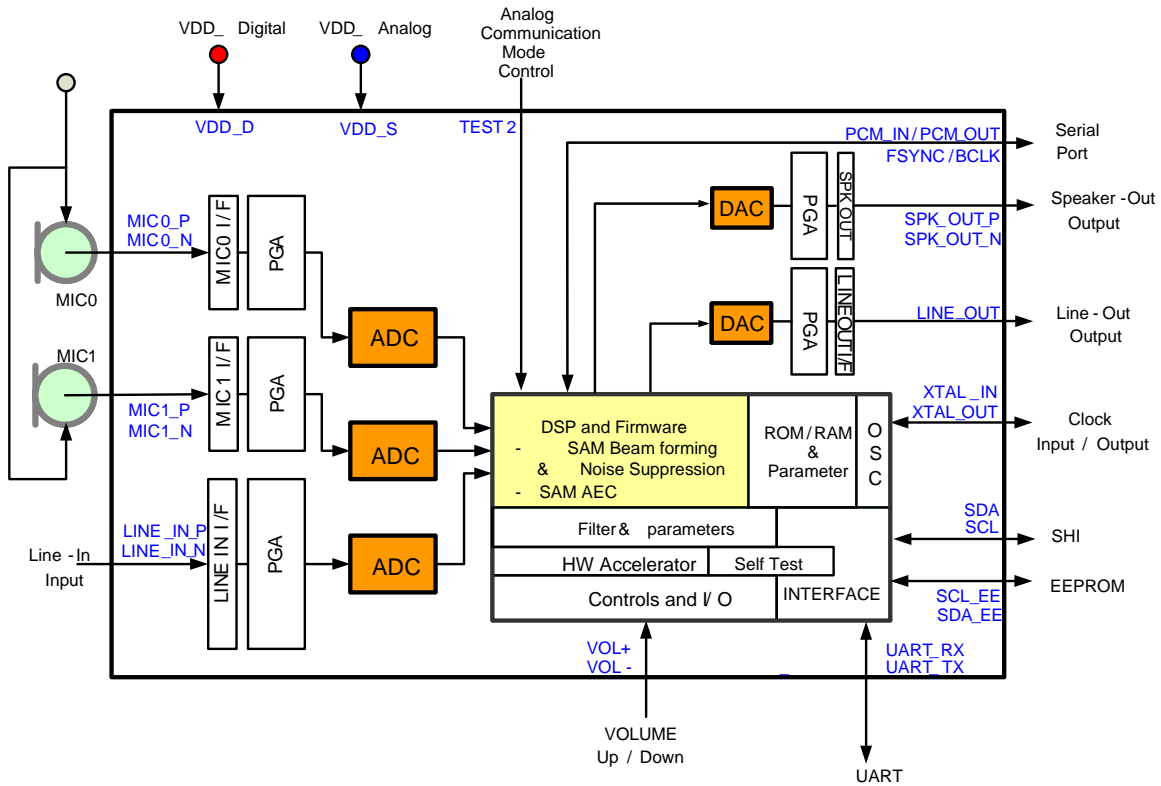
Figure 3: IC Hardware Block Diagram

1.5 System Application Block Diagram
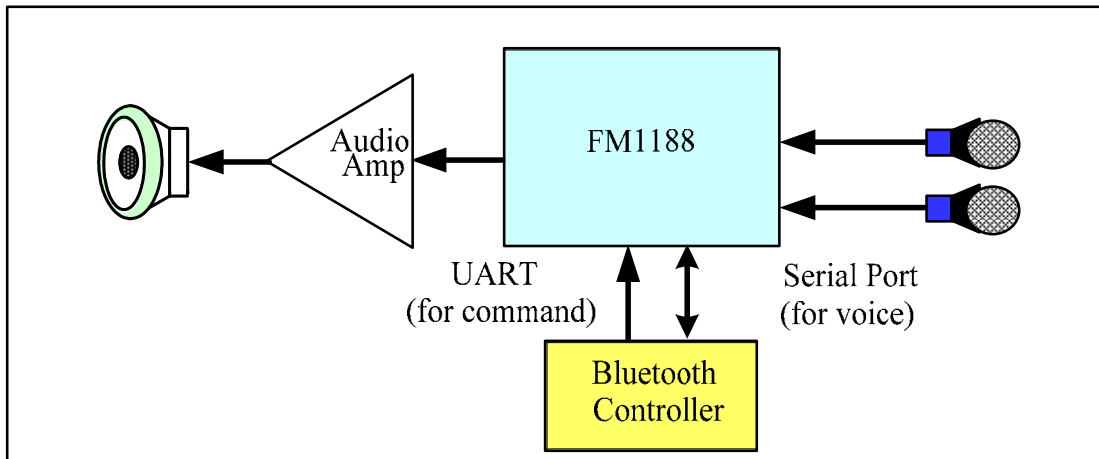
Figure 4: Bluetooth Application Block Diagram

2. Functional Description
2.1 Overview
The FM1188 voice processor digitizes the two microphone inputs and processes them with SAM noise suppression algorithm and echo cancellation functions, The result is output through either Serial PCM Port or D/A converter for the Line_Out signal (analog interface). The line input from either Serial PCM Port or the Line_In signal is primarily used as a reference for its DSP algorithm to cancel the echo. This line input is further processed by the DSP algorithm to perform functions such as side tone cancellation or Dynamic Range Control before sending out to the SPK_Out signal. The other functions are explained in the following.

2.2 Serial EEPROM Interface (Pins 15, 16)
FM1188 supports a serial interface to an optional external EEPROM. It supports 256 bytes (small sized) and 1Kbytes (large sized) EEPROM. Upon FM1188 initial selection of this mode, internal parameters are downloaded through this EEPROM interface. An example of retrieving data instruction is shown in below figure.
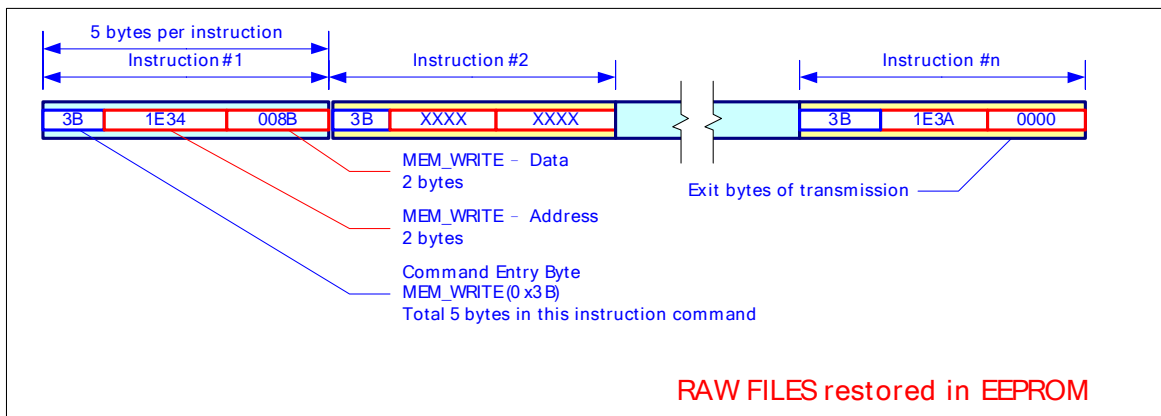
Figure 5: EEPROM Command Instruction

2.3 UART Interface (Pins 12, 13)
FM1188 has one UART port which is used to transmit and receive control commands. Each transfer will have one command byte, one or two address bytes, and up to two data bytes. UART requires two bytes "FC" and "F3" to synchronize with each transfer. The top speed of the UART interface is 38400bps with 13MHz input, or 115200bps with 4.096MHz.

The UART port is recommended as the standard interface to access FM1188.
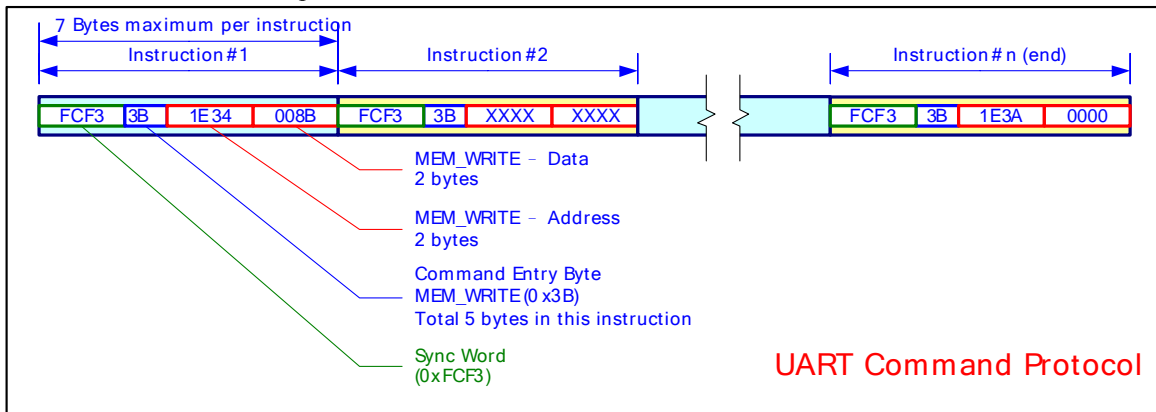
Figure 6: UART Command Protocol
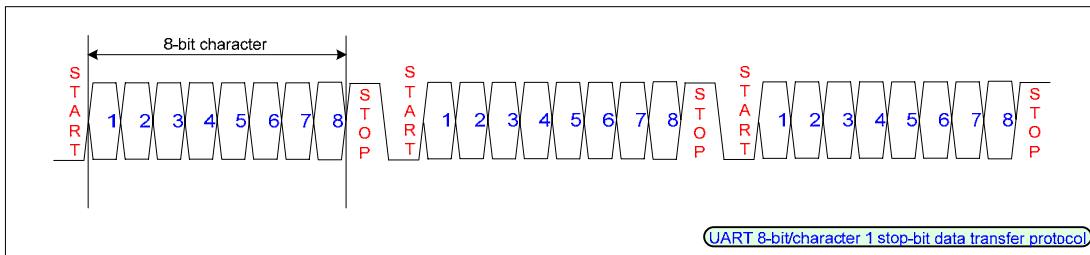
Figure 7: UART Data Transfers (TX and RX)

2.4 SHI (Serial Host Interface) (Pins 23, 24)

The SHI block is a serial interface between FM1188 and an external micro-controller. FM1188 communicates to the micro-controller through a bi-directional serial data line and a serial clock line. The standard byte format of SHI data line(Pin 24) must be 8–bit long in every byte. An acknowledge bit is necessary to follow each byte transmission, and there is no restriction on the maximum number of bytes per data transfer. Data transfer can be aborted if the master device generate a STOP condition to terminate a transfer. The master device is obligated to generate an acknowledge-related clock pulse through the clock line(Pin 23). The SHI interface supports up to the maximum clock speed of 100 kHz. Each data transfer must compose of one command byte, one or two address bytes, and a maximum of two data bytes. SHI command protocol requires two bytes "FC" and "F3" to synchronize with each transfer. Note that SHI is used for transferring parameters after reset, and is turned off when the Voice Processor enters into normal operation mode. Refer to *AN: FM1188 SHI Implementation* for more details.
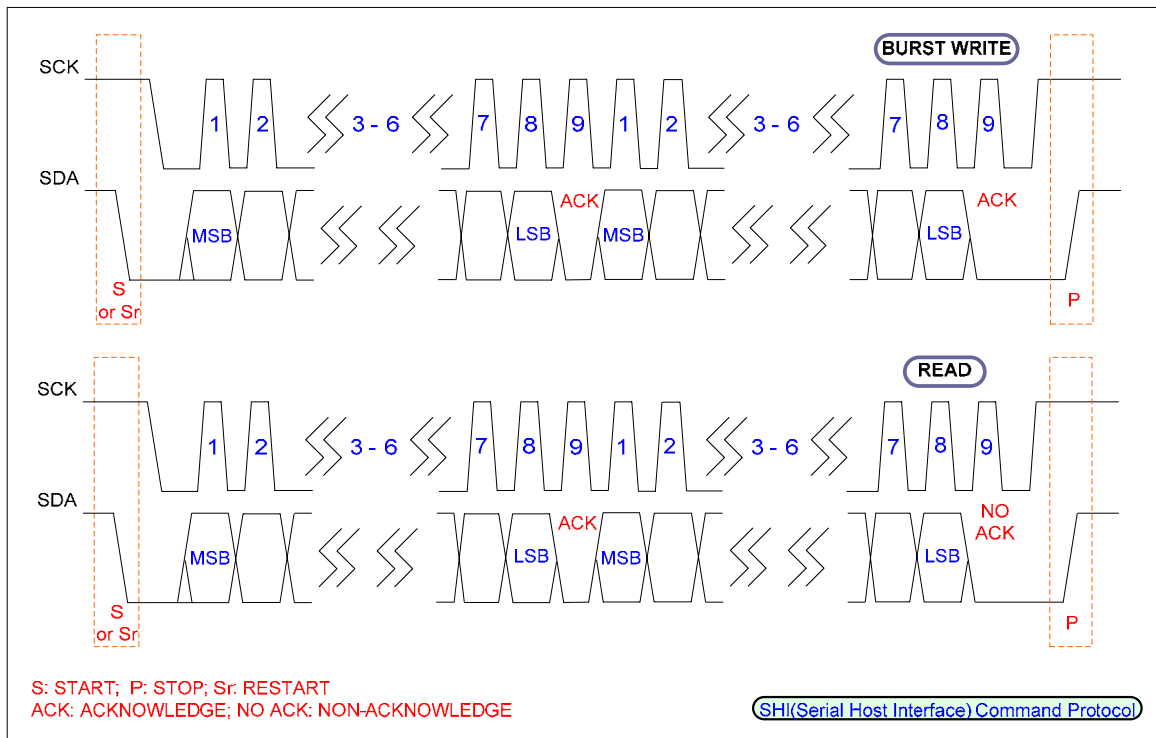
Figure 8: SHI (Serial Host Interface) Data Transfer Command Protocol
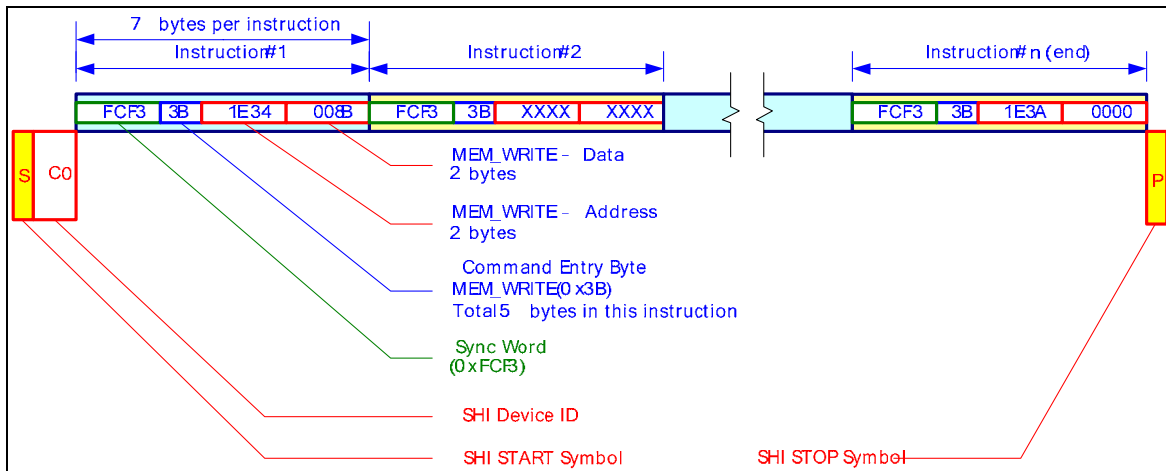
Figure 9: SHI (Serial Host Interface) Command Sequence

2.5 Serial Port (Pins 8, 9, 10, 11)

The serial port provides an interface to an existing host (micro-controller) for digital voice data transfer. Both the master and the slave modes support either an internal or external clock source for the FSYNC and BCLK signals. While operating with the internal clock or external clock, FSYNC runs at 8KHz.

The serial port data format can be linear pulse code modulation (linear PCM). The default setting is to run 16-bit linear PCM mode. Other supported linear PCM formats includes 13-bit zero padding and 13-bit sign extension that can be selected by EEPROM or an external controller.

In the slave mode, FM1188 accepts both short and long "FSYNC" and in the master mode, FM1188 drives short "FSYNC". Table 1 below shows the status of the serial port output pins during different modes.

Table 1: Status of Serial Output Pins

	Master Mode			Slave Mode		
Pin Name	Power-down	Serial Port Disabled [1]	Analog Communication Mode [2]	Power-down	Serial Port Disabled [1]	Analog Communication Mode [2]
BCLK	Tri-state	Normal	"0"	note [3]	note [4]	"0"
FSYNC	Tri-state	Normal	"0"	note [3]	note [4]	"0"
PCM_OUT	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state

Notes:
1. Setting (bit8 of 0x1E30) to "0" will disable the serial port (Refer to FM1188 Parameter Tuning Guide).
2. Asserting TEST2 will go into Analog Communication Mode.
3. The logic state will be the same state before the Power –down.
4. The logic state will be the same state before the Serial Port Disabled
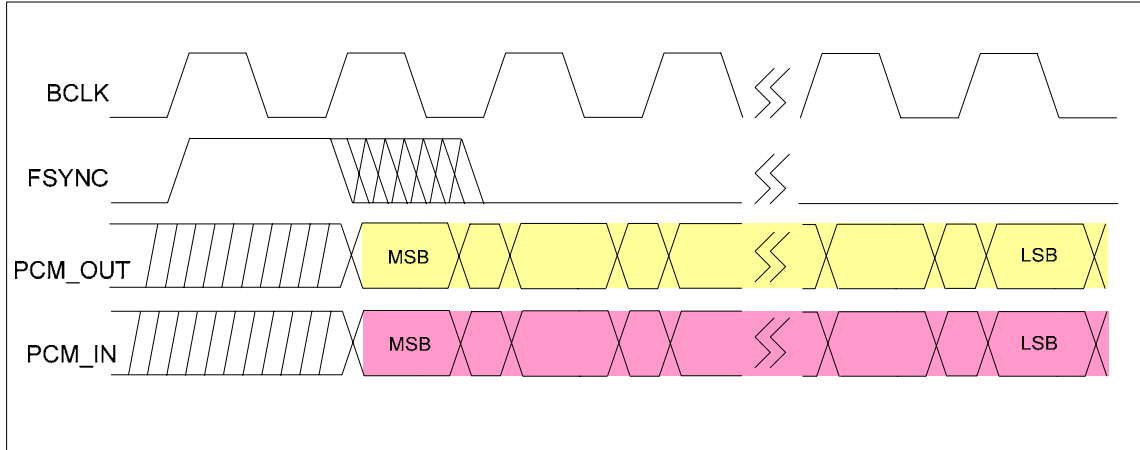
Figure 10: Serial Port - One Clock Delay
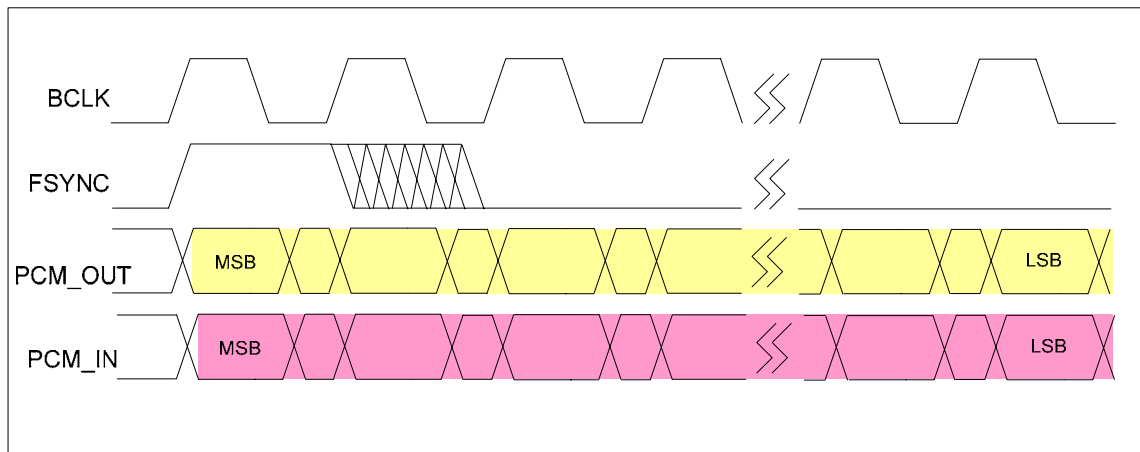
Figure 11: Serial Port - Zero Clock Delay

2.6 ADC (Pins 39, 40, 41, 42, 43, 44)

FM1188 includes 3 analog-to-digital converters (ADC). The converters are at 16-bit precision and 8K sampling rate with sigma-delta architecture. All 3 converters are differential; they are used for 2 microphone inputs with built-in microphone pre-amplifier and 1 line level input. The full scale of the input is 2.4Vpp. See Figure 14 for details.

For more information on how to program the attenuation/gains for the ADC and DAC blocks, please refer to the *FM1188 Parameter Tuning Guide*.
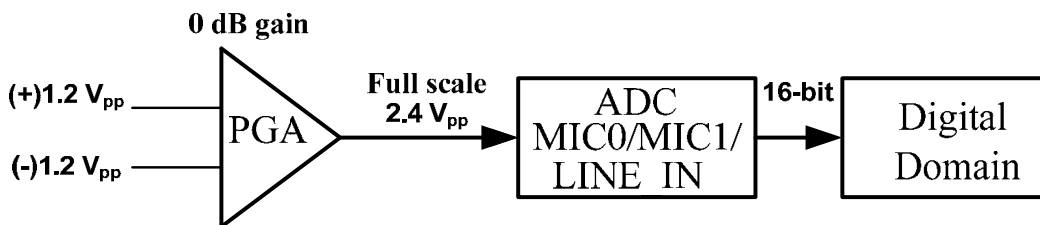
Figure 12: Analog-to-Digital Converter Block Diagram

2.7 DAC (Pins 3, 47, 48)

FM1188 includes two digital-to-analog converters (DAC). The converters are at 16-bit precision and 8k sampling rate with $\Sigma\Delta$ architecture. One of the converters (differential output) is used to feed into an external power amplifier to drive the speaker (Spk_out). The other converter (single-ended) provides programmable attenuations/gains that can be connected to an analog input (Line_out). See Figure 15 for more details.

For more information on how to program the attenuation/gains for the ADC and DAC blocks, please refer to the *FM1188 Parameter Tuning Guide*.
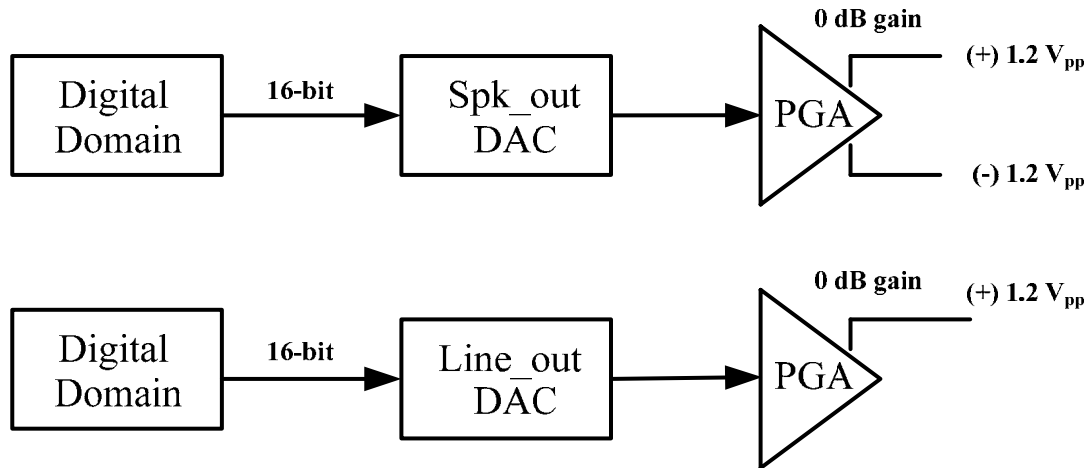
Figure 13: Digital-to-Analog Converter Block Diagram

2.8 Modes of Operation

Depending on the condition, the FM1188 chip may operate in one of the following 4 modes.

Hardware Reset Mode

Whenever power is applied or when RST_ is low, the chip will enter into this mode and remain until 10ms after the RST_ pin is pulled high. In this mode, the chip samples the strap-options, adjusts the clock source, and waits for the external clock (XTAL_IN or BCLK) and internal PLL to stablize. After the 10ms, the chip enters the Software Reset Mode. Note that RST_pin should not be used as a power-down function.

Software Reset Mode

In this mode, the embedded Voice Processor software reads the strap-options (section 2.9), determines where the parameters will be coming from, and then either waits passively for the download from an external host (through UART or SHI) or it actively reads the parameters from an external EEPROM. The chip exits this mode and moves to the Operational Mode after the Software Reset Mode when the parameter value at 1E3A becomes 0 (handled by embedded Voice Processor when parameter configuration is done). Note that RST_pin should not be used as a power-down function.

Operational Mode

In this mode, software will set up hardware internal registers according to the parameter configuration which followed by a nominal 70 ms initialization. Then FM1188 starts to samples its input and delivers its outputs through the analog/digital interfaces. After this operation, the chip may enter the Power Down Mode if the PWD_ pin is pulled low.

Power Down Mode

The chip enters the Power Down Mode 10ms after the PWD_ pin is pulled low. During the Power Down Mode, because the on-chip PLL is turned off, the PLL source clock can be also be turned off. After the Power Down Mode, the chip may move to either the Software Reset Mode or the Operational Mode (depending on the setting of the pwrdwn_set parameter, 0X1E51). If it moves to the Operation Mode, no parameter setting is required since all the internal register value will be maintained. In order for the chip to exit the Power Down Mode correctly, the chip will need 13ms for house-cleaning work before it can take the new round of parameter download, or resume to the Operational Mode.
* Note:
1. In the above modes, FM1188 re-enters the Hardware Reset Mode whenever the RST_ pin is pulled low externally.
2. The RST__pin is not designed for power saving purpose, therefore it is advised to use PWD for power-down function.

The following figure is a state transition diagram which shows the FM1188 chip transition between these 4 states.
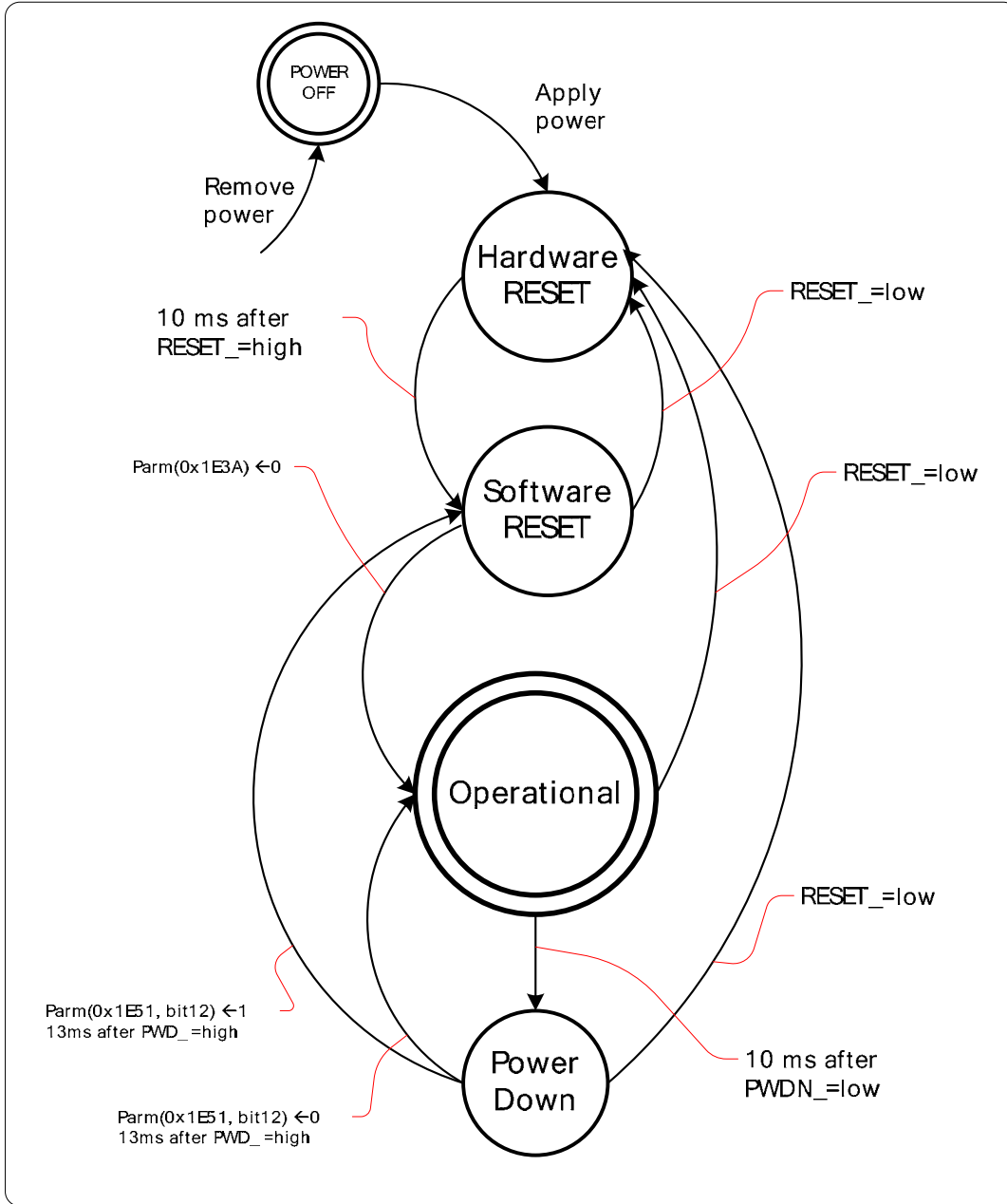
Figure 14: State Transition Diagram

2.9 Power-Up Option Pins (Strap Options)

Strap options are used to determine the desired operation of the chip. All the strap options mentioned below must be pulled high or low using a 100kΩ weak load. If pin left floating, the status will be unknown.

In the software reset mode, the chip samples 6 different strap options to determine desired operation, such as the source location of its parameters loading. (through an external EEPROM or from an external uP through the UART or SHI interface).

Table 2: Strap Option Pins to Select Operation Mode

Mode	Pin 17 (GPIO7)	Pin 20 (STRAP0)	Pin 21 (MUTE_OUT)
Reserved	0	0	X
Reserved	0	1	X
Small EEPROM (256 Byte)	1	0	0
Large EEPROM (1 KByte)	1	1	0
SHI	1	0	1
UART	1	1	1

If one of the EEPROM modes is selected, use the strap option pins shown in the table below to select which section of the EEPROM to load parameters from.

Table 3: Strap Option Pins for EEPROM

Segment	Starting Address		Pin 10 (PCM_OUT)	Pin 13 (UART_TX)
	Small (256 Byte)	Large (1 KByte)		
0	0x00	0x000	0	0
1	0x40	0x100	0	1
2	0x80	0x200	1	0
3	0xC0	0x300	1	1

2.10 Miscellaneous Functions

Speaker Volume Control (Pins 25, 26)

The speaker volume of FM1188 can be controlled by the Vol- (pin 25) and Vol+ (pin 26) pins. These input signals are level triggered and active high. The FM1188 will increase or decrease the volume by one step once it senses a level high signal on either pin (The minimum length of active high state is 150ms. The minimum length of de-active low state is 100ms). If the level stays high, every one second, it will continue to increase or decrease the volume until it hits the cap. The maximum volume is programmable (see *FM1188 Parameter Tuning Guide*).
If the pins are not used, they must be pulled low using a weak 100kΩ resistor.

Microphone Mute (Pins 21, 24)

A user can mute the microphone input of FM1188 by using mute_in (pin 24). This signal is level triggered and active high. The default setting after reset is the "no mute" mode, and will toggle between "no mute" and "mute" every time the signal is active (minimum length of the active state is 100ms, continuous press longer than 100ms will not further toggle the state). Please note that the mute function is not available in SHI mode when pin 24 serves as the SDA pin of the SHI bus. The mute_out (pin 21) signal is active high and is a status indication of the "mute" mode. It will output a level "high" if it is in "mute" mode.

If the pin 24 is not used, it must be pulled low using a weak 100 kΩ resistor.

Earpiece and Speaker Mode (Pin 23)

This input signal is edge triggered. On the falling edge, FM1188 will switch to the "earpiece" mode which has a lower internal power amplifier gain. On the rising edge, FM1188 will switch to the "speaker" mode which has the standard internal gain. Please note that this feature is not available in SHI mode when pin 23 serves as the SCL pin of the SHI bus.

If this pin is not used, pin must be pulled high with a weak 100kΩ resistor to be in speakerphone mode.

2.11 System Clock

A user can apply a clock source (crystal or oscillator) of either 4.096MHz or 13MHz to pin 27 (XTAL_IN). A crystal applied to pins 27(XTAL_IN) and 28(XTAL_OUT) will also work. For more information on crystal specifications, please refer to Appendix I.

2.12 Analog Communication Mode

The FM1188 supports an analog communication mode by asserting TEST2 pin to high. In this Analog Communication mode, the microphone input signal of MIC0_IN will route to LINE_OUT and LINE_IN to SPK_OUT directly through a pre-amplifier. It bypasses the internal ADC, DSP, and DAC. The gain control and internal pre-amplifiers are still working with the input and output signal.

The mode can be switched on-the-fly by the hardware TEST2 pin. The Analog Communication mode consumes less power than either 1 or 2 microphone mode since it halts the ADC/DAC and DSP operations.

3. Accessing FM1188 Through EEPROM, UART, SHI

Users can read or write to registers in FM1188 through one of the two interfaces: UART, or SHI. To access the registers in FM1188, designers must use a pre-defined command entry pattern (see figure below). The UART or SHI interfaces are used if applications require control through an external host (SHI is off after Voice Processor is in normal operation mode). As an option, the content in the external EEPROM can be automatically loaded into the registers after reset.

Command Byte	Address Byte(s)	Data Byte(s)

Figure 15: Command Entry Data Pattern

The table below shows the available command entries and the associated number of bytes required for each entry.

Table 4: Command Entries

Command Entry	Available for Interface	Command Byte	No. of Address Bytes	No. of Data Bytes	Total No. of Bytes
Mem_write	UART, SHI, EEPROM	0x3B	2	2	5
Mem_read	UART, SHI	0x37	2	0	3
Short_reg_write	UART	68	1	1	3
Long_reg_write	UART	6A	1	2	4
reg_read	UART	60	1	0	2

3.1 Accessing Through EEPROM

Users can have a maximum of 4 different sets of parameters in the same EEPROM. Every time a reset(i.e. power up reset or system cold reset) is initiated, the user can select specific set of parameters to access. For a large size EEPROM (1 Kbyte), each section can have the absolute maximum number of 256 bytes.

When the EEPROM mode is selected to be the source to initialize the parameters after reset, the EEPROM access is set to burst mode up to 256 bytes. FM1188 will retrieve data continuously in burst mode until the end of transfer byte "0xF0" is detected or until 0x1E3A is set to 0x0000. Then FM1188 will enter into the normal operation mode.

3.2 Examples of Accessing Through EEPROM

The table below provides a few examples of updating parameters in FM1188 through the EEPROM interface. For more details, please refer to the *FM1188 Parameter Tuning Guide*.

Table 5: Examples of Accessing through EEPROM

a. setup speaker volume `3B 1E 3E 02 00`
b. set microphone PGA `3B 1E 34 00 33`
c. set mic_in volume `3B 1E 3D 08 00`
d. terminate EEPROM transfer `3B 1E 3A 00 00 F0    -- end of EEPROM initial read command –`

3.3 Accessing Through UART

UART serves as an interface between the FM1188 and a host PC or controller that it can send commands to program the chip's parameters. UART is an asynchronous bi-directional serial interface and the protocol is determined by a start bit, number of character bits, a parity bit and a stop bit. The transfer speed is determined by the baud rate which can be programmed internally. There is no clock signal between the transmitter and receiver.

There are 5 different types of command entries for the FM1188 UART interface. Two synchronize bytes "FC" and "F3" are required before each command entry. Since the speed of the UART interface is much slower than the internal clock of FM1188, it is safe to continue a "write" transfer without checking the status of the data transfer.

There are two access modes: mem_read and reg_read. Mem_read is used to read the memory contents and save the contents in registers 25 and 26 of FM1188. Reg_read then transfers the register contents to the UART interface output pin TXD. The micro-controller host will then receive the register contents by monitoring the TXD pin. No partial command entry is allowed. A partial command entry may cause system mal-function.

3.4 Examples of Accessing Through UART

The table below provides a few examples of updating parameters in FM1188 through the UART interface. For more details, please refer to the *FM1188 Parameter Tuning Guide*.

Table 6: Examples of Accessing through UART

```
a. mem_write transfer
FC F3 3B 1E 34 00 55          -- write memory 1E34 with 0055


b. mem_read
FC F3 37 1E 34                -- read memory contents of 1E34


c. long_reg_write
FC F3 6A 2A 00 30             -- software reset of the voice processor

d. reg_read
FC F3 60 25                   -- read register 25


e. read out contents of memory location 1E34
FC F3 37 1E 34
FC F3 60 26        -- MSB of 1E34 will transmit through TXD
FC F3 60 25        -- LSB of 1E34 will transmit through TXD
```

3.5 Accessing Through SHI

User can use SHI interface to obtain parameters from an external master device to initialize FM1188 after reset. Data transfer are through the two bi-directional serial data and serial clock lines. All data are transmitted with the most significant bit(MSB) first. The SHI protocol's start condition command is "S" and stop condition command is "P" (please refer to figure 9). If a slave for any reason can't receive nor transmit another byte of data after the start condition, the master can be forced into a wait state by holding the clock line to a low state. When the slave is ready, it can then resume the data transferring for the next byte of data by releasing the clock line back to a high state.

3.6 Examples of Accessing Through SHI

The table below provides a few examples of updating parameters in FM1188 through the SHI interface.
For more details, please refer to the *FM1188 Parameter Tuning Guide*.

Table 7: SHI Command Symbols

Command Symbol	Definition	Command Symbol	Definition
W	SHI Write Control (Add as SHI ID Bit[0])	*AH*	Address High Byte
R	SHI Read Control (Add as SHI ID Bit[0])	*AL*	Address Low Byte
FC	Command Sync Byte-1	*DH*	Data High Byte Write
F3	Command Sync Byte-2	*DL*	Data Low Byte Write
3B	Memory Write Command Byte	*XX*	Dummy Byte used in Burst Write between W and FC
37	Memory Read Command Byte	RH	Read out Data High Byte
60	Byte Read Command	P	SHI Stop Condition

Note: Command symbols in bold are reserved and must be followed in exact order.

Table 8: Examples of Accessing through SHI

a. single memory write
S C0 W FC F3 3B *AH AL DH DL* **P**
Example: S C0 W FC F3 3B 1E 41 00 01 P -- writes 0x0001 to memory address 0x1E41

b. burst mode memory write
S C0 W XX XX **FC F3 3B** *AH AL DH DL* …… **FC F3 3B** *AH AL DH DL* **P**
Example: S C0 W 00 1C FC F3 3B 1E 30 00 02 FC F3 3B 1E 41 00 01 FC F3 3B 1E 51 D0 00 P
 -- writes 0x0002 to DM 0x1E30, 0x0001 to DM 0x1E41 and 0xD000 to DM 0x1E51 0x00 and
    0x1C between **W** and **FC** are dummy bytes, and ignored.

c. fast memory read
S C0 W FC F3 37 *AH AL* **P**
S C0 R RH RL **P**
Examples: S C0 W FC F3 37 1E 41 P -- read memory address 0x1E41
     S C0 R 00 01 P -- get value 0x0001.

4. Electrical and Timing Specification

* Note: All data in this section are measured at room temperture and in normal operating condition.

4.1 Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VDD_S	-	2.0	V
Digital Input Voltage	VIN	-	3.6	V
Digital Output Voltage	VOUT	-	3.6	V
Storage Temperature	T_{stg}	-	-40 to 150	^{0}C

4.2 Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ESD Protection		HBM			2	kV
Power Supply Voltage[1]	VDD_S	-	1.62	1.8	2.0	V

I/O Supply Voltage	VDD_D		1.62	1.8 or 3.3	3.6	V
Operating Temperature	T_{amb}	Extended Grade Auto Grade	-20 -40	25 25	70 85	°C
Input High Voltage	V_{IH}		VDD_D-0.3		VDD_D	V
Input Low Voltage	V_{IL}		0		0.3	V
Master Clock Frequency	f_{mck}	XTAL_IN		4.096, 13		MHz
Master Clock Duty Ratio	D_{mck}	XTAL_IN	40	50	60	%
Bit Clock Frequency	f_{bck}	BCLK (Master Mode)	128	256	1,024	kHz
Bit Clock Frequency	f_{bck}	BCLK (Slave Mode)	128	256	4,096	kHz
Bit Clock Duty Cycle	D_{bck}	BCLK	40	50	60	%
Sync Signal Frequency	f_{sync}	FSYNC		8		kHz

Notes: The power ripple (AC element) has to be limited within 100mV

4.3 DC Characteristics

Table 11: DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply for Core	V10		1.62	1.8	2.0	V
Power Supply Current	ISU	Operating, Analog + Digital	-	17	19	mA
Power Down Current	IPD	PWD_ is low	-	40*	-	µA
Input Leakage Current	IIH	VI = VDD_D	-	-	10	µA
	IIL	VI = 0 V	-	-	10	µA
High Level Digital Output Voltage	VOH	No Load	VDD_D	-		V
Low Level Digital Output Voltage	VOL	No Load		-	0	V
Digital Output Leakage Current	IO		-	-	10	µA
Input Capacitance	CIN		-	10	-	pF
Power Dissipation	PSYS	V10 =1.8V, Tamb=25°C	-	30.6	34.2	mW

Notes:
* I_{PD} is only for V10. VDD_D and VDD_S leakage current may be up to additional 20 µA.

4.4 AC Characteristics

Table 12: AC Characteristics (room temperature, gain set to 0 dB, VDD=1.8V)

Parameter	Condition	Min	Typ	Max	Unit
Mic0/1 to Digital Line Out Full Scale	Mic 0/1 @ 0dB PGA gain	2.2	2.4	2.6	Vpp
Line_in Input Range (differential)	Reference as 0dB full scale		2.4		Vpp
Digital Line in to Speaker Out Full Scale	Speaker Out @ 0dB PGA	2.2	2.4	2.6	Vpp
Line_out Full Scale Output	@ 0dB PGA gain;	1.1	1.2	1.3	Vpp
(single-ended)	@ 2dB PGA gain		1.5		Vpp
SNR for Digital Line_in to Speaker out Path	Line In and Speaker @ 0dB PGA with input off	72	77		dB
SNR for Analog Line_in to Speaker out Path	Speaker @ 0dB PGA with input off	72	77		dB
SNR for Mic0 & Mic1 to Digital Line_out Path	Mic0/1 PGA set to 0dB with input off	75	81		dB
SNR for Mic0 & Mic1 to Analog Line_out Path	Mic 0/1 and Line Out PGA set to 0dB with input off	68	72		dB
CODEC Sampling Frequency			8		kHz
Input Impedance for Mic/Line_in	Reference as 0dB full scale		27.5		kΩ
Load impedance for Line_out / Spk_out		600			Ω

Parameter	Condition	Min	Typ	Max	Unit
Gain Range	-	-2	-	26	dB
Step Size	Range: -2dB to 0dB	-	1	-	dB
Step Size	Range: 0dB to 26dB	-	2	-	dB
Step Size Error	Range: -2dB to 0dB	-0.5	-	0.5	dB
Step Size Error	Range: 0dB to 26dB	-1	-	1	dB

Notes:
* All input pins become high impedance in the power down mode.
* Please refer to the FM1188 Input High Pass Filter Design App Note for more information regarding use of the ADC PGA gain.

Table 13: DAC PGA (Line_out, Spk_out)

Parameter	Condition	Min	Typ	Max	Unit
Gain Range	-	-29	-	2	dB
Step Size	Range: -29dB to 2dB	-	1	-	dB
Step Size Error	Range: -29dB to 2dB	-0.5	-	0.5	dB

4.5 Timing Characteristics

Table 14: Timing Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-down to power-up time	t_{pda}	-	100	-	-	ms
Reset hold time			2*			ms
Set parameter timing after reset	t_{param}	-	10	-	-	ms

Parameter setting delay	t_{data}		-	70	-	ms
Speaker out delay after parameter setting	t_{spk}		-	75	-	ms
Bit clock frequency	f_{bclk}	Output Mode	128	256	1,024	kHz
FSYNC Setup Time	t_{fs}	-	-	100	-	ns
FSYNC Hold Time	t_{fh}	-	-	100	-	ns
PCM Input Setup Time	t_{ds}	-	-	100	-	ns
PCM Input Hold Time	t_{dh}	-	-	100	-	ns
Digital Output Delay Time	t_{dd}	Output Mode	-	-	100	ns
FSYNC Output Delay Time	t_{fd}	Output Mode	-	-	100	ns

* Please refer to Figure 18: Timing Chart of External Reset for more detail description on Reset hold time.
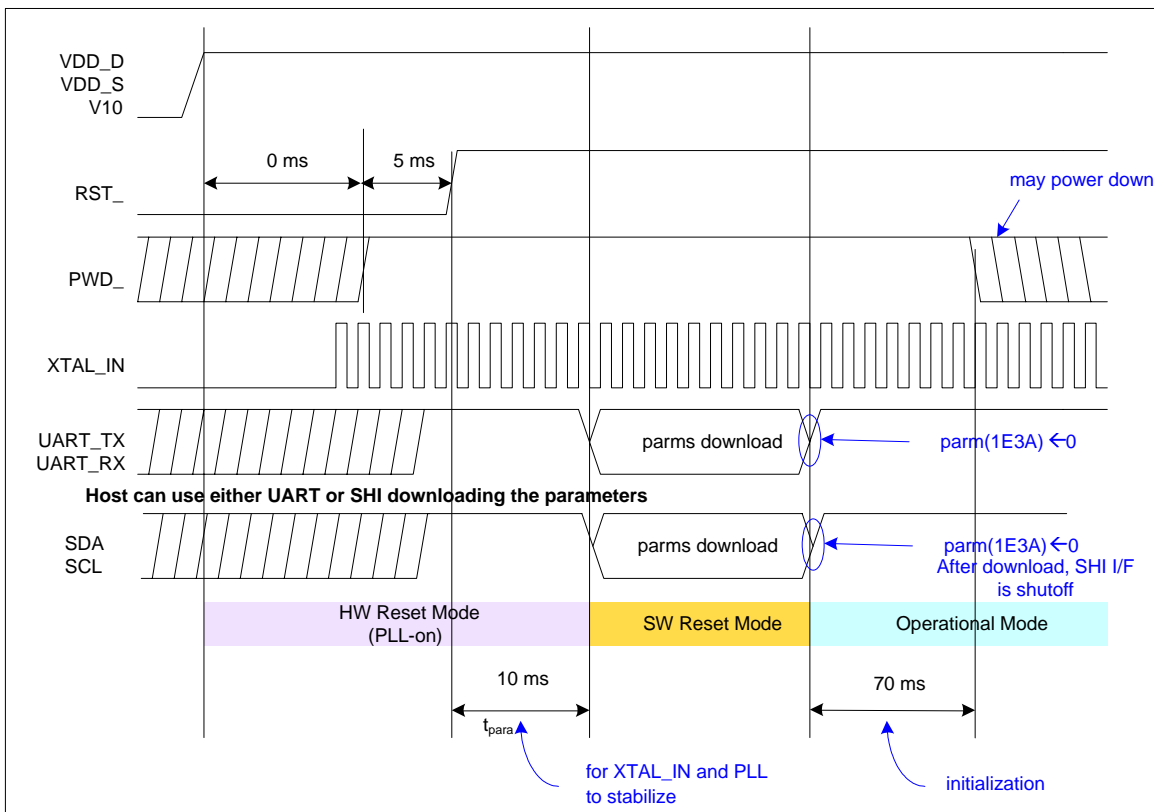
Figure 16: Timing Chart of State Transitions
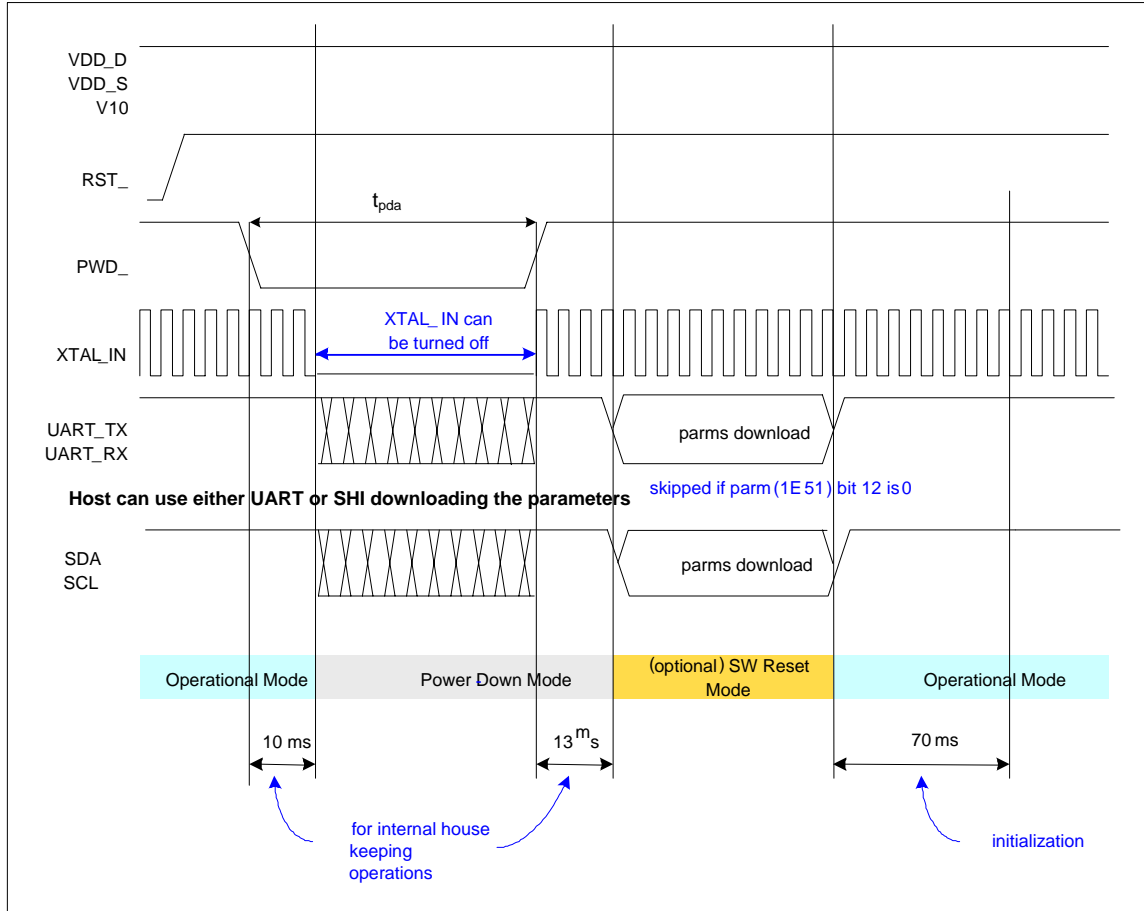
Figure 17: Timing Chart of Power-Down Transitions
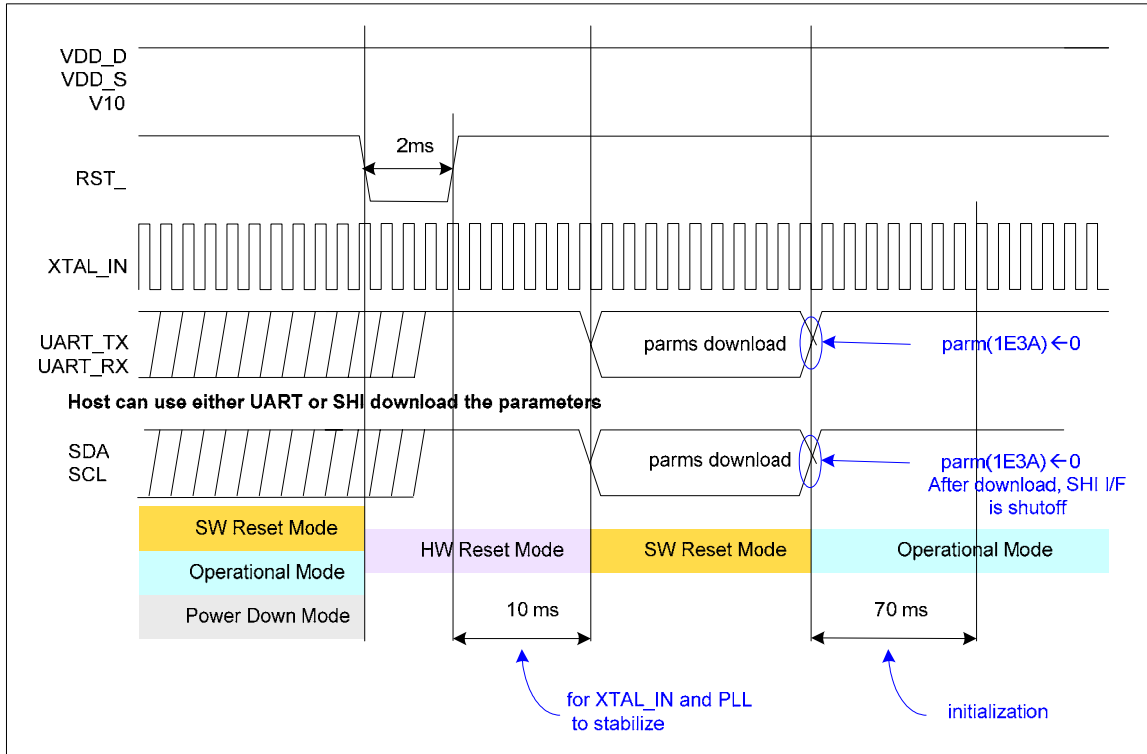
Figure 18: Timing Chart of External Reset
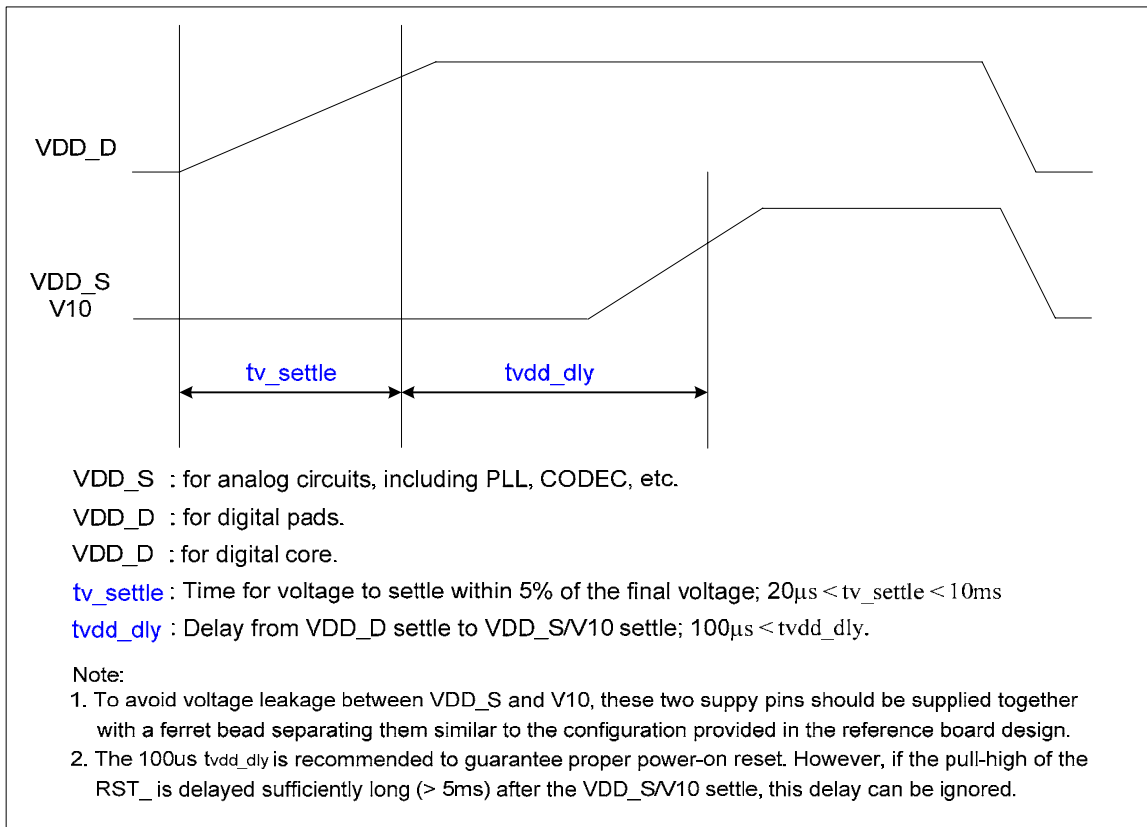
Figure 19: Timing Chart of Power On/Off Sequence

Figure 20: Serial Port Digital Input Timing (No clock delay)

Figure 21: Serial Port Digital Input Timing (One clock delay)
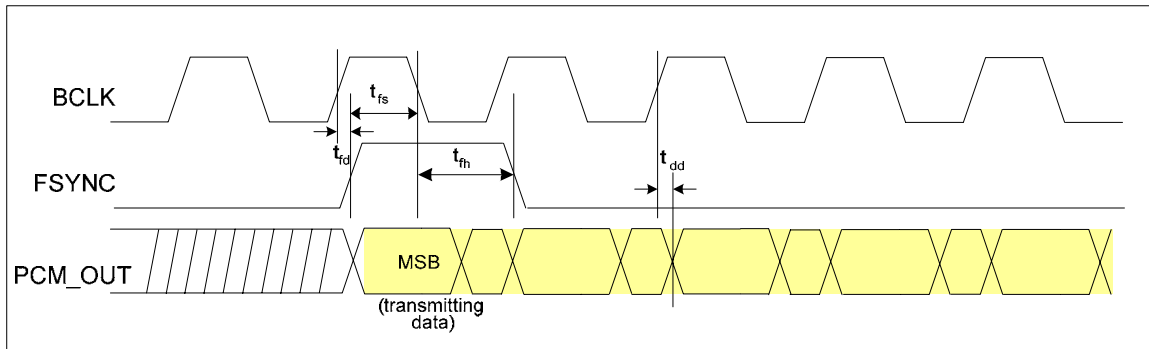
Figure 22: Serial Port Digital Output Timing (No clock delay)
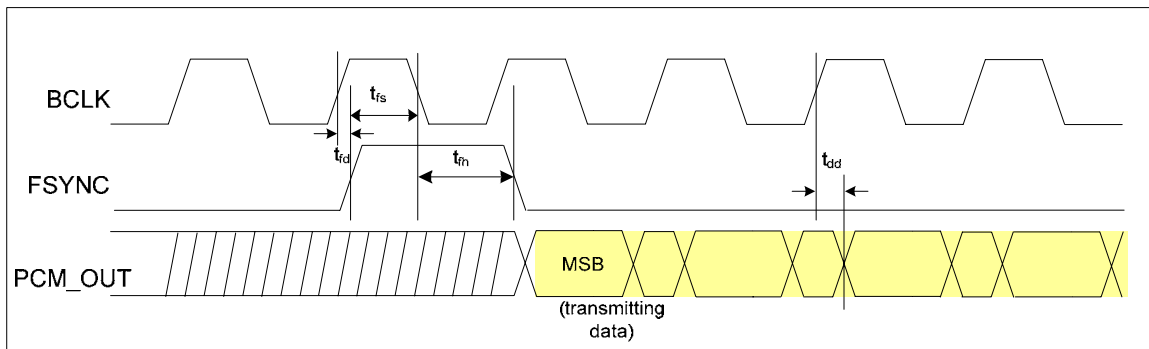
Figure 23: Serial Port Digital Output Timing (One clock delay)
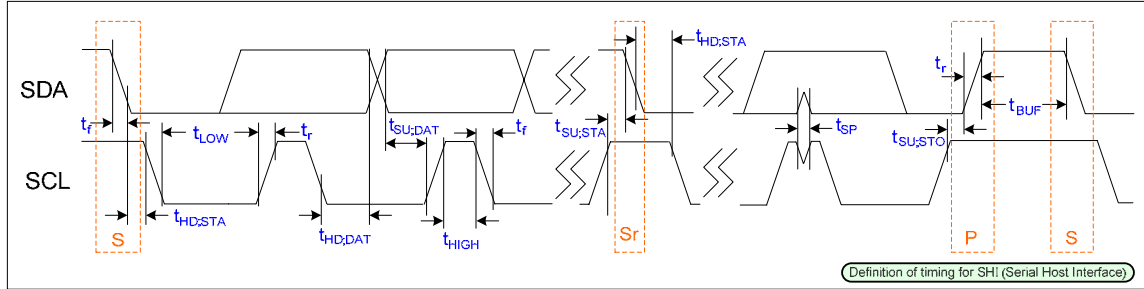
Figure 24: SHI bus (SDA and SCL) Timing Chart

Table 15: Timing Characteristics for SHI bus

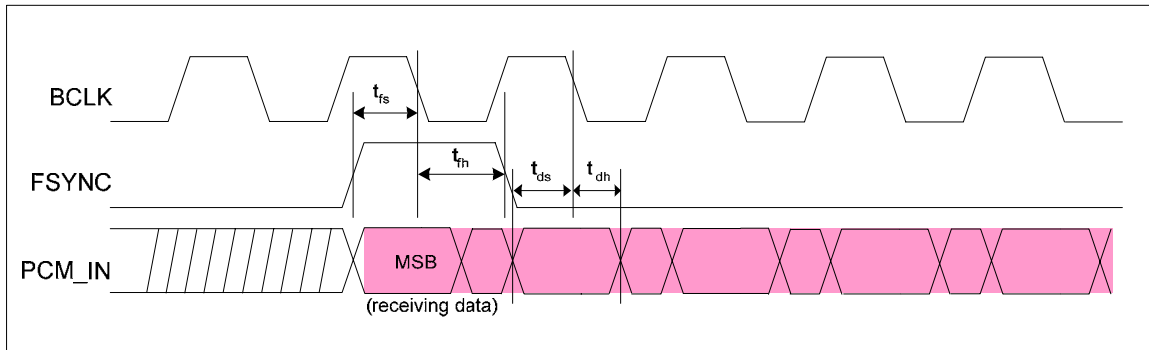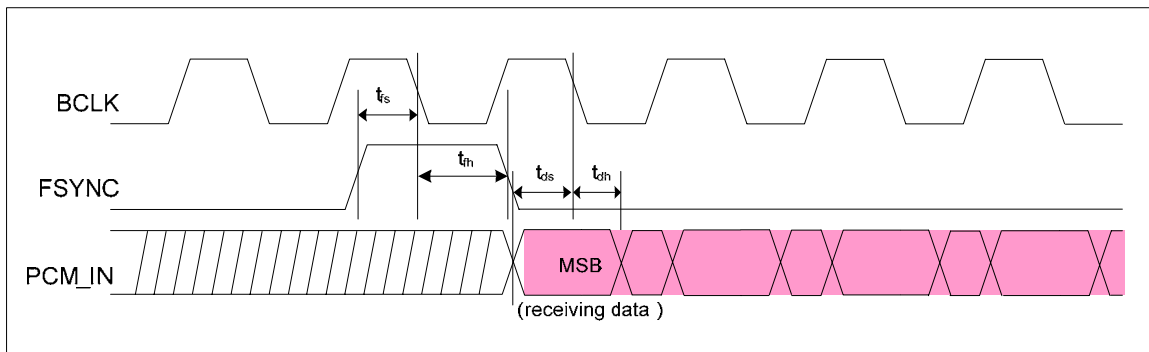| Parameter | Symbol | Standard-Mode | | UNIT |
		Min	Max	
SCL clock frequency	f_{SCL}	0	100	kHz
Hold time START condition.	$t_{HD;STA}$	4.0	-	μs
LOW period of the SCL clock	t_{LOW}	4.7	-	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	μs
Data hold time	$t_{HD;DAT}$	0	-	μs
Data set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	ns
Fall time of both SDA and SCL signals	t_f	-	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	μs

5. Voice Processor Performance Details

Table 16: Voice Processor Performance Details

Parameter	Condition	Min	Typ	Max	Unit
Acoustic Echo Cancellation	2-mic mode	-	-	65	dB
Stationary Noise Suppression	For Mic0, Mic1	-	12	-	dB
Non-stationary Noise Suppression	For Mic0 & Mic1 Beam-forming	-	20	-	dB
Beam-forming angle	U+O SAM beamforming*	-	120	-	º
Side Tone Cancellation	-	25	-	35	dB
Acoustic Echo Tail Length	-	-	-	100	ms
Sidetone Tail Length				8	ms
Echo Convergence	2-mic mode	-	40	-	ms
Non-stationary Noise Convergence	2-mic mode, beam-forming operating mode	-	200	-	ms
Stationary Noise Convergence	1-mic mode	-	3	-	s
Mic_in to Line_out Latency	-	-	54	-	ms

* Based on uni-directional microphone with 6dB difference between 0º and 60º.

6. Pin Definition

Table 17: Pin Description

QFP Pin #	BGA Ball #	Pin Name	I/O Type	PD Status[5]	Pin Description
1	E3	NC	NC	NC	No connect
2	G2	NC	NC	NC	No connect
3	G1	SPK_OUT_N	Out	Tri-State	Speaker output (-)
4	F3	NC	NC	NC	Not connect
5	G3	NC	NC	NC	Not connect
6	F4	NC	NC	NC	Not connect
7	E4	VSS_D	GND	GND	Digital ground
8	G4	BCLK	In/Out	In	BCLK signal for Serial Port
9	G5	FSYNC	In/Out	In	Frame sync signal for Serial Port
10	F5	PCM_OUT	In/Out	In	During power up, used as strap option (section 2.9); after power up, transmits voice data to Serial Port
11	G6	PCM_IN	In	In	Receive voice data from Serial Port
12	G7	UART_RX	In	In	Serial commands from UART port
13	F6	UART_TX	In/Out	In	During power up, used as strap option (section 2.9); after power up, transmits serial commands to UART port
14	E5	TEST2	In	In	For analog communications mode, which will bypass Voice Processor [1]
15	F7	SDA_EE	In/Out	In	Serial data access for EEPROM
16	E6	SCL_EE	In/Out	In	Serial clock for EEPROM
17	E7	GPIO7	In/Out	In	Mode select strap option (section 2.9)
18	D4	VSS_D	GND	GND	Digital ground
19	D7	VDD_D	VDD	VDD	I/O Supply Voltage[2]
20	D6	STRAP0	In/Out	In	During power up, used as strap option (section 2.10); not used during normal operation
21	C7	MUTE_OUT	In/Out	In	During power up, used as strap option (section 2.9); after power up, serves as output LED to indicate microphone "mute" status
22	D5	VAD_LED	In/Out	In	Must pull low using weak 100kΩ resistor to select XTAL_IN as PLL clock source; after power up, serves as LED output to indicate internal status for VAD (Voice Activity Detection) tuning
23	B7	SCL	In/Out	In	Serial clock for SHI interface, if selected; if SHI is not selected, serves as input pin to select "earpiece" mode where the speaker output gain will be reduced to support earpiece function [3] ; if not

					used, pull high using weak 100kΩ resistor to be in speaker-phone mode
24	C6	SDA/MUTE_IN	In/Out	In	Serial data access for SHI interface, if selected; if SHI is not selected, serves as input pin to select "mute" function on the microphone [4] ; if not used, pull low using weak 100kΩ resistor
25	A7	Vol-	In/Out	In	Volume Down input pin (level triggered, active high); if not used, pull low using weak 100kΩ resistor
26	B6	Vol+	In/Out	In	Volume Up input pin (level triggered, active high); if not used, pull low using weak 100kΩ resistor
27	A6	XTAL_IN	In	In	Crystal input. The logic level depends on the voltage level of V10 (ranged from 1.62V to 2.0V). The maximum V_{IL} is 0.3V, and the minimum V_{IH} is V10-0.3V.
28	A5	XTAL_OUT	Out	Out	Crystal output
29	C5	GND_D	GND	GND	Digital ground
30	B5	PWD_	In	In	Powerdown pin, edge trigger from high to low. Active low
31	A4	RST_	In	In	Reset pin, active low
32	C4	TEST1	In	In	Connect a 100kΩ resistor to ground
33	A3	V10	VDD	VDD	Power supply for digital core connect a 1μF capacitor to ground and connect a ferrite bead to VDD_S
34	B4	NC	NC	NC	No Connect
35	A2	VDD_S	VDD	VDD	Analog power supply
36	B3	NC	NC	NC	No Connect
37	A1	VREF	VDD	Tri-state	Connect a 1μF capacitor to ground
38	C3	VSS_A	GND	GND	Analog Ground for CODEC
39	B1	MIC0_P	In	In	Mic0 (+) input
40	B2	MIC0_N	In	In	Mic0 (-) input
41	C1	MIC1_P	In	In	Mic1 (+) input
42	C2	MIC1_N	In	In	Mic1 (-) input
43	D1	LINE_IN_P	In	In	Line_in (+) input
44	D2	LINE_IN_N	In	In	Line_in (-) input
45	E1	VSS_REF	GND	GND	Connect to ground
46	E2	BG_REF	In/Out	Tri-state	Connect a 1μF capacitor to ground
47	F1	LINE_OUT	Out	Tri-state	Analog output
48	F2	SPK_OUT_P	Out	Tri-state	Speaker output (+)
n/a	D3	NC	NC	NC	No Connect

Notes:
(1)   Active high: when Test 2 is "high", Voice Processor will be in idle state and Voice Processor will restart on high to low transition.
(2)   This separate voltage source is designed to adapt to the level of the digital interface voltage level; it can either be 1.8V or 3.3V, depending on the interface logic level

(3)   Edge triggered: falling edge to "earpiece" mode and rising edge to "speaker" mode
(4)   Level triggered with active high, and it will toggle between "mute" and "not mute"; the default after reset is always "not mute".
(5)   PD Status = Powerdown Status

7. Package Dimensions (LQFP & BGA)

BGA Top and Side View
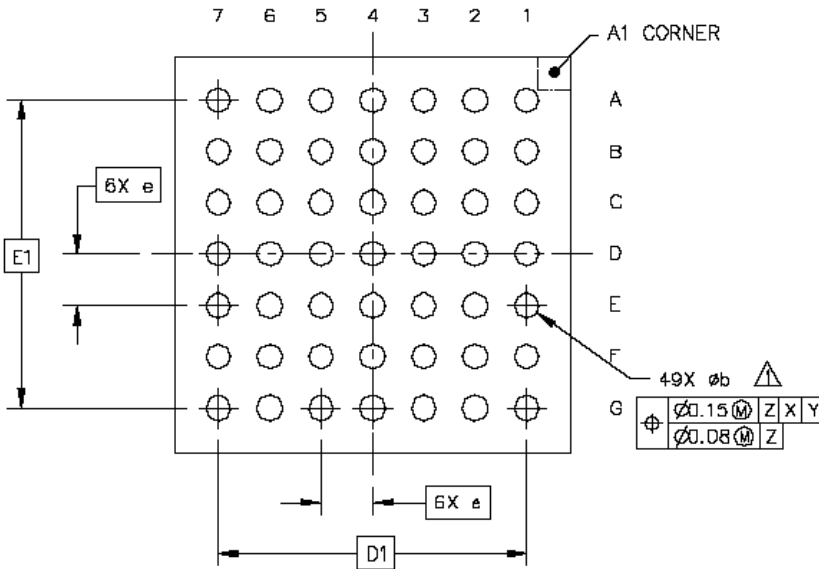
Wafer lot code
X: internal

Date code:
D: internal
S: engineering sample

BGA-48 pin Top View

FM1188-BE
XXXXX.XX
DDDDS

A1 Corner

B: BGA

E: Extended Grade
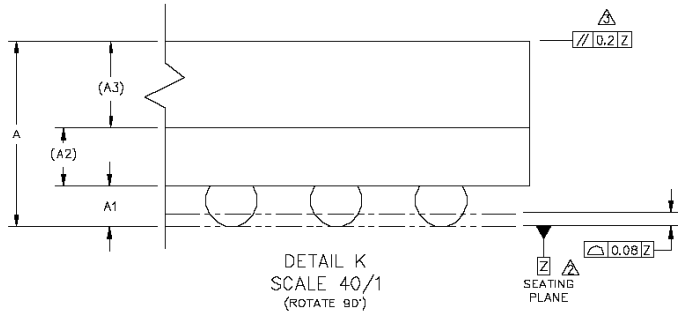
DETAIL K

BGA Bottom View

Note: The third line of the package marking contains date code. "Y" indicates the year and WW indicates the week of the year.

BGA Side View

DETAIL K
SCALE 40/1
(ROTATE 90°)

SEATING PLANE

DIM	MIN.	NOR.	MAX.	NOTES
A	---		1.2	⚠1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
A1	0.16		0.26	
A2		0.36 REF		⚠2 DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
A3		0.54 REF		
b	0.27		0.37	⚠3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
D		5 BSC		
E		5 BSC		
e		0.65 BSC		
D1		3.9 BSC		
E1		3.9 BSC		

UNIT	DIMENSION AND TOLERANCES	
MM	ASME Y14.5M	

Figure 25: 48-pin BGA Package Drawing and Dimensions

48 Pin LQFP Package Outline

LQFP: 7x7x1.4 mm

LQFP Top View

Wafer lot code
X: internal

Date code:
D: internal
S: engineering sample

G: LQFP

E: Extended Grade

fortémedia
FM1188-GE
XXXXX.XX
DDDDS

LQFP- 48 pin Top View

Pin 1

LQFP Side View

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.15	0.002	0.006
A2 (LQFP)	1.35	1.45	0.053	0.057
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
e	0.50 TYP		0.02 TYP	
L	0.45	0.75	0.018	0.030
HD/HE	8.80	9.20	0.346	0.362
D/E	6.90	7.10	0.272	0.280

Note: The third line of the package marking contains date code. "Y" indicates the year and WW indicates the week of the year.

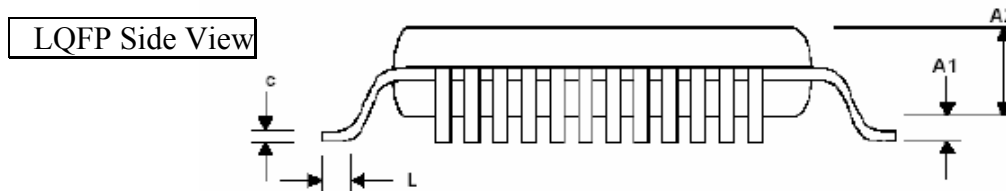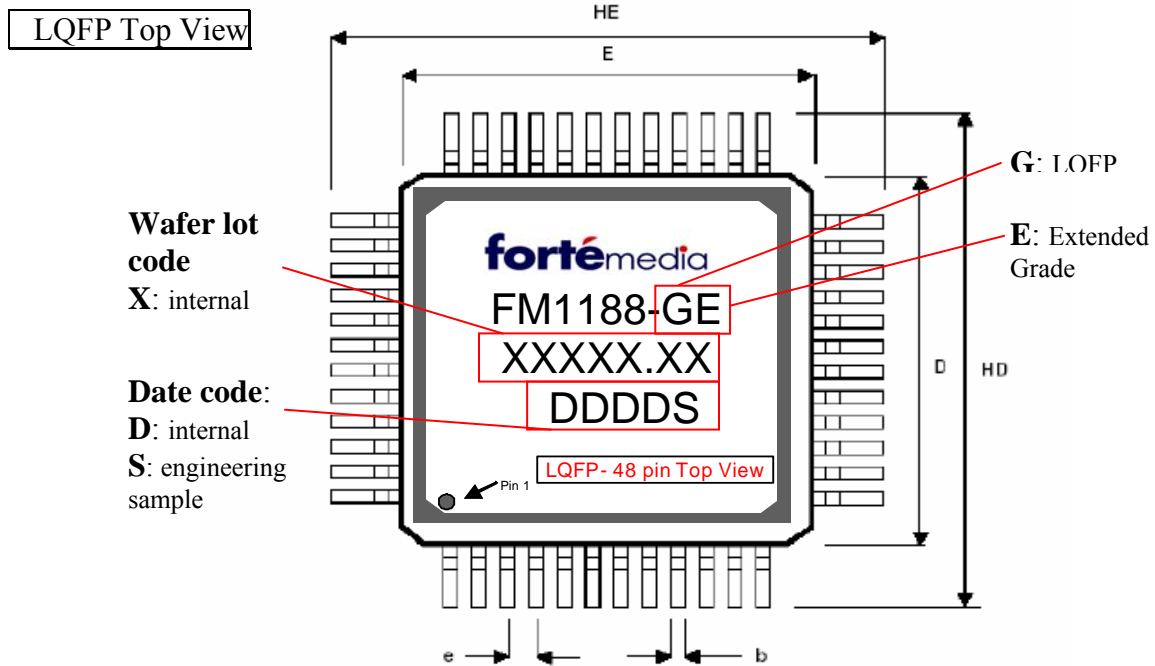**Figure 26: 48-pin LQFP Package Drawing and Dimensions**

8. Ordering Information

Table 18: Available Packages and Temperature Grade

Package	Green	Temperature Grade	Ordering Code
48-pin LQFP	Yes	Extended	FM1188-GE
48-pin BGA	Yes	Extended	FM1188-BE
48-pin LQFP	Yes	Auto	FM1188-GA1

Note: Consumer = 0 to 70º C
            Extended = -20 to 70ºC
            Auto = -40 to 85ºC

Appendix I: Required External Components for Operation

**Table 19: External Components Recommendations**

Microphone Specification

Parameter	Value
Type	Electret Condenser Microphone
Sensitivity	-44 ~ -47 dB (1V/PA)
Operating Voltage	2V (standard)
Impedance	2.2kΩ maximum

External Speaker/Headphone Driver

Amplifier with 20kΩ input impedance is preferred

Crystal/Oscillator Specification

Parameter	Value
Table Operating Frequency	4.096 MHz or 13 MHz
Resonant Mode	Parallel
Frequency Tolerance	+/- 30ppm
Aging per Year	+/- 5ppm / yr
Operating Mode	Fundamental Mode
Crystal Co	< 10 pF
Crystal Rs (ESR)	< 150 Ω
R_S (external)	330 Ω
CL (external load capacitance)	16 pF
Drive Level	500 µW
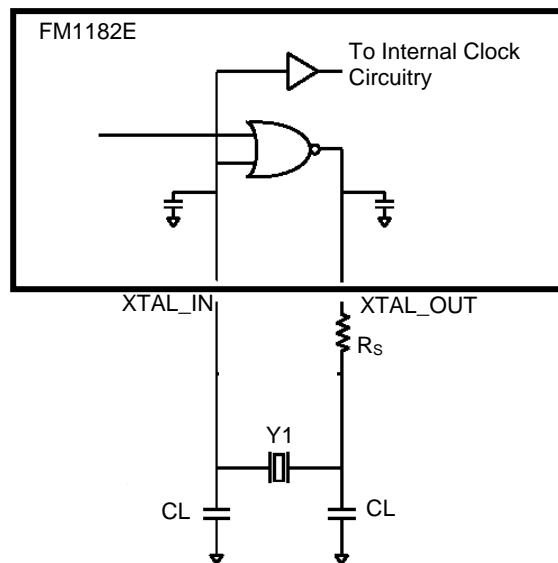
Figure 27 External XTAL_IN Clock Source

Serial EEPROM (optional)
Fortemedia recommends using a 1.8V serial EEPROM such as 24AA02 (256 bytes – small size) or 24AA08 (1Kbytes – large size).
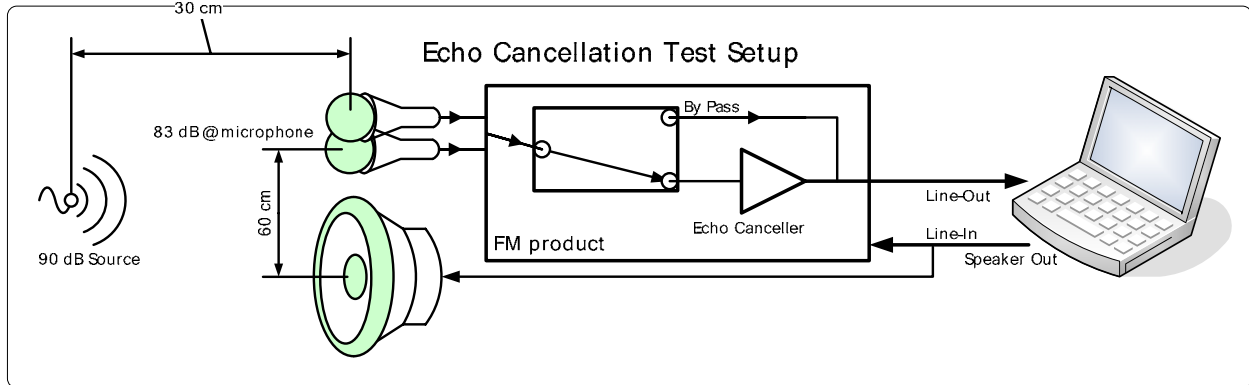
Appendix II: Audio Measurement System

Settings
PC microphone: -45dB sensitivity
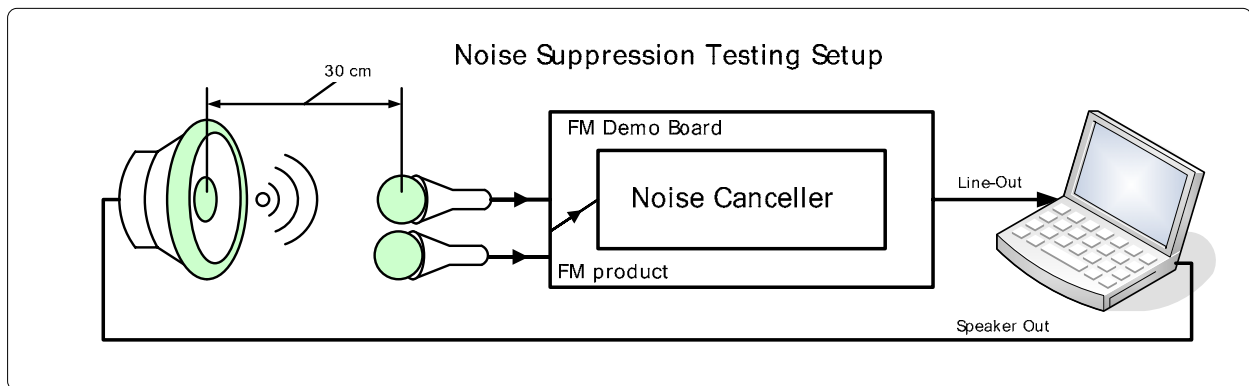Speaker: 8W

Table 20: Echo Cancellation Measurement

Parameter	Condition	Typical
Acoustic Echo Cancellation	Voice band	50 to 65dB

Figure 28: Echo Cancellation Test Setup

Table 21: Noise Suppression Measurement

Parameter	Condition	Typical
Stationary Noise Suppression	Pink noise and car noise	12dB

Figure 29: Noise Suppression Test Setup

References

I. Terminology

Table 22: Terminology

Term	Definition
ADC	Analog to Digital
AEC	Acoustic echo-cancellation
DAC	Digital to Analog
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read-Only Memory
HFCK	Hands Free Car Kit
FM	Fortemedia Inc.
MIC	Microphone
MIPS	Million instruction per second
NC	Not Connected
Omni	Omni-directional microphone
PCM	Pulse Code Modulation
PGA	Programmable Gain Amplification
PM	Program Memory
PND	Portable Navigation Device
ROM	Read Only Memory
SHI	Serial Host Interface
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/ Transmitter
Uni	Unidirectional Microphone

II. Related Documents

Table 23: Related Documents

Fortemedia Technology Documents	Document Location
FM1182 SHI Implementation	Contact Fortemedia Sales
FM1188 Parameter Tuning Guide	Contact Fortemedia Sales