FM25H20

2Mb Serial 3V F-RAM Memory

Features

2M bit Ferroelectric Nonvolatile RAM
- Organized as 256K x 8 bits
- High Endurance 100 Trillion (10^{14}) Read/Writes
- 10 Year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Very Fast Serial Peripheral Interface - SPI
- Up to 40 MHz Frequency
- Direct Hardware Replacement for Serial Flash
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)

Write Protection Scheme
- Hardware Protection
- Software Protection

Low Power Consumption
- Low Voltage Operation 2.7V – 3.6V
- Sleep Mode Current 3 µA (typ.)

Industry Standard Configurations
- Industrial Temperature -40°C to +85°C
- 8-pin "Green"/RoHS TDFN Package
- 8- pin "Green"/RoHS EIAJ SOIC Package

Description

The FM25H20 is a 2-megabit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes like a RAM. It provides reliable data retention for 10 years while eliminating the complexities, overhead, and system level reliability problems caused by Serial Flash and other nonvolatile memories.

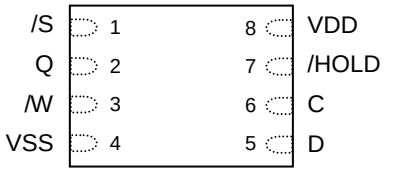
Unlike Serial Flash, the FM25H20 performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after it has been transferred to the device. The next bus cycle may commence without the need for data polling. The product offers virtually unlimited write endurance, orders of magnitude more endurance than Serial Flash. Also, F-RAM exhibits lower power consumption than Serial Flash.

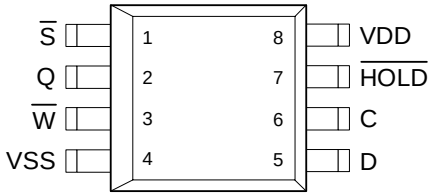
These capabilities make the FM25H20 ideal for nonvolatile memory applications requiring frequent or rapid writes or low power operation. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of Serial Flash can cause data loss.

The FM25H20 provides substantial benefits to users of Serial Flash as a hardware drop-in replacement. The FM25H20 uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. Device specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration

Top View





Pinout is equivalent to other SPI F-RAM devices.

Pin Name	Function
/S	Chip Select
/W	Write Protect
/HOLD	Hold
C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
VDD	Supply Voltage (2.7 to 3.6V)
VSS	Ground

Ordering Information	
FM25H20-DG	8-pin "Green"/RoHS TDFN
FM25H20-DGTR	8-pin "Green"/RoHS TDFN, Tape & Reel
FM25H20-G	8-pin "Green"/RoHS EIAJ SOIC
FM25H20-GTR	8-pin "Green"/RoHS EIAJ SOIC, Tape & Reel

This is a product in the pre-production phase of development. Device characterization is complete and Ramtron does not expect to change the specifications. Ramtron will issue a Product Change Notice if any specification changes are made.

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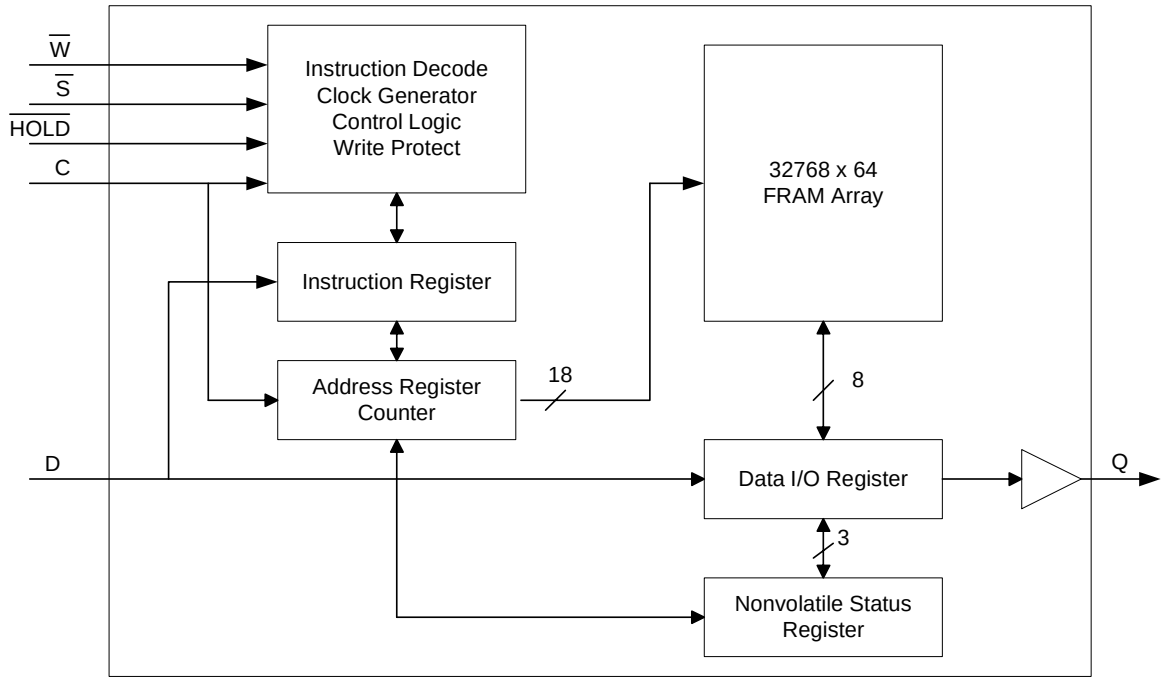


Figure 1. Block Diagram

Pin Descriptions

Pin Name	I/O	Description
/S	Input	Chip Select: This active low input activates the device. When high, the device enters low-power standby mode, ignores other inputs, and all outputs are tri-stated. When low, the device internally activates the C signal. A falling edge on /S must occur prior to every op-code.
C	Input	Serial Clock: All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Since the device is static, the clock frequency may be any value between 0 and 40 MHz and may be interrupted at any time.
/HOLD	Input	Hold: The /HOLD pin is used when the host CPU must interrupt a memory operation for another task. When /HOLD is low, the current operation is suspended. The device ignores any transition on C or /S. All transitions on /HOLD must occur while C is low.
/W	Input	Write Protect: This active low pin prevents write operations only to the Status Register. A complete explanation of write protection is provided on pages 6 and 7.
D	Input	Serial Input: All data is input to the device on this pin. The pin is sampled on the rising edge of C and is ignored at other times. It should always be driven to a valid logic level to meet I_{DD} specifications. * D may be connected to Q for a single pin data interface.
Q	Output	Serial Output: This is the data output pin. It is driven during a read and remains tri-stated at all other times including when /HOLD is low. Data transitions are driven on the falling edge of the serial clock. * Q may be connected to D for a single pin data interface.
VDD	Supply	Power Supply (2.7V to 3.6V)
VSS	Supply	Ground

Overview

The FM25H20 is a serial F-RAM memory. The memory array is logically organized as 262,144 x 8 and is accessed using an industry standard Serial Peripheral Interface or SPI bus. Functional operation of the F-RAM is similar to Serial Flash. The major differences between the FM25H20 and a Serial Flash with the same pinout are the F-RAM's superior write performance, very high endurance, and lower power consumption.

Memory Architecture

When accessing the FM25H20, the user addresses 256K locations of 8 data bits each. These data bits are shifted serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an op-code, and a three-byte address. The complete address of 18-bits specifies each byte address uniquely.

Most functions of the FM25H20 either are controlled by the SPI interface or are handled automatically by on-board circuitry. The access time for memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike Serial Flash, it is not necessary to poll the device for a ready condition since writes occur at bus speed. So, by the time a new bus transaction can be shifted into the device, a write operation will be complete. This is explained in more detail in the interface section.

Users expect several obvious system benefits from the FM25H20 due to its fast write cycle and high endurance as compared to Serial Flash. In addition there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than Serial Flash since it is completed quickly. By contrast, Serial Flash requiring milliseconds to write is vulnerable to noise during much of the cycle.

Serial Peripheral Interface – SPI Bus

The FM25H20 employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 40MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25H20 operates in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. A typical system configuration uses one or more FM25H20 devices with a microcontroller that has a dedicated SPI port, as Figure 2 illustrates. Note that the clock, data-in, and data-out pins are common among all devices. The Chip Select and Hold pins must be driven separately for each FM25H20 device.

For a microcontroller that has no dedicated SPI bus, a general purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins together and tie off the Hold pin. Figure 3 shows a configuration that uses only three pins.

Protocol Overview

The SPI interface is a synchronous serial interface using clock and data pins. It is intended to support multiple devices on the bus. Each device is activated using a chip select. Once chip select is activated by the bus master, the FM25H20 will begin monitoring the clock and data lines. The relationship between the falling edge of /S, the clock and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM25H20 supports only modes 0 and 3. Figure 4 shows the required signal relationships for modes 0 and 3. For both modes, data is clocked into the FM25H20 on the rising edge of C and data is expected on the first rising edge after /S goes active. If the clock starts from a high state, it will fall prior to the first data transfer in order to create the first rising edge.

The SPI protocol is controlled by op-codes. These op-codes specify the commands to the device. After /S is activated the first byte transferred from the bus master is the op-code. Following the op-code, any addresses and data are then transferred.

Certain op-codes are commands with no subsequent data transfer. The /S must go inactive after an operation is complete and before a new op-code can be issued. There is one valid op-code only per active chip select.

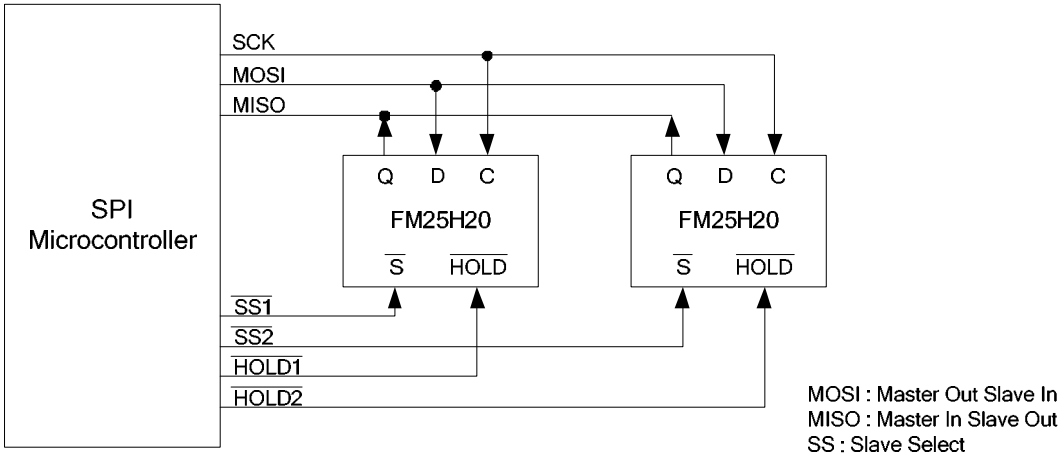


Figure 2. 512KB System Configuration with SPI port

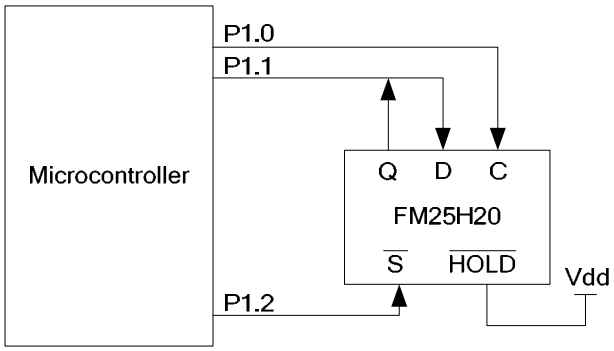
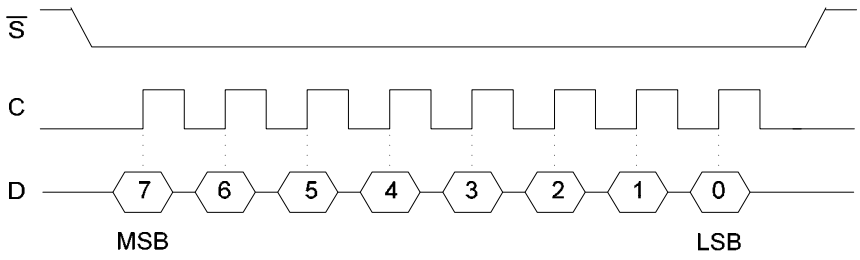


Figure 3. System Configuration without SPI port

SPI Mode 0: CPOL=0, CPHA=0



SPI Mode 3: CPOL=1, CPHA=1

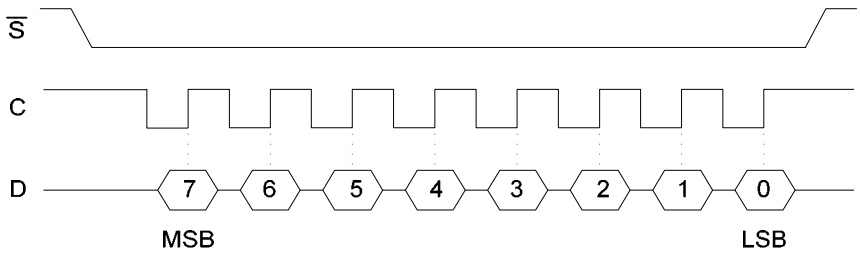


Figure 4. SPI Modes 0 & 3

Power Up to First Access

The FM25H20 is not accessible for a period of time (1 ms) after power up. Users must comply with the timing parameter t_{PU}, which is the minimum time from V_{DD} (min) to the first /S low.

Data Transfer

All data transfers to and from the FM25H20 occur in 8-bit groups. They are synchronized to the clock signal (C), and they transfer most significant bit (MSB) first. Serial inputs are registered on the rising edge of C. Outputs are driven from the falling edge of C.

Command Structure

There are six commands called op-codes that can be issued by the bus master to the FM25H20. They are listed in the table below. These op-codes control the functions performed by the memory. They can be divided into three categories. First, there are commands that have no subsequent operations. They perform a single function such as to enable a write operation. Second are commands followed by one byte, either in or out. They operate on the Status Register. The third group includes commands for memory transactions followed by address and one or more bytes of data.

Table 1. Op-code Commands

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110b
WRDI	Write Disable	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read Memory Data	0000 0011b
WRITE	Write Memory Data	0000 0010b
SLEEP	Enter Sleep Mode	1011 1001b

WREN - Set Write Enable Latch

The FM25H20 will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the Status Register (WRSR) and writing the memory (WRITE).

Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit – only the WREN op-code can set this bit. The WEL bit will be automatically cleared on the rising edge of /S following a WRDI, a WRSR, or a WRITE operation. This prevents further writes to the Status Register or the F-RAM array without another WREN command. Figure 5 below illustrates the WREN command bus configuration.

WRDI - Write Disable

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the Status Register and verifying that WEL=0. Figure 6 illustrates the WRDI command bus configuration.

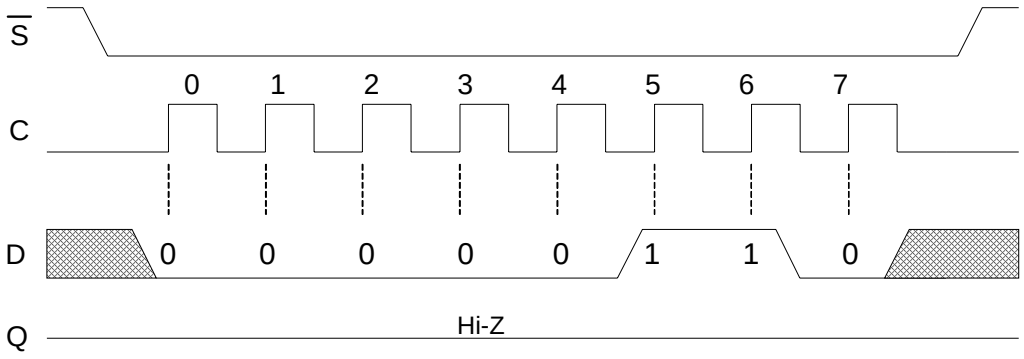


Figure 5. WREN Bus Configuration

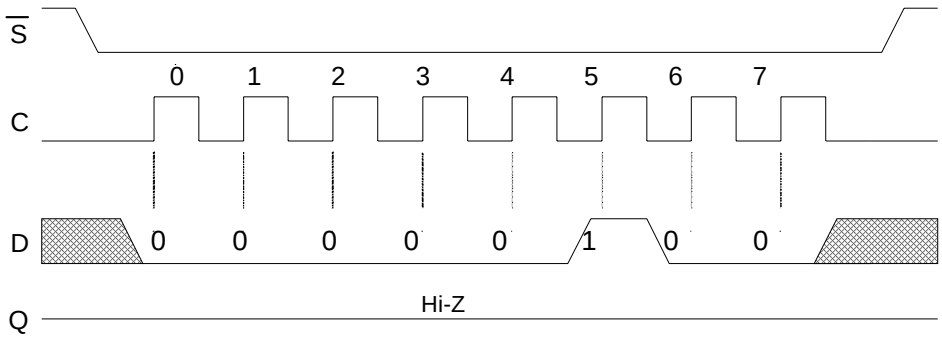


Figure 6. WRDI Bus Configuration

RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading Status provides information about the current state of the write protection features. Following the RDSR op-code, the FM25H20 will return one byte with the contents of the Status Register. The Status Register is described in detail in the section below.

WRSR – Write Status Register

The WRSR command allows the user to select certain write protection features by writing a byte to the Status Register. Prior to issuing a WRSR command, the /W pin must be high or inactive. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch. The bus configuration of RDSR and WRSR are shown below.

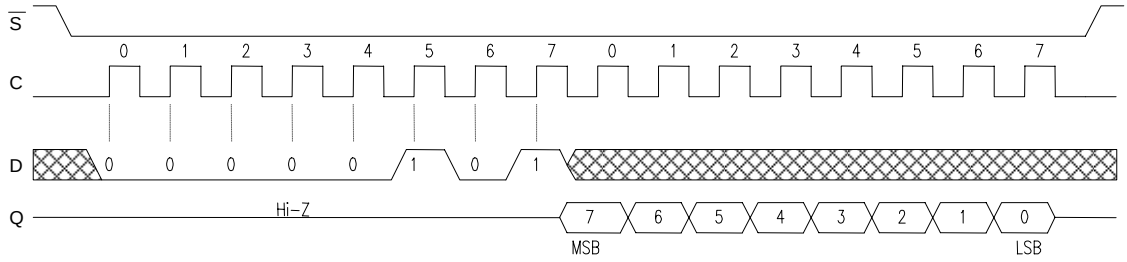


Figure 7. RDSR Bus Configuration

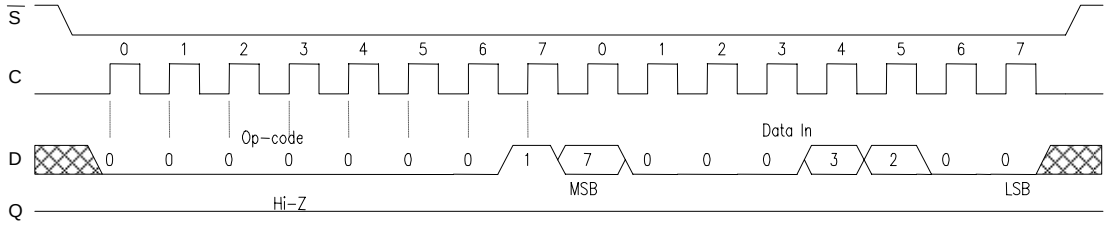


Figure 8. WRSR Bus Configuration

Status Register & Write Protection

The write protection features of the FM25H20 are multi-tiered. A WREN op-code must be issued prior to writing the memory (WRITE) or Status Register (WRSR). Protecting the Status Register can be accomplished via software using the WPEN bit or hardware using the /W pin. Status Register write operations are blocked when the /W pin is low and WPEN=1. Memory write operations are protected by the block protect (BP) bits in the Status Register. The state of the /W pin has no effect on memory writes. As described above, writes to the Status Register are performed using the WRSR command and subject to the WPEN bit and /W pin. The Status Register is organized as follows.

Table 2. Status Register

Bit	7	6	5	4	3	2	1	0
Name	WPEN	1	0	0	BP1	BP0	WEL	0

Bits 0, 4, 5 are fixed at 0 and bit 6 is fixed at 1, and none of these bits can be modified. Note that bit 0 ("Write in Progress" bit in Serial Flash) is unnecessary as the F-RAM writes in real-time and is never busy, so it reads out as a '0'. There is an exception to this when the device is waking up from Sleep Mode, which is described on the following page. The BP1 and BP0 control software write protection features. They are nonvolatile (shaded yellow). The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in the following table.

Table 3. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	30000h to 3FFFFh (upper ¼)
1	0	20000h to 3FFFFh (upper ½)
1	1	00000h to 3FFFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The WPEN bit controls the effect of the hardware pin /W. When WPEN=0, the /W pin is ignored. When WPEN=1, the /W pin controls write access to the Status Register. Thus the Status Register is write-protected only when WPEN=1 and the /W pin is low.

This scheme provides a write protection mechanism which can prevent software from writing the memory under any circumstances. This occurs if the BP1 and BP0 are set to 1, the WPEN bit is set to 1, and the /W pin is low. This occurs because the block protect bits prevent writing memory and the /W signal in hardware prevents altering the block protect bits (if WPEN is high). Therefore in this condition, hardware must be involved in allowing a write operation. The following table summarizes the write protection conditions.

Table 4. Write Protection

WEL	WPEN	/W	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Memory Operation

The SPI interface, which is capable of a relatively high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike Serial Flash, the FM25H20 can perform sequential writes at bus speed. No page buffer is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory array begin with a WREN op-code. The next op-code is the WRITE instruction. This op-code is followed by a three-byte address value, which specifies the 18-bit address of the first data byte of the write operation. Note that the first 6-bits in the most significant address byte are ignored. Subsequent bytes are data and they are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 3FFFFh is reached, the counter will roll over to 00000h. Data is written MSB first. A write operation is shown in Figure 9.

Unlike Serial Flash, any number of bytes can be written sequentially and each byte is written to memory immediately after it is clocked in (after the 8th clock). The rising edge of /S terminates a WRITE op-code operation. Asserting /W active in the middle of a write operation will have no effect until the next falling edge of /S.

Read Operation

After the falling edge of /S, the bus master can issue a READ op-code. Following this instruction is a three-byte address value, 18-bits specifying the address of the first data byte of the read operation. After the op-code and address are complete, the D line is ignored. The bus master issues 8 clocks, with one bit read out for each. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 3FFFFh is reached, the counter will roll over to 00000h. Data is read MSB first. The rising edge of /S terminates a READ op-code operation. A read operation is shown in Figure 10.

Hold

The /HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master pulls the /HOLD pin low while C is low, the current operation will pause. Taking the /HOLD pin high while C is low will resume an operation. The transitions of /HOLD must occur while C is low, but the C and /S pins can toggle during a hold state.

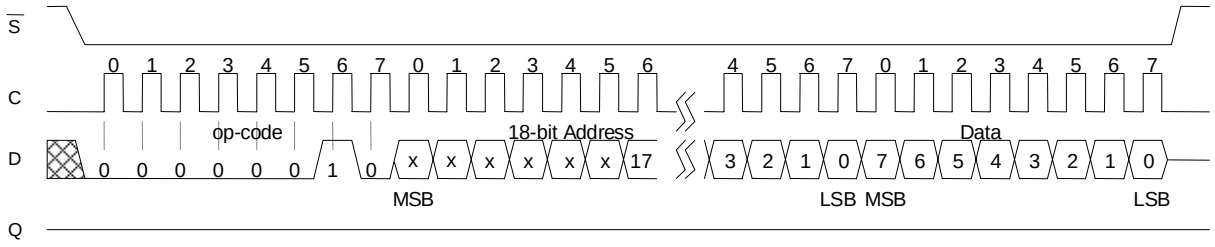


Figure 9. Memory Write

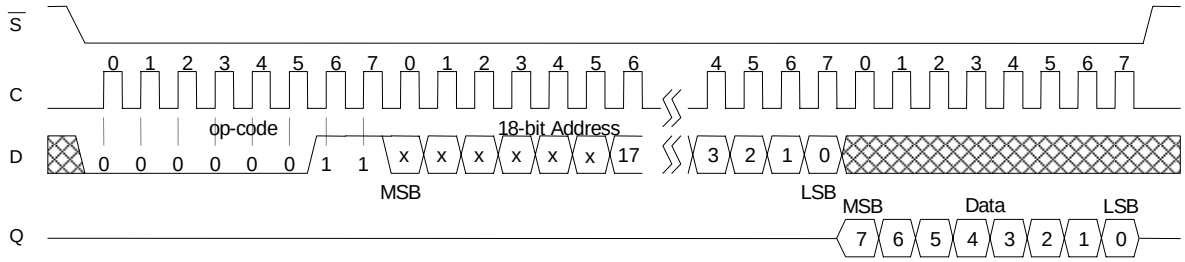


Figure 10. Memory Read

Sleep Mode

A low power mode called Sleep Mode is implemented on the FM25H20. The device will enter this low power state when the SLEEP op-code (B9h) is clocked in, and the device seeing the rising edge of /S. Once in sleep mode, the C and D pins are ignored and Q will go to a hi-Z state, but the device continues to monitor the /S pin. On the next falling edge of /S, the device will return to normal operation within t_{REC} (450 µs max.). The Q pin remains in a hi-Z state during the wakeup period. The FM25H20 will not necessarily respond to an opcode within the wakeup period. To start the wakeup procedure, the controller may send a "dummy" read, for example, and wait the remaining t_{REC} time.

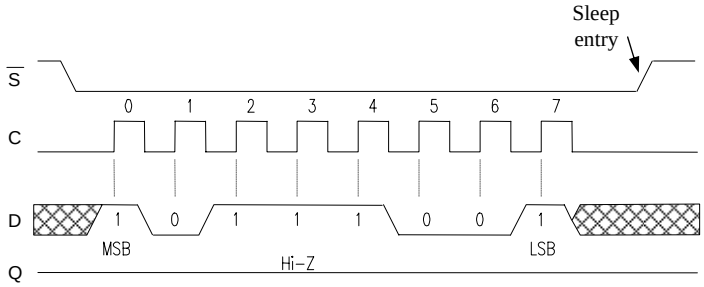


Figure 11. Sleep Mode Entry

Endurance

The FM25H20 is capable of being accessed at least 10^{14} times, reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis for each access (read or write) to the memory array. The F-RAM architecture is based on an array of rows and columns. Rows are defined by A17-A3 and column addresses by A2-A0. See Block Diagram (pg 2) which shows the array as 32K rows of 64-bits each. The entire row is internally accessed each time a byte in that row is read or written. All 8 bytes in the row are counted separately for each access in an endurance calculation. The table below shows endurance calculations for 256-byte repeating loop, which includes an op-code, a starting address (3 bytes), and a sequential 256-byte data stream. This causes each byte to experience eight endurance cycles through the loop. F-RAM read and write endurance is very high even at 40MHz clock rate.

Table 5. Time to Reach 100 Trillion Cycles for Repeating 256-byte Loop

SCK Freq (MHz)	Endurance Cycles/sec.	Endurance Cycles/year	Years to Reach 10^{14} Cycles
40	153,848	4.85×10^{12}	20.6
20	76,924	2.43×10^{12}	41.2
10	38,462	1.21×10^{12}	82.4
5	19,231	6.06×10^{11}	164.8

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +4.5V
V_{IN}	Voltage on any pin with respect to V_{SS}	-1.0V to +4.5V and $V_{IN} < V_{DD}$+1.0V
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (AEC-Q100-002 Rev. D) - Charged Device Model (AEC-Q100-011 Rev. B) - Machine Model (AEC-Q100-003 Rev. E)	 2kV 1kV 200V
	Package Moisture Sensitivity Level	MSL-1 (TDFN) MSL-1 (EIAJ)

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40°C to + 85°C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply Voltage	2.7	3.3	3.6	V	
I_{DD}	Power Supply Current @ C = 1 MHz @ C = 40 MHz		 - -	 1.0 10.0	 mA mA	1
I_{SB}	Standby Current @ T_A = 25°C @ T_A = 85°C		 80 -	 150 270	 µA µA	2
I_{ZZ}	Sleep Mode Current @ T_A = 25°C @ T_A = 85°C		 3 -	 5 8	 µA µA	3
I_{LI}	Input Leakage Current	-		±1	µA	4
I_{LO}	Output Leakage Current	-		±1	µA	4
V_{IL}	Input Low Voltage	-0.4		0.3 V_{DD}	V	
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage @ I_{OL} = 1.6 mA	 -		 0.4	 V	
V_{OH}	Output High Voltage @ I_{OH} = -100 µA	 V_{DD} – 0.2		 -	 V	

Notes

1. C toggling between V_{DD}-0.2V and V_{SS}, other inputs V_{SS} or V_{DD}-0.2V.
2. /S=V_{DD}. All inputs V_{SS} or V_{DD}.
3. In Sleep mode and /S=V_{DD}. All inputs V_{SS} or V_{DD}.
4. $V_{SS} \le V_{IN} \le V_{DD}$ and $V_{SS} \le V_{OUT} \le V_{DD}$.

AC Parameters (T_A = -40°C to + 85°C, V_{DD} = 2.7V to 3.6V, C_L = 30pF)

Symbol	Parameter	Min	Max	Units	Notes
f_{CK}	C Clock Frequency	0	40	MHz	
t_{CH}	Clock High Time	11		ns	1
t_{CL}	Clock Low Time	11		ns	1
t_{SU}	Chip Select Setup	10		ns	
t_{SH}	Chip Select Hold	10		ns	
t_{OD}	Output Disable Time		12	ns	2
t_{ODV}	Output Data Valid Time		9		
t_{OH}	Output Hold Time	0		ns	
t_D	Deselect Time	40		ns	
t_R	Data In Rise Time		50	ns	2,3
t_F	Data In Fall Time		50	ns	2,3
t_{SU}	Data Setup Time	5		ns	
t_H	Data Hold Time	5		ns	
t_{HS}	/HOLD Setup Time	10		ns	
t_{HH}	/HOLD Hold Time	10		ns	
t_{HZ}	/HOLD Low to Hi-Z		20	ns	2
t_{LZ}	/HOLD High to Data Active		20	ns	2

Notes
1. $t_{CH} + t_{CL} = 1/f_{CK}$.
2. This parameter is characterized but not 100% tested.
3. Rise and fall times measured between 10% and 90% of waveform.

AC Test Conditions

Input Pulse Levels	10% and 90% of V_{DD}
Input rise and fall times	3 ns
Input and output timing levels	0.5 V_{DD}
Output Load Capacitance	30 pF

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 3.3V)

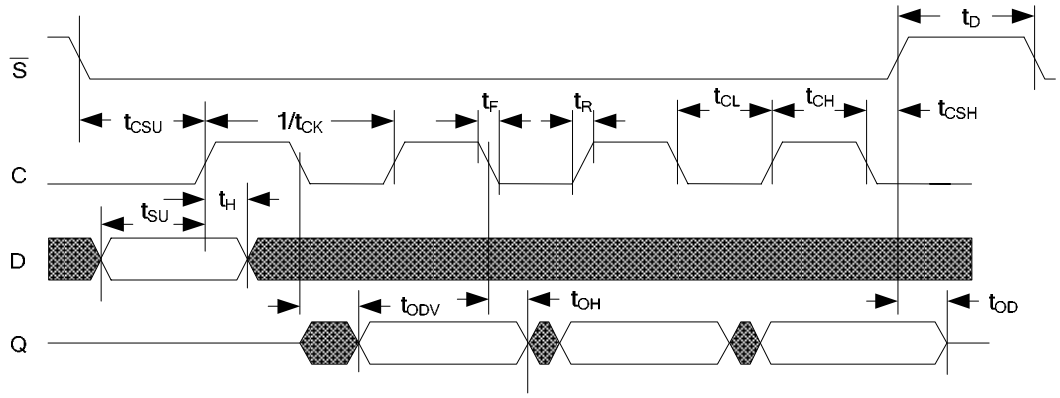
Symbol	Parameter	Min	Max	Units	Notes
C_O	Output Capacitance (Q)	-	8	pF	1
C_I	Input Capacitance	-	6	pF	1

Notes
1. This parameter is characterized and not 100% tested.

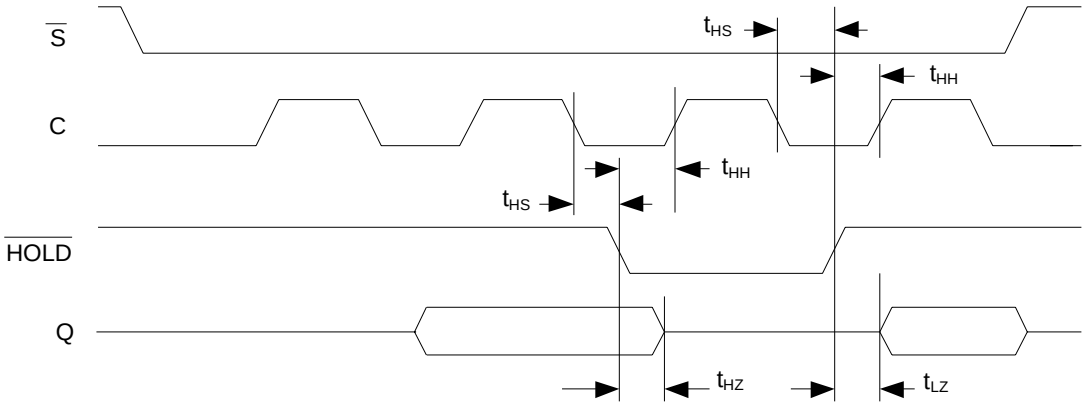
Data Retention (T_A = -40°C to +85°C)

Symbol	Parameter	Min	Units	Notes
T_{DR}	Data Retention	10	Years	

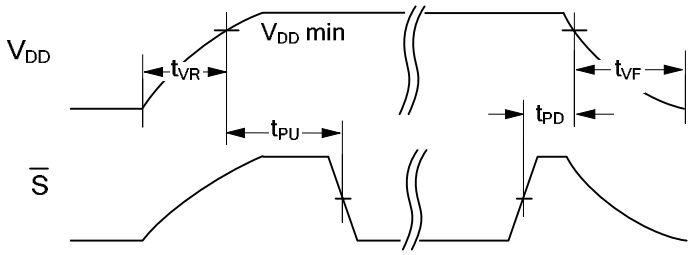
Serial Data Bus Timing



/HOLD Timing



Power Cycle Timing



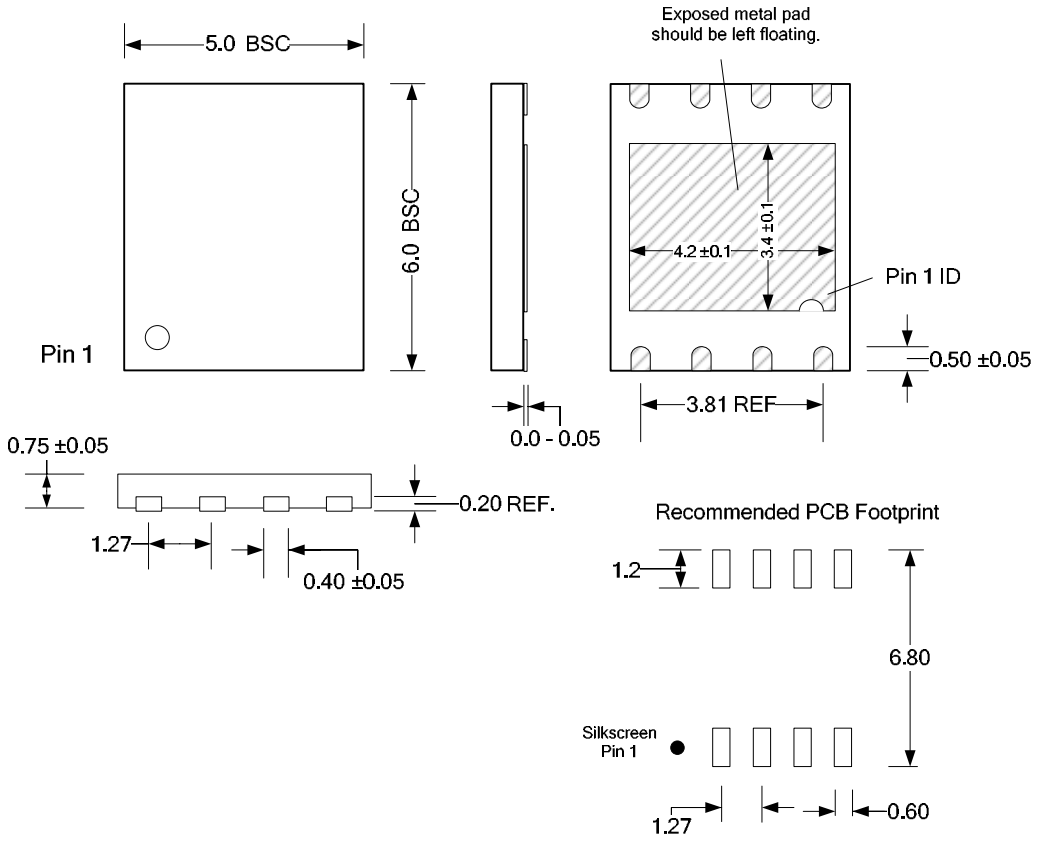
Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	Power Up (V_{DD} min) to First Access (/S low)	1	-	ms	
t_{PD}	Last Access (/S high) to Power Down (V_{DD} min)	0	-	µs	
t_{REC}	Recovery Time from Sleep Mode	-	450	µs	
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1,2
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1,2

Notes
1. This parameter is characterized and not 100% tested.
2. Slope measured at any point on V_{DD} waveform.

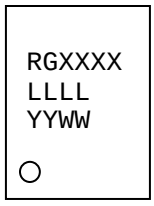
Mechanical Drawing

8-pin TDFN (5.0 mm x 6.0 mm body, 1.27 mm pad pitch)



Note: All dimensions in millimeters. **This package is footprint compatible with the 8-pin SOIC. The exposed pad should be left floating.**

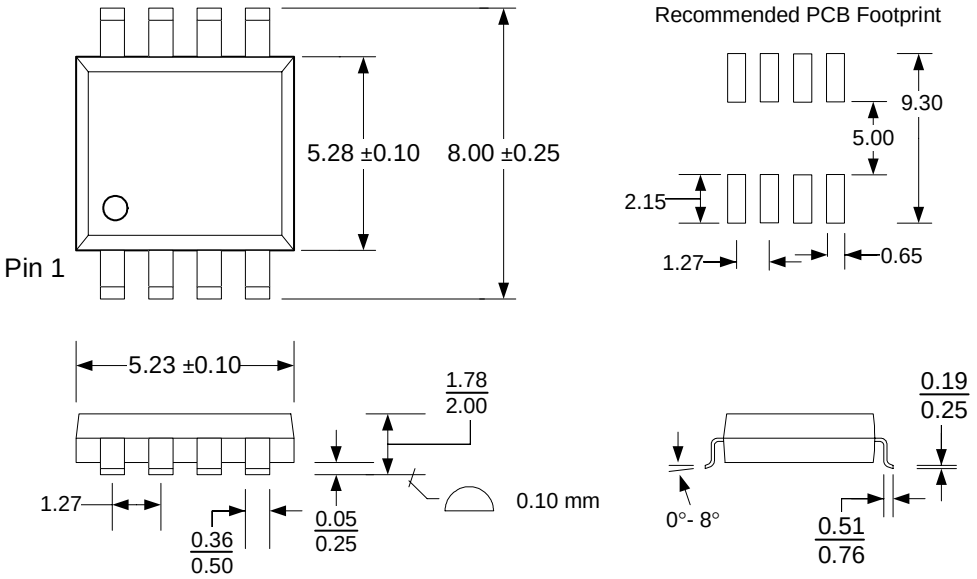
TDFN Package Marking Scheme for Body Size 5.0mm x 6.0mm



Legend:
R=Ramtron, G="green" TDFN package
XXXX=base part number
LLLL= lot code
YY=year, WW=work week

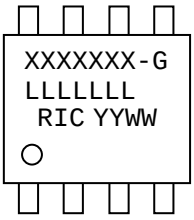
Example: "Green" TDFN package, FM25H20, Lot 0012, Year 2008, Work Week 31
RG5H20
0012
0831

8-pin EIAJ SOIC



All dimensions in millimeters.

EIAJ SOIC Package Marking Scheme



Legend:
XXXXXX= part number
LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

FM25H20, "Green" EIAJ SOIC package, Year 2009, Work Week 40
FM25H20-G
B90003G1
RIC 0940

Revision History

Revision	Date	Summary
1.0	8/22/2007	Initial release.
1.1	3/18/2008	Changed endurance limit. Changed I_{DD}, I_{SB}, and I_{ZZ} limits. Changed t_{REC} sleep mode exit timing spec. Added package MSL rating and placeholder for ESD ratings. Changed V_{OH}/V_{OL} specs.
1.2	8/11/2008	Removed Q pin's ability to drive high/low during wakeup from Sleep mode (pg. 8). The user must wait t_{REC} for the device to be ready for normal operation.
1.3	1/28/2009	Added Tape & Reel ordering information. Modified mechanical drawing and added pcb footprint.
2.0	2/25/2009	Changed status to Pre-Production. Modified mechanical drawing and added pcb footprint.
2.1	9/15/2009	Added EIAJ SOIC package. Added ESD ratings. Changed recommended DFN pcb footprint. Updated lead temperature rating in Abs Max table.