FM3144

4xSPST Antenna Tuning Switch

Features

- Broadband frequency range: 0.4 to 5.0GHz
- MIPI RFFE V2.1 interface compatible
- Small QFN 12-pin (1.5mm x 1.5mm x 0.45mm) package, MSL1

Applications

- GSM/WCDMA/LTE/5G NR band and mode switching
- Antenna tuning switching

Description

The FM3144 is a CMOS silicon-on-insulator (SOI), four single-pole, single-throw (4xSPST) switch. The high linearity and ruggedness performance and extremely low Ron and COFF make the device an ideal choice for GSM/WCDMA/LTE/5G NR handset antenna tuning application.

The FM3144 is compatible with MIPI RFFE V2.1 control interface, which is a key requirement for many cellular transceivers. It is provided in a compact QFN 12-pin 1.5mm x 1.5mm x 0.45mm package. A functional block diagram is shown in Figure 1. The pin configuration and package are also shown in Figure 1. Signal pin assignments and functional pin descriptions are provided in Table 1.

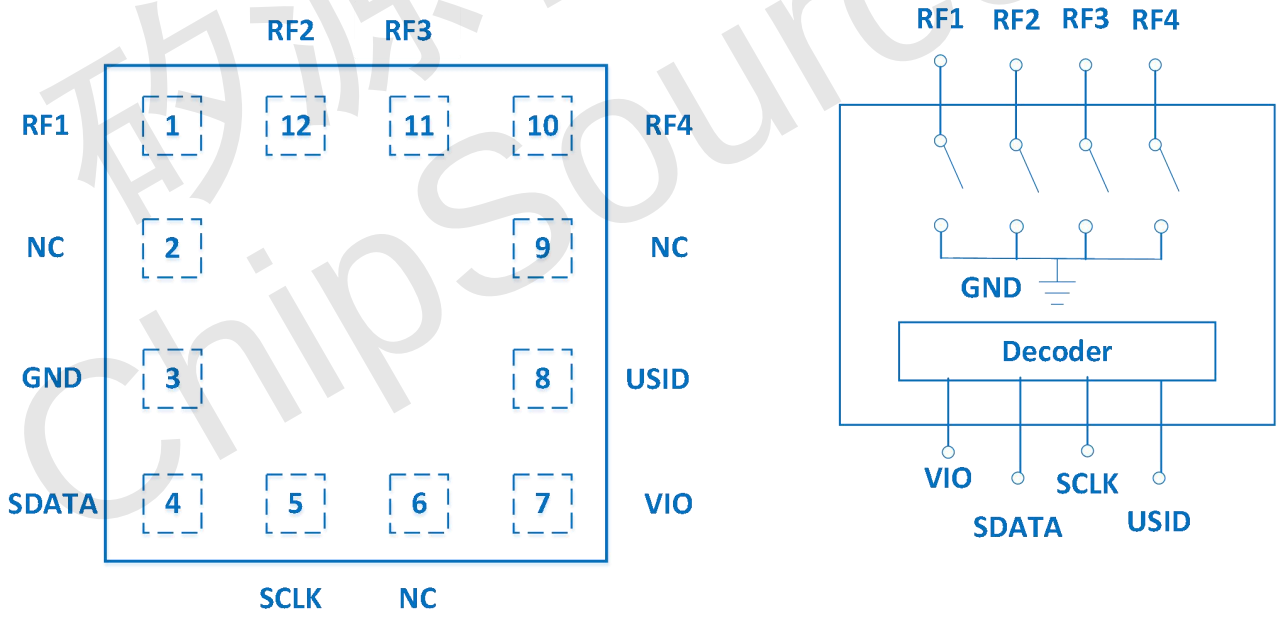

Figure 1 Functional Block Diagram and Pin Configuration (Top View)

Function Characteristics

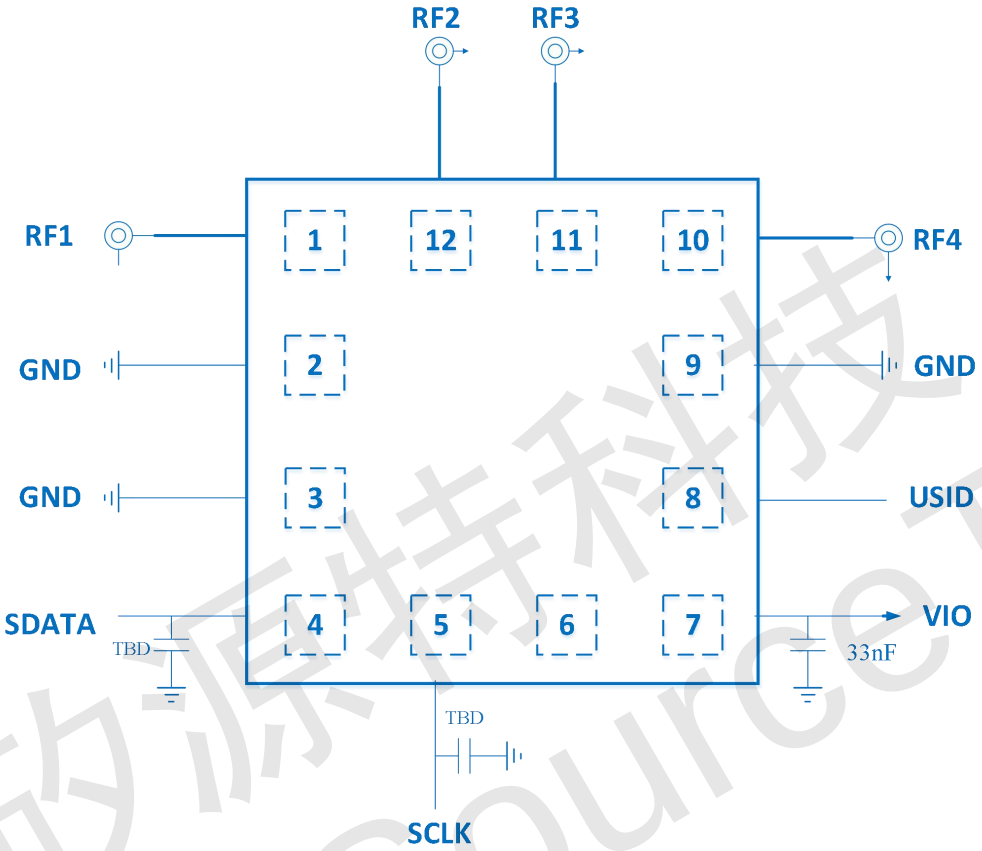

Figure 2. Application Circuit

Table 1 Pin Descriptions

NO.	Name	Description	NO.	Name	Description
1	RF1	RF Port1	7	VIO	RFFE Reference Voltage
2	NC	Can be grounded or Not Connect	8	USID	RFFE USID Select Pin
3	GND	Ground	9	NC	Can be grounded or Not Connect
4	SDATA	RFFE Data Bus	10	RF4	RF Port4
5	SCLK	RFFE Clock Bus	11	RF3	RF Port3
6	NC	Can be grounded or Not Connect	12	RF2	RF Port2

Table 2 Register_0 for RF Operating Modes

State	Mode	D7	Register_0						
			D6	D5	D4	D3	D2	D1	D0
1	All ISO	x	x	x	x	0	0	0	0
2	RF1 to GND	x	x	x	x	0	0	0	1
3	RF2 to GND	x	x	x	x	0	0	1	0
4	RF2 & RF1 to GND	x	x	x	x	0	0	1	1
5	RF3 to GND	x	x	x	x	0	1	0	0
6	RF3 & RF1 to GND	x	x	x	x	0	1	0	1
7	RF3 & RF2 to GND	x	x	x	x	0	1	1	0
8	RF3, RF2 & RF1 to GND	x	x	x	x	0	1	1	1
9	RF4 to GND	x	x	x	x	1	0	0	0
10	RF4 & RF1 to GND	x	x	x	x	1	0	0	1
11	RF4 & RF2 to GND	x	x	x	x	1	0	1	0
12	RF4, RF2 & RF1 to GND	x	x	x	x	1	0	1	1
13	RF4 & RF3 to GND	x	x	x	x	1	1	0	0
14	RF4, RF3 & RF1 to GND	x	x	x	x	1	1	0	1
15	RF4, RF3 & RF2 to GND	x	x	x	x	1	1	1	0
16	All to GND	x	x	x	x	1	1	1	1

x-- either 0 or 1

Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
RFFE Reference Voltage	V_{IO}	-0.3	2.5	V	T_A=25℃
RFFE Bus Voltage(SDATA, SCLK)	V_I	-0.3	2.5	V	T_A=25℃
RFFE USID Voltage	V_{USID}	-0.3	2.5	V	T_A=25℃
Max RF Input Power (RF1/2/3/4 to GND)	P_{INMAX}		47	dBm	F_0=0.4 to 5.0GHz, 20% DC V_{IO}=1.8V, VSWR=1:1, T_A=25℃
Device Operating Temperature	T_{OP}	-40	90	℃	
Device Storage Temperature	T_{STG}	-55	150	℃	
Electrostatic Discharge(All Pins)	$V_{ESD(HBM)}$	1000		V	Human Body Model
	$V_{ESD(CDM)}$	1000		V	Charged Device Model

Notice

Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Table 4 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Frequency	F_0	0.4		5.0	GHz
Power Supply for MIPI	V_{IO}	1.65	1.80	1.95	V
RFFE Bus Voltage(SDATA, SCLK) High	V_{IH}	0.8*VIO	VIO	VIO	V
RFFE Bus Voltage(SDATA, SCLK) Low	V_{IL}	0	0	0.2*VIO	V
RFFE USID Voltage	V_{USID}	0		VIO	V

Table 5 Nominal Operating Parameters

Parameter	Symbol	Specification			Unit	Condition
		MIN	TYP	MAX		
Normal Condition	V_{IO}=1.80V, V_{IH}=1.80V, V_{IL}=0V, P_{IN}=0dBm, VSWR=1:1, T_A=25℃, Unless Otherwise Stated					
DC Characteristics						
VIO Current	I_{IO}		160	220	μA	Active State
			20	30	μA	Low Power State
VIO Supply Rise Time	T_{VIO_R}	80			μs	VIO(OFF) to VIO(MIN) to enable to trigger POR, VIO(OFF)≤120mV
VIO Supply Reset Time	T_{VIO_RST}			10	μs	Time for VIO Off to its Repower-up to trigger POR
RF Path Switching Speed	T_{SW}			20	μs	End of RFFE Command (50% of SCLK) to 90% RF Output
Adjacent Port Isolation (One Port On, Another Port Off)	ISO	39			dB	F_0=617 to 960MHz
		28			dB	F_0=960 to 2170MHz
		23			dB	F_0=2170 to 2700MHz
		18			dB	F_0=3300 to 3800MHz
		14			dB	F_0=3800 to 4200MHz
		11			dB	F_0=4200 to 5000MHz
Adjacent Port Isolation (All Ports Off)	ISO	28			dB	F_0=617 to 960MHz
		23			dB	F_0=960 to 2170MHz
		18			dB	F_0=2170 to 2700MHz
		16			dB	F_0=3300 to 3800MHz
		13			dB	F_0=3800 to 4200MHz
		11			dB	F_0=4200 to 5000MHz
Non-Adjacent Port Isolation (One Port On, Another Port Off)	ISO	43			dB	F_0=617 to 960MHz
		38			dB	F_0=960 to 2170MHz
		31			dB	F_0=2170 to 2700MHz
		28			dB	F_0=3300 to 3800MHz
		23			dB	F_0=3800 to 4200MHz
		18			dB	F_0=4200 to 5000MHz
Non-Adjacent Port Isolation (All Ports Off)	ISO	43			dB	F_0=617 to 960MHz
		38			dB	F_0=960 to 2170MHz
		36			dB	F_0=2170 to 2700MHz
		31			dB	F_0=3300 to 3800MHz
		28			dB	F_0=3800 to 4200MHz
		26			dB	F_0=4200 to 5000MHz

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Parameter	Symbol	Specification			Unit	Condition
		MIN	TYP	MAX		
On Resistance	R_{ON}		2.3	2.5	Ω	Switch on Path @ DC
Off Resistance	R_{OFF}	200			kΩ	Switch off Path @ DC
Off Capacitance	C_{OFF}			0.16	pF	Switch off Path
RFx Port Off Harmonics	$2F_0$			-75	dBm	GSM850/900@35dBm,CW
	$3F_0$			-75	dBm	GSM850/900@35dBm,CW
	$2F_0$			-75	dBm	GSM1800/1900@33dBm,CW
	$3F_0$			-75	dBm	GSM1800/1900@33dBm,CW
RFx Port Off Vpeak	V_{RF}	80			V	GSM850/900 Tx Band
		80			V	GSM1800/1900 Tx Band

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MIPI RFFE Read and Write Timing

The FM3144 supports the following operating commands which are stated in the MIPI Alliance Specification for RF Front-End Control Interface (RFFESM) V2.1 (18-DEC-2017).

- Register 0 Write
- Register Write
- Register Read
- Extended Register Write
- Extended Register Read
- Masked Write
- USID Program (Procedure1 to 3)

Figure 3 and Figure 4 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 5 describes the Register_0 write command sequence. In the below timing figures, SA[3:0] is the slave address. A[4:0] is the register address. D[7:0] is the data. “P” is a parity bit.

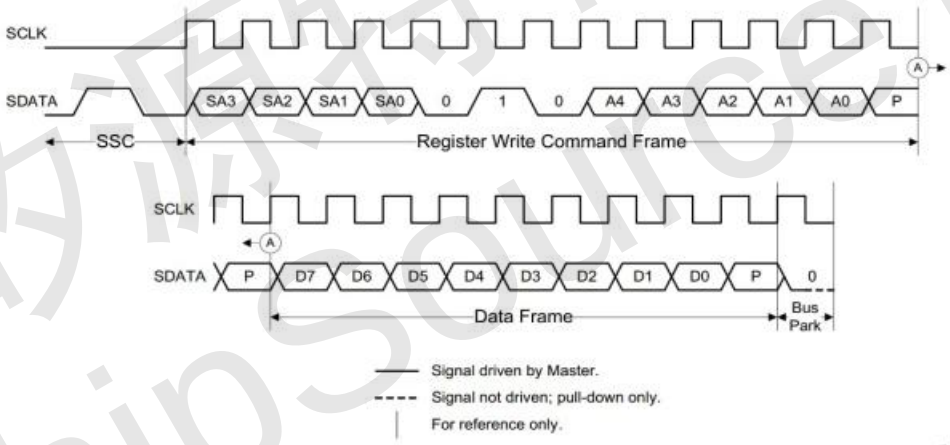


Figure 3 Register Write Command Sequence

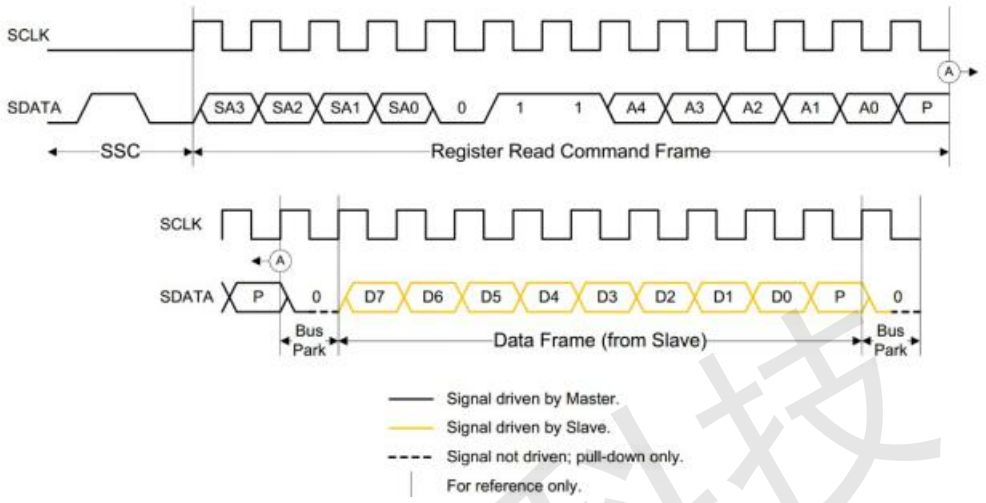


Figure 4 Register Read Command Sequence

Figure 5 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and a only seven- bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle.

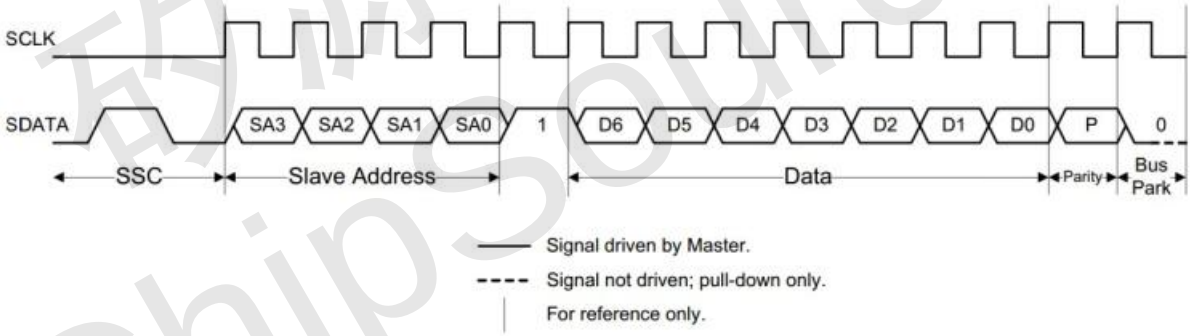


Figure 5 Register_0 Write Command Sequence

Other information such as MIPI USID programming sequence, MIPI bus specifications, etc. are stated in the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V2.1 (18-DEC-2017).

Register Definition

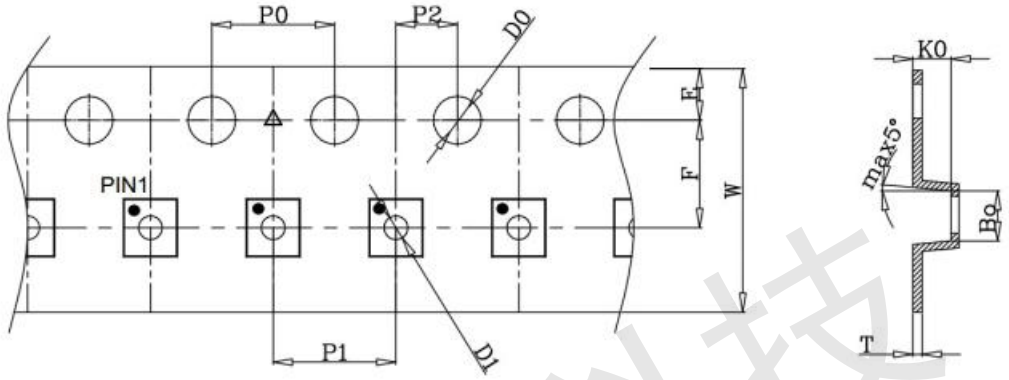
Table 6 Register Definition Table

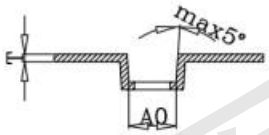
Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x00	REGISTER_0	7:0	R/W	RF Control	Register_0 truth Table: Table 2	0x00	No	Yes
		7	R/W	PWR_MODE_1	0b0: Normal Operation Mode Write Value:0b0, Read Value:0b0 0b1: Low Power Mode Write Value:0b1, Read Value:0b1	0b1	Yes	No
		6	R/W	PWR_MODE_0	0b0: Normal Operation (ACTIVE) 0b1: Reset all registers to default settings (STARTUP) Write value: 0b1, Read Value: 0b0	0b0	Yes	No
					Note: Writing PWR_MODE_0 with a logic '1' will reset all register, and then automatically reenter the Active Mode.			
		5	R/W	Trigger_Mask_2	0b0: Trigger_2 enabled 0b1: Trigger_2 disabled	0b0	No	No
		4	R/W	Trigger_Mask_1	0b0: Trigger_1 enabled 0b1: Trigger_1 disabled	0b0	No	No
		3	R/W	Trigger_Mask_0	0b0: Trigger_0 enabled 0b1: Trigger_0 disabled	0b0	No	No
		Note: If any one of the three Trigger Masks is set to a logic '1' the corresponding Trigger is disabled, in that case data written to a register associated with the Trigger goes directly to the destination register. Otherwise, if the Trigger Mask is enabled (via a logic '0'), incoming data is written to the shadow register, and the destination register is unchanged until its corresponding Trigger is asserted.						
		2	W	Trigger_2	0b0: Keep its associated destination registers unchanged 0b1:Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_2 is disabled(Logic '0')	0b0	Yes	No

0x1C	PM_TRIG	1	W	Trigger_1	0b0: Keep its associated destination registers unchanged 0b1:Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_1 is disabled(Logic '0')	0b0	Yes	No
		0	W	Trigger_0	0b0: Keep its associated destination registers unchanged 0b1:Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_0 is disabled(Logic '0')	0b0	Yes	No
0x1D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x52	No	No
0x1E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x78	No	No
0x1F	MAN_USID	7:6	R	RESERVED		0b00	No	No
		5:4	R	MANUFACTURER_ID[9:8]	Upper two bits of MIPI registered Manufacturer ID	0b10	No	No
		3:0	R/W	USID	Unique Slave Address		No	No
					USID pin connected to GND	0x6		
					USID pin connected to VIO	0x7		
0x20	Extended PID	7:0	R	EXT_PRODUCT_ID[15:8]	Extended Product Number	0x00	No	No
0x21	Chip ID	7:0	R	Chip_ID[7:0]	Chip ID Number	0x00	No	No
0x22	GROUP_SID	7:4	R/W	GSID0	Group Slave ID0	0x0	No	No
		3:0	R/W	GSID1	Group Slave ID1	0x0	No	No
					0b0: Normal operation 0b1: Software reset	0b0	No	No

0x23	UDR_RST	7	W	SOFTWARE RESET	Note: During software reset, this register and all configurable registers are set to their default values except for reserved registers.			
		6:0	R	RESERVED	Reserved for future use	0b000_0000	NO	NO
0x24	ERR_SUM	7	R/W	SPARE	Reserved for future use	0b0	NO	NO
		6	R/W	COM_FP_P_ER	Command Frame with parity error	0b0	No	No
		5	R/W	COM_LEN_ER	Command Sequence with incorrect length	0b0	No	No
		4	R/W	ADD_FP_P_ER	Address Frame with parity error	0b0	No	No
		3	R/W	DAT_FP_P_ER	Data Frame with parity error	0b0	No	No
		2	R/W	RD_IVD_ADD	Read Command Sequence to an invalid address	0b0	No	No
		1	R/W	WR_IVD_ADD	Write Command Sequence to an invalid address	0b0	No	No
		0	R/W	BID_GID_ER	Read Command Sequence with a BSID or GSID Note: Reading this register resets this register.	0b0	No	No

Tape and Reel Dimensions





SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	1.65±0.05	1.65±0.05	0.50±0.05	4.00±0.10	4.00±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.20±0.05	1.75±0.10	3.50±0.05	1.55±0.05	0.50±0.10	8.00±0.10

Figure 8 Tape and Reel Dimensions

Reflow Chart

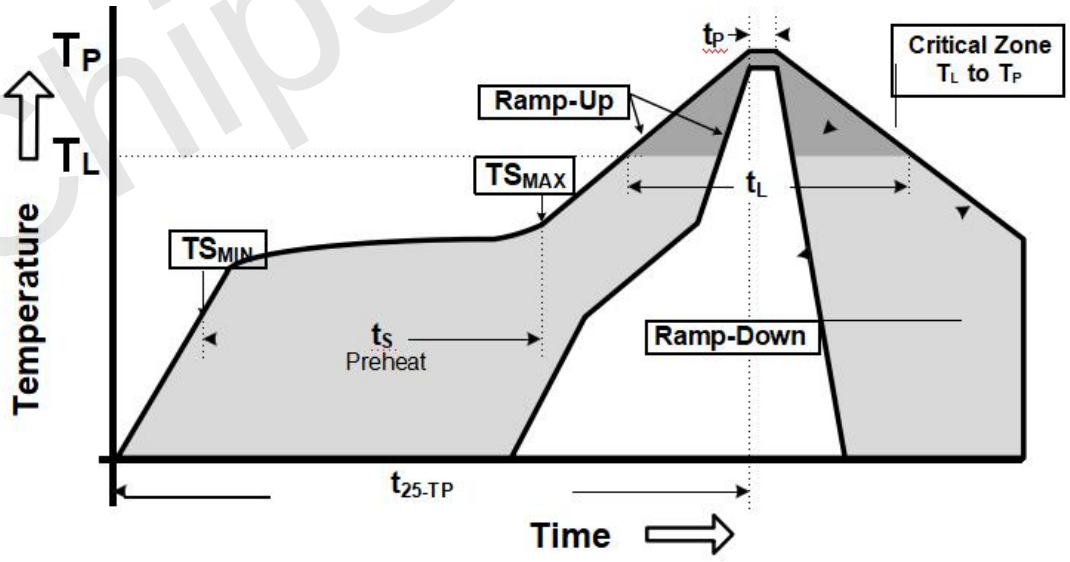


Figure 9 Recommended Lead-Free Reflow Profile

Table 7 Reflow Chart Parameters

Reflow Profile	Parameter
Preheat Temperature(T_{SMIN} to T_{SMAX})	150℃ to 200℃
Preheat Time(ts)	60 to 180 Seconds
Ramp-Up Rate(T_{SMAX} to T_P)	3℃/s MAX
Time Above T_L 217℃(t_L)	60 to 150 Seconds
Peak Temperature (T_P)	260℃
Time within 5℃ of Peak Temperature(t_P)	20 to 40 Seconds
Ramp-Down Rate(T_{SMAX} to T_P)	6℃/s MAX
Time for 25℃ to Peak Temperature($t_{25\text{-}TP}$)	8 Minutes MAX

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.