FEELING TECHNOLOGY

FM8P756

OTP-Based 8-Bit Microcontroller with LCD Driver

Devices Included in this Data Sheet:

- FM8P756A : 24-pin OTP device
- FM8P756B : 20-pin OTP device
- FM8P756C : 16-pin OTP device
- FM8P756D : 28-pin OTP device with VR pin
- FM8P756E : 24-pin OTP device with VR pin
- FM8P756F : 18-pin OTP device with VR pin
- FM8P756G : 20-pin OTP device with VR pin

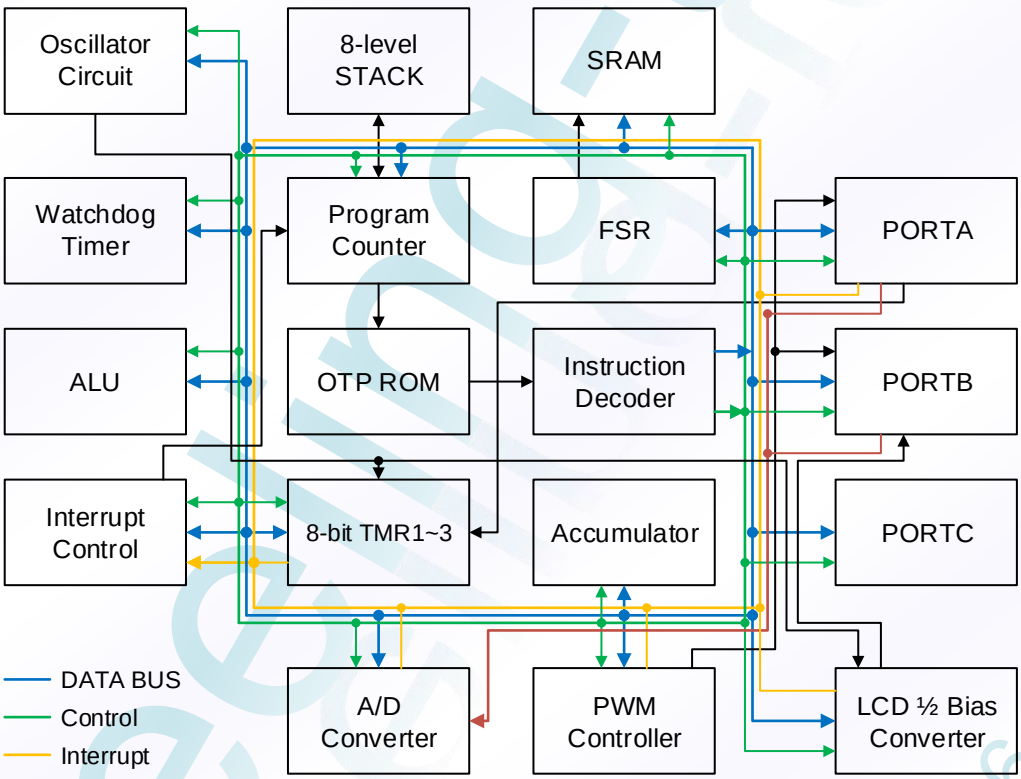
FEATURES

- Total 8 channel 10bit AD converter with ±2LSB resolution
- All instructions are single cycle except for program branches which are two-cycles
- All OTP area GOTO instruction
- All OTP area subroutine CALL instruction
- 8-bit wide data path
- 8-level deep hardware stack
- 2K x 16 bits on chip OTP
- 36x8 bits on chip special purpose registers and 96 x 8 bits on chip general purpose registers (SRAM)
- Operating speed: DC-20 MHz clock input, or DC-100 ns instruction cycle
- Direct, indirect addressing modes for data accessing
- Three real time down-count Timer/Counter with 3-bit programmable prescaler
  - TMR1: 8-bit, PWM1 & Timer
  - TMR2: 8-bit, PWM2 & Timer
  - TMR3: 8-bit, Timer
- Software controlled 4-COM lines LCD driver with 1/2bias
- Built-in 3 levels Low Voltage Detector (LVDT) (2.2V/2.6V/3.7V) for Brown-out Reset (BOR)
- Power-up Reset Timer (PWRT)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation and soft-ware watch-dog enable/disable control
- Three I/O ports Port A, Port B and Port C with independent direction control
  - 21 Bi-direction I/O port (Programmable Pull-up enable in Input mode)
  - One Input only port (IOA7/RSTB)
- Four kinds of interrupt source: 3 Timers/Counters, 8 external interrupt sources: IOA0~IOA7, Internal watchdog timer (i_WDT) wakeup, and A/D end of conversion
- Wake-up from SLEEP:
  - Port A (IOA0~IOA7) pin change wakeup
  - WDT overflow
  - i_WDT overflow
- Power saving SLEEP mode
- Programmable Code Protection
- Selectable oscillator options:
  - ERC: External Resistor/ Voltage Controlled Oscillator
  - XT: Crystal/Resonator Oscillator
  - LF: Low Frequency Crystal Oscillator
  - HIRC: Internal Resistor/Capacitor High speed Oscillator
  - LIRC: Internal Resistor/Capacitor Low speed Oscillator
- Operating voltage range:
  - ≤4MHz: 2.2V to 5.5V
  - ≤8MHz: 2.4V to 5.5V, see 6.1 for more information.

GENERAL DESCRIPTION

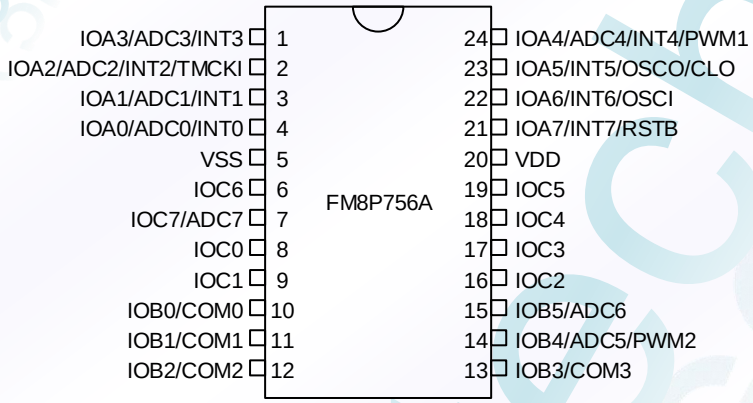
The FM8P756 is a low-cost, high speed, high noise immunity, OTP-based 8-bit CMOS microcontrollers. It employs a RISC architecture with 54 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.
The FM8P756 consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Watchdog Timer, OTP, SRAM, tri-state I/O port, I/O pull-high control, Power saving SLEEP mode, 3 real time programmable clock/counter, Interrupt, Wake-up from SLEEP mode, and Code Protection for OTP products.
There are eight oscillator configurations to be chosen from, including the power-saving LF (Low Frequency) oscillator and cost saving internal RC oscillator.
The FM8P756 address 2K×16 of program memory.
The FM8P756 can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory.
The FM8P756 provides total 8 channel 10bit AD converter with ±2LSB resolution.
The FM8P756 provides total 4 COM LCD pins, drive waveform is controlled by Software.

BLOCK DIAGRAM

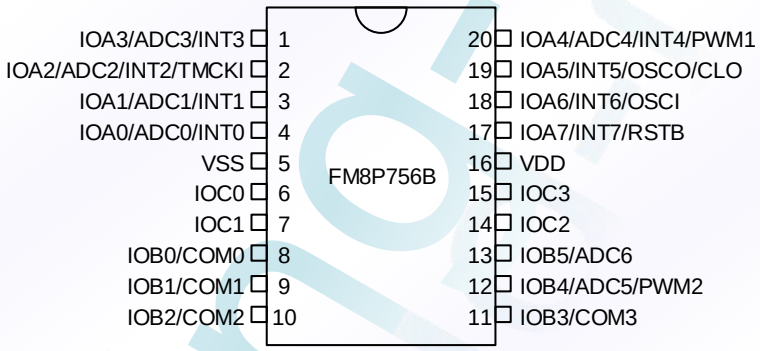


PIN CONNECTION

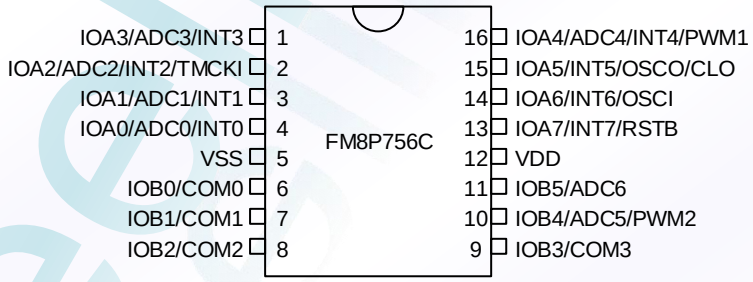
PDIP24, SOP24



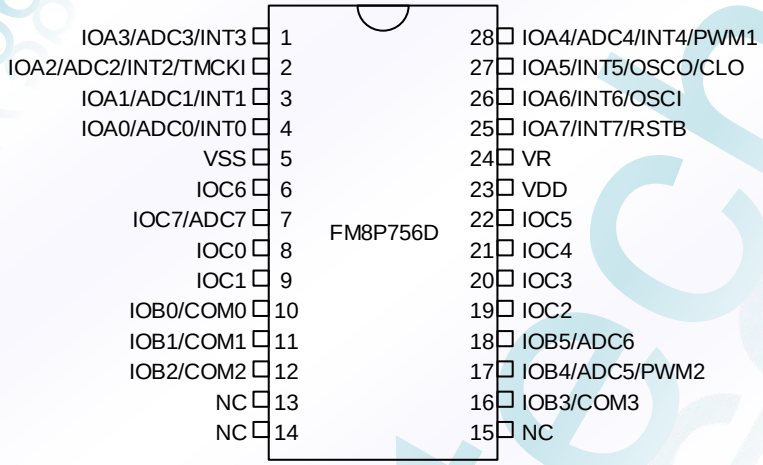
PDIP20, SOP20



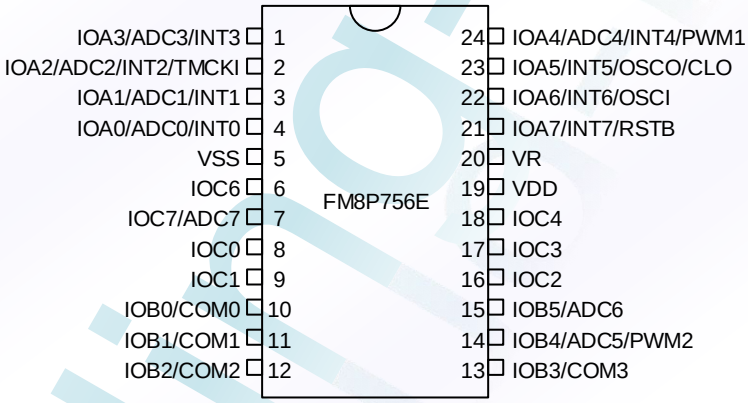
PDIP16, SOP16



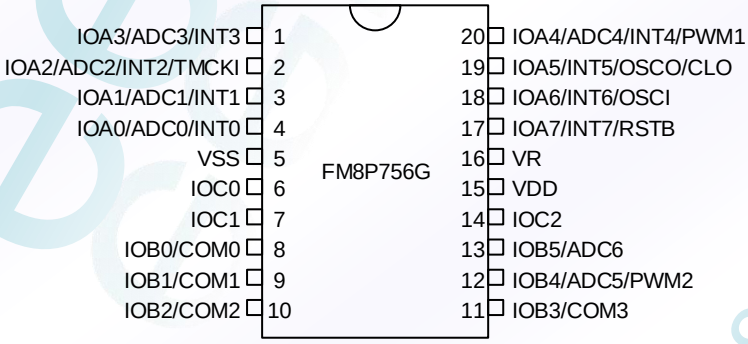
PDIP28, SOP28 (With VR PIN)



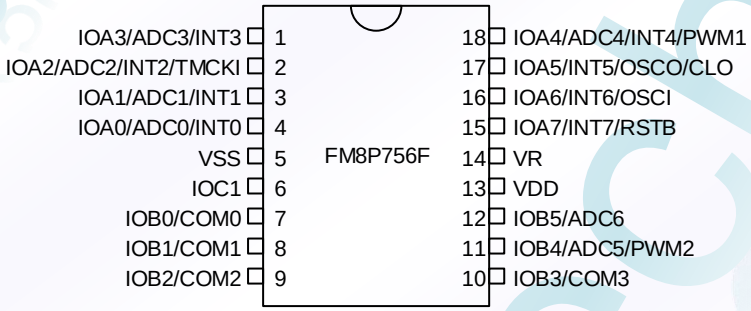
PDIP24, SOP24 (With VR PIN)



PDIP20, SOP20 (With VR PIN)



PDIP18, SOP18 (With VR PIN)



PIN DESCRIPTIONS

Name	I/O	Description
IOA0/AD0/INT0 | IOA4/AD4/INT4	I/O	• Bi-direction I/O port (programmable Pull-high in Input mode) • Wake-up on pin change • External interrupt input • A/D converter input • IOA4 is PWM1 output
IOA5/INT5 /OSCO	I/O	• Bi-direction I/O port (programmable Pull-high in Input mode) • Wake-up on pin change • External interrupt input • Clock output shared with IOA5 • Oscillator output (XT, LF, ERC mode)
IOA6/INT6 /OSCI	I/O	• Bi-direction I/O port (programmable Pull-high in Input mode) • Wake-up on pin change • External interrupt input • Oscillator input (XT, LF, ERC mode)
IOA7/INT7 /RSTB	I	• Input port • Wake-up on pin change • External interrupt input • System clear (RESET) input. **This pin is an active low RESET to the device. The voltage on this pin must not exceed VDD.**
IOB0/COM0 | IOB3/COM3	I/O	• Bi-direction I/O port (programmable Pull-high in Input mode) • Software controlled 1/2bias LCD COM0 ~ COM3 output
IOB4/AD5 | IOB5/AD6	I/O	• Bi-direction I/O port (programmable Pull-high in Input mode) • IOB4 is PWM2 output • A/D converter input
IOC0 | IOC6	I/O	• Bi-direction I/O port (programmable Pull-high in Input mode) • LCD segment output
IOC7/ADC7	I/O	• Bi-direction I/O port (programmable Pull-high in Input mode) • LCD segment output • A/D converter input
VR	-	ADC module reference input. **The voltage on this pin must not exceed VDD.**
VDD	-	Positive supply
VSS	-	Ground

Legend: I=input, O=output, I/O=input/output

Note: Please refer to 2.2 for detail IO type description

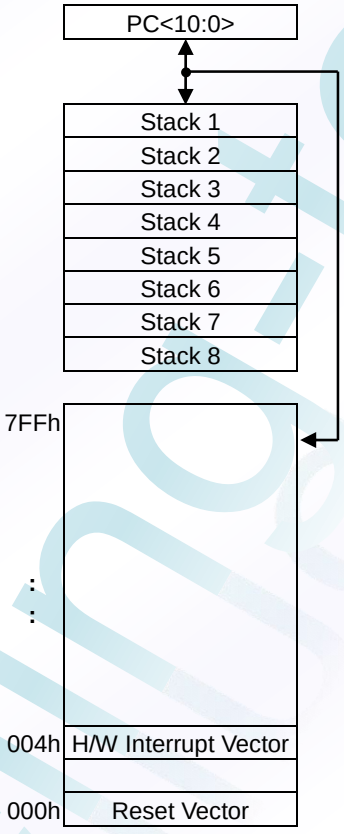
1.0 MEMORY ORGANIZATION

FM8P756 memory is organized into program memory and data memory.

1.1 Program Memory Organization

The FM8P756 has a 11-bit Program Counter capable of addressing a 2K×16 program memory space.
The RESET vector for the FM8P756 is at 000h.
The H/W interrupt vector is at 004h.
FM8P756 supports all OTP area CALL/GOTO instructions without page.

Figure 1.1: Program Memory Map and STACK



FM8P756

1.2 Data Memory Organization

Data memory is composed of 36 bytes Special Function Registers and 96 bytes General Purpose Registers. The data memory can be accessed either directly or indirectly through the FSR register.

Table 1.1: Registers File Map for FM8P756

Address	Description
00h : : 2Ch	Special Purpose Register
40h : : 9Fh	General Purpose Register

Table 1.2: Special Purpose Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
System									
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
01h (r/w)	PCL	Low order 8 bits of PC							
02h (r/w)	PCHBUF	-	-	-	-	-	High order 3 bits of PC		
03h (r/w)	STATUS	-	-	-	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04h (r/w)	FSR	Indirect data memory address pointer							
IO PAD & CONTROL									
05h (r/w)	IOSTA	-	IOSTA6	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0
06h (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
07h (r/w)	IOSTB	-	-	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0
08h (r/w)	PORTB	-	-	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
09h (r/w)	IOSTC	IOSTC7	IOSTC6	IOSTC5	IOSTC4	IOSTC3	IOSTC2	IOSTC1	IOSTC0
0Ah (r/w)	PORTC	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
Timer1: 8-bit Timer & PWM1 Duty									
10h (r/w)	T1CON	T1EN	-	T1SO1	T1SO0	T1EDG	T1PS2	T1PS1	T1PS0
11h (r/w)	PWM1CON	T1MOD	PWM1S	EPWM1	-	PIR13	PIR12	PIR11	PIR10
12h (r/w)	T1LA	8-bit real-time timer/counter latch							
2Bh (r)	T1CNT	8-bit real time timer/counter Count							
Timer2: 8-bit Timer & PWM2 Duty									
13h (r/w)	T2CON	T2EN	-	T2SO1	T2SO0	T2EDG	T2PS2	T2PS1	T2PS0
14h (r/w)	PWM2CON	T2MOD	PWM2S	EPWM2	-	PIR23	PIR22	PIR21	PIR20
15h (r/w)	T2LA	8-bit real-time timer/counter latch							
2Ch (r)	T2CNT	8-bit real time timer/counter Count							
Timer3: 8-bit Timer									
16h (r/w)	T3CON	T3EN	T3LOAD	T3SO1	T3SO0	T3EDG	T3PS2	T3PS1	T3PS0
17h (r/w)	T3LA	8-bit real-time timer/counter latch							
18h (r)	T3CNT	8-bit real-time timer/counter Count							
IRQ									
19h (r/w)	INTEN	GIE	ADCIE	PAIE	COMIE	-	T3IE	T2P2IE	T1P1IE
1Ah (r/w)	INTFLAG	-	ADCIF	PAIF	COMIF	-	T3IF	T2P2IF	T1P1IF

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
ADC Control									
1Bh (r/w)	ADCON1	ADCEN	-	-	-	-	CHSL2	CHSL1	CHSL0
1Ch (r/w)	ADCON2	-	-	-	-	-	-	CLKSL1	CLKSL0
1Dh (r/w)	ADCON3	-	-	-	-	ANISL3	ANISL2	ANISL1	ANISL0
1Eh (r)	ADDATL	D1	D0	-	-	-	-	-	-
1Fh (r)	ADDATH	D9	D8	D7	D6	D5	D4	D3	D2
Software LCD									
20h (r/w)	COMCON1	-	-	-	-	COM3E	COM2E	COM1E	COM0E
21h (r/w)	COMCON2	COMEN	-	-	COMIS1	COMIS0	COMCK2	COMCK1	COMCK0
Others									
22h (r/w)	SYSCLK	CLKS	-	-	-	-	-	IRCPD	ECLKPD
23h (r/w)	CLOCON	CLOEN	-	EXCLK	DINV	DUTY	CLOPS2	CLOPS1	CLOPS0
25h (r/w)	APHCON	-	PHA6	PHA5	PHA4	PHA3	PHA2	PHA1	PHA0
26h (r/w)	BPHCON	-	-	PHB5	PHB4	PHB3	PHB2	PHB1	PHB0
27h (r/w)	CPHCON	PHC7	PHC6	PHC5	PHC4	PHC3	PHC2	PHC1	PHC0
28h (r/w)	INTPA	PA7IEN	PA6IEN	PA5IEN	PA4IEN	PA3IEN	PA2IEN	PA1IEN	PA0IEN
29h (r/w)	WDTCON	WDTEN	I_WDT	I_TWDT	-	-	WDTPS2	WDTPS1	WDTPS0
2Ah (r/w)	TAB_BNK	-	-	-	-	-	BNK2	BNK1	BNK0

Legend: - = unimplemented, read as '0'.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

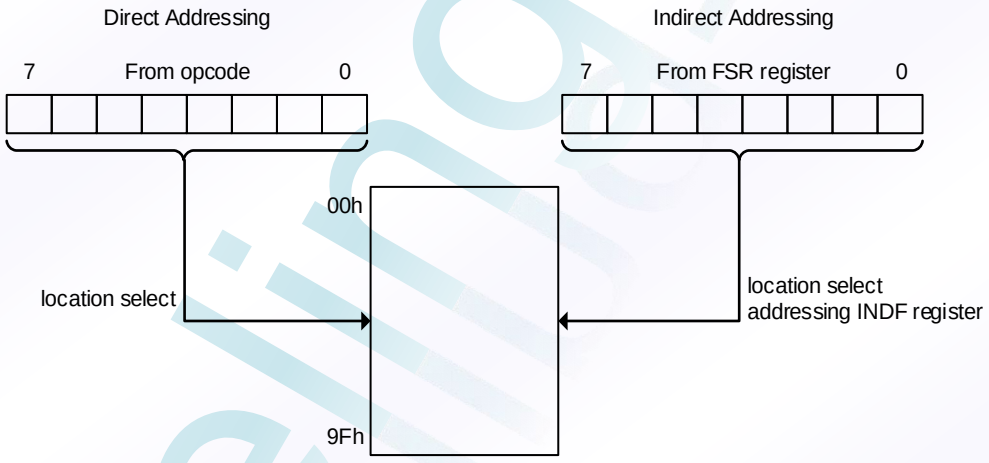
2.1.1 INDF (Indirect Addressing Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0") will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).

Example 2.1: INDIRECT ADDRESSING
Register file 48 contains the value 10h
Register file 49 contains the value 0Ah
Load the value 48 into the FSR Register
A read of the INDF Register will return the value of 10h
Increment the value of the FSR Register by one (@FSR=49h)
A read of the INDF register now will return the value of 0Ah.

Figure 2.1: Direct/Indirect Addressing for FM8P756



2.1.2 PCL / PCHBUF (Low / High Bytes of Program Counter) & Stack

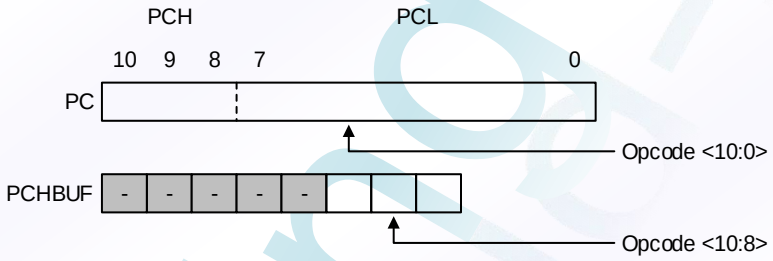
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
01h (r/w)	PCL	Low order 8 bits of PC							
02h (r/w)	PCHBUF	-	-	-	-	-	High order 3 bits of PC		

Legend: - = unimplemented, read as '0'.

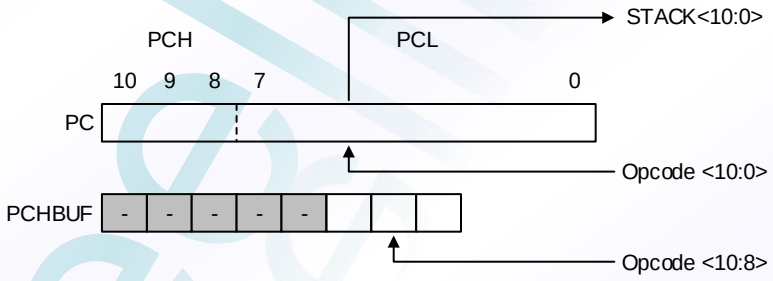
FM8P756 devices have an 11-bits wide Program Counter (PC) and eight-level deep 11-bit hardware push/pop stack. This 11-bits Program Counter can be accessed and controlled by two registers, PCHBUF and PCL. The low byte of PC control register is called the PCL. This register is readable and writable. The high byte of PC control register is called the PCHBUF. This register contains the PC<10:8> bits also readable or writable.
The PCL and PCHBUF registers normally indicate the value of Program Counter. But when interrupt occurrence and execution of RETF and RETFIE, the PCHBUF data would not be update.
Any address within the program memory can be written into PCL and PCHBUF registers. If the PCHBUF register been changed and different from Program Counter., the value of PCHBUF register updated only when execute GOTO, CALL, RETURN, or PCL value changed or increases from 0xff to 0x00. Once the value of PCL register changed, the program and Program Counter will jump to the location indicated by PCL and PCHBUF register.

Figure 2.2: Loading of PC in Different Situations

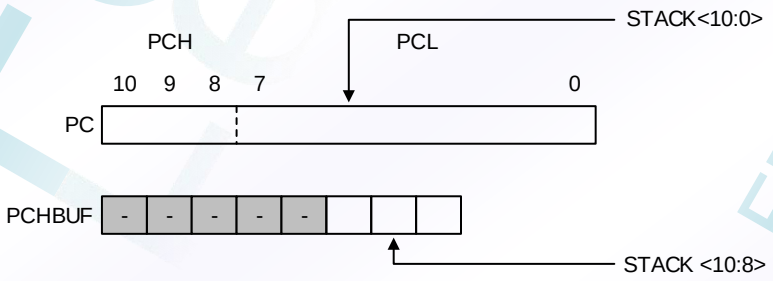
Situation 1: GOTO Instruction



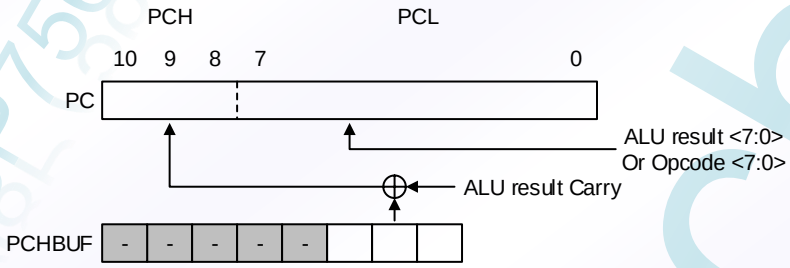
Situation 2: CALL Instruction



Situation 3: RETURN, RETF, RETIA or RETFIE Instruction



Situation 4: Instruction with PCL as destination



2.1.3 STATUS (Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
03h (r/w)	STATUS	-	-	-	$\overline{TO}$	$\overline{PD}$	Z	DC	C

Legend: - = unimplemented, read as '0'.

This register contains the arithmetic status of the ALU, the RESET status.
If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C : Carry/borrow bit.
ADDAR
= 1, Carry occurred.
= 0, No Carry occurred.
SUBAR
= 1, No borrow occurred.
= 0, Borrow occurred.
Note : A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC : Half carry/half borrow bit
ADDAR
= 1, Carry from the 4th low order bit of the result occurred.
= 0, No Carry from the 4th low order bit of the result occurred.
SUBAR
= 1, No Borrow from the 4th low order bit of the result occurred.
= 0, Borrow from the 4th low order bit of the result occurred.

Z : Zero bit.
= 1, The result of a logic operation is zero.
= 0, The result of a logic operation is not zero.

$\overline{PD}$: Power down flag bit.
= 1, after power-up or by the CLRWDT instruction.
= 0, by the SLEEP instruction.

$\overline{TO}$: Watch-dog timer overflow flag bit.
= 1, after power-up or by the CLRWDT or SLEEP instruction
= 0, a watch-dog time overflow occurred

2.1.4 FSR (Indirect Data Memory Address Pointer)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
04h (r/w)	FSR	Indirect data memory address pointer							

Bit7:Bit0 : Select registers address in the indirect addressing mode. See 2.1.1 for detail description.

2.1.5 PORTA, PORTB, PORTC, IOSTA, IOSTB and IOSTC (Port Data Registers and Port Direction Control Registers)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
05h (r/w)	IOSTA	-	IOSTA6	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0
06h (r/w)	PORTA	IOA7*	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
07h (r/w)	IOSTB	-	-	IOSTB5	IOSTB4	IOSTB3	IOSTB2	IOSTB1	IOSTB0
08h (r/w)	PORTB	-	-	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
09h (r/w)	IOSTC	IOSTC7	IOSTC6	IOSTC5	IOSTC4	IOSTC3	IOSTC2	IOSTC1	IOSTC0
0Ah (r/w)	PORTC	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0

Legend: - = unimplemented, read as '0'.

The registers (IOSTA, IOSTB and IOSTC) are used to define the input or output of each port.
= 1, Input.
= 0, Output.
Reading the port (PORTA, PORTB and PORTC register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch. Please refer to 2.2 for detail I/O Port description.
Note: IOA7 is read only.

2.1.6 TMR1: 8-bit Timer & PWM1 Duty

The Timer1 is an 8-bit down count timer/counter which includes counter register (T1CNT), and latch register (T1LA). Please refer to 2.3 for detail Timer description.
The Timer1 can also be PWM1 and controlled by the register PWM1CON. Please refer to 2.4 for detail PWM description.

2.1.6.1 T1CON (Timer1 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
10h (r/w)	T1CON	T1EN	-	T1SO1	T1SO0	T1EDG	T1PS2	T1PS1	T1PS0

Legend: - = unimplemented, read as '0'.

T1EN : TMR1 Enable/Disable
= 1, TMR1 (PWM1) Enable.
= 0, TMR1 (PWM1) Disable.

T1SO1:T1SO0 : TMR1 clock source selection

T1SO1	T1SO0	TMR1 clock source
0	0	TMCKI(IOA2)
0	1	Crystal mode OSCI or LIRC
1	0	Internal 8MHz RC or ERC
1	1	8 MHz IRCx2

Note: Please refer 2.3 for detail description.

T1EDG : TMR1 clock edge selection. This bit works only when external clock source TMCKI (IOA2) selected.
= 1, TMR1 decreased while external clock H→L (Falling edge).
= 0, TMR1 decreased while external clock L→H (Rising edge).

T1PS2:T1PS0 : TMR1 Prescaler selection

T1PS2	T1PS1	T1PS0	TMR1 Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.1.6.2 PWM1CON (PWM1 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
11h (r/w)	PWM1CON	T1MOD	PWM1S	EPWM1	-	PIR13	PIR12	PIR11	PIR10

Legend: - = unimplemented, read as '0'.

T1MOD : TMR1 operation mode select bit.
= 1, The TMR1 in PWM mode operation.
= 0, The TMR1 in Timer mode operation.

PWM1S : Initial State of PWM1 output duty.
= 1, Set the initial state to L, change to H when TMR1 duty underflow.
= 0, Set the initial state to H, change to L when TMR1 duty underflow.

EPWM1 : Extension PWM mode selection
= 1, PWM1 is Extension PWM mode.
= 0, PWM1 is normal PWM mode.
Note: Please refer to 2.4 for detail PWM description.

PIR13:PIR10 : Interrupt Event Rate of PWM1.
"1:N" means interrupt occurred after "N" PWM1 pulses.

PIR13 : PIR10	PWM1 Interrupt rate
0 0 0 0	1:1
0 0 0 1	1:2
0 0 1 0	1:3
0 0 1 1	1:4
|	|
1 1 0 1	1:14
1 1 1 0	1:15
1 1 1 1	1:16

2.1.6.3 T1LA (Timer1 Latch Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
12h (r/w)	T1LA	8-bit real-time timer/counter latch							

T1LA is a Timer1 pre-set latch buffer, see 2.3 for detail description.

2.1.6.4 T1CNT (Timer1 Counter Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
2Bh (r)	T1CNT	8-bit real-time timer/counter Count							

T1CNT is a Timer1 real-time counter, this register is only read, see 2.3 for detail description.

2.1.7 TMR2: 8-bit Timer & PWM2 Duty

The Timer2 is an 8-bit down count timer/counter which includes counter register (T2CNT), and latch register (T2LA). Please refer to 2.3 for detail Timer description.
The Timer2 can also be PWM2 and controlled by the register PWM2CON. Please refer to 2.4 for detail PWM description.

2.1.7.1 T2CON (Timer2 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
13h (r/w)	T2CON	T2EN	-	T2SO1	T2SO0	T2EDG	T2PS2	T2PS1	T2PS0

Legend: - = unimplemented, read as '0'.

T2EN : TMR2 Enable/Disable
= 1, TMR2 (PWM2) Enable.
= 0, TMR2 (PWM2) Disable.

T2SO1:T2SO0 : TMR2 clock source selection

T2SO1	T2SO0	TMR2 clock source
0	0	TMCKI(IOA2)
0	1	Crystal mode OSCI or LIRC
1	0	Internal 8MHz RC or ERC
1	1	8MHz IRCx2

Note: Please refer 2.3 for detail description.

T2EDG : TMR2 clock edge selection. This bit works only when external clock source TMCKI (IOA2) selected.
= 1, TMR2 decreased while external clock H→L (Falling edge).
= 0, TMR2 decreased while external clock L→H (Rising edge).

T2PS2:T2PS0 : TMR2 Prescaler selection

T2PS2	T2PS1	T2PS0	TMR2 Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.1.7.2 PWM2CON (PWM2 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
14h (r/w)	PWM2CON	T2MOD	PWM2S	EPWM2	-	PIR23	PIR22	PIR21	PIR20

Legend: - = unimplemented, read as '0'.

T2MOD : TMR2 operation mode select bit.
= 1, The TMR2 in PWM mode operation.
= 0, The TMR2 in Timer mode operation.

PWM2S : Initial State of PWM2 output duty.
= 1, Set the initial state to L, change to H when TMR2 duty underflow.
= 0, Set the initial state to H, change to L when TMR2 duty underflow.

EPWM2 : Extension PWM mode selection
= 1, PWM2 is Extension PWM mode.
= 0, PWM2 is normal PWM mode.
Note: Please refer to 2.4 for detail PWM description.

PIR23:PIR20 : Interrupt Event Rate of PWM2.
"1:N" means interrupt occurred after "N" PWM2 pulses.

PIR23 : PIR20	PWM2 Interrupt rate
0 0 0 0	1:1
0 0 0 1	1:2
0 0 1 0	1:3
0 0 1 1	1:4
|	|
1 1 0 1	1:14
1 1 1 0	1:15
1 1 1 1	1:16

2.1.7.3 T2LA (Timer2 Latch Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
15h (r/w)	T2LA	8-bit real-time timer/counter latch							

T2LA is a Timer2 pre-set latch buffer, see 2.3 for detail description.

2.1.7.4 T2CNT (Timer2 Counter Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
2Ch (r)	T2CNT	8-bit real-time timer/counter Count							

T2CNT is a Timer2 real-time counter, this register is only read, see 2.3 for detail description.

2.1.8 TMR3: 8-bit Timer

The Timer3 is an 8-bit down count timer/counter which includes counter register (T3CNT), and latch register (T3LA). Please refer to 2.3 for detail Timer description.

2.1.8.1 T3CON (Timer3 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
16h (r/w)	T3CON	T3EN	T3LOAD	T3SO1	T3SO0	T3EDG	T3PS2	T3PS1	T3PS0

T3EN : TMR3 Enable/Disable
= 1, TMR3 Enable.
= 0, TMR3 Disable.

T3LOAD : Enable/Disable Latch Buffer automatically load to counter register while writing to latch register
= 1, Enable TMR3 latch buffer automatically load to counter register while writing to latch register.
= 0, Disable TMR3 latch buffer automatically load to counter register while writing to latch register.
Note: This bit is only affected after latch register written. When the timer underflows, the latch register data will automatically load into counter register.

T3SO1:T3SO0 : TMR3 clock source selection

T3SO1	T3SO0	TMR3 clock source
0	0	TMCKI(IOA2)
0	1	Crystal mode OSCI or LIRC
1	0	Internal 8MHz RC or ERC
1	1	Not function, don't use.

Note: Please refer 2.3 for detail description.

T3EDG : TMR3 clock edge selection. This bit works only when external clock source TMCKI (IOA2) selected.
= 1, TMR3 decreased while external clock H→L (Falling edge).
= 0, TMR3 decreased while external clock L→H (Rising edge).

2.1.8.2 T3LA (Timer3 Latch Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
17h (r/w)	T3LA	8-bit real-time timer/counter latch							

T3LA is a Timer3 pre-set latch buffer, see 2.3 for detail description.

2.1.8.3 T3CNT (Timer3 Counter Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
18h (r)	T3CNT	8-bit real-time timer/counter Count							

T3CNT is a Timer3 real-time counter, this register is only read, see 2.3 for detail description.

T3PS2:T3PS0 : TMR3 Prescaler selection

T3PS2 : T3PS0			TMR3 Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.1.9 INTEN (Interrupt Mask Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
19h (r/w)	INTEN	GIE	ADCIE	PAIE	COMIE	-	T3IE	T2P2IE	T1P1IE

Legend: - = unimplemented, read as '0'.

GIE : Global interrupt enable bit.
= 1, Enable all un-masked interrupts.
= 0, Disable all interrupts.
Note : When an interrupt event occurred with the GIE bit and its corresponding interrupt enable bits are set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

ADCIE : ADC conversion completed interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

PAIE : PORTA interrupt enable
= 1, Enable interrupt.
= 0, Disable interrupt.

COMIE : LCD COM interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

T3IE : Timer3 underflow interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

T2P2IE : Timer2 / PWM2 underflow interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

T1P1IE : Timer1 / PWM1 underflow interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

2.1.10 INTFLAG (Interrupt Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
1Ah (r/w)	INTFLAG	-	ADCIF	PAIF	COMIF	-	T3IF	T2P2IF	T1P1IF

Legend: - = unimplemented, read as '0'.

ADCIF : ADC Interrupt flag. Set when ADC conversion is completed, reset by software.

PAIF : Port A <7:0> Interrupt flag. Set when pin changed on selected I/O by register INTPA, reset by software.

COMIF : LCD COM interrupt flag. Set when LCD clock overflows, and reset by software.

T3IF : TMR3 interrupt flag. Set when TMR3 underflows, and reset by software.

T2P2IF : TMR2 or PWM2 interrupt flag. Set when TMR2 underflows or PWM2 pulse counts to selected interrupt rate, and reset by software.

T1P1IF : TMR1 or PWM1 interrupt flag. Set when TMR1 underflows or PWM1 pulse counts to selected interrupt rate, and reset by software.

Note : BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).

2.1.11 ADCON1 (AD converter Control Register1)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
1Bh (r/w)	ADCON1	ADCEN	-	-	-	-	CHSL2	CHSL1	CHSL0

Legend: - = unimplemented, read as '0'.

ADCEN : ADC enable/disable setting
= 1, Enable.
= 0, Disable.
Note : This bit should be set by software and would be reset by hardware after the ADC end of conversion.

CHSL2:CHSL0 : ADC input channel select

CHSL2	CHSL1	CHSL0	Input channel
0	0	0	Channel 0, IOA0 pin
0	0	1	Channel 1, IOA1 pin
0	1	0	Channel 2, IOA2 pin
0	1	1	Channel 3, IOA3 pin
1	0	0	Channel 4, IOA4 pin
1	0	1	Channel 5, IOB4 pin
1	1	0	Channel 6, IOB5 pin
1	1	1	Channel 7, IOC7 pin

2.1.12 ADCON2 (AD converter Control Register2)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
1Ch (r/w)	ADCON2	-	-	-	-	-	-	CLKSL1	CLKSL0

Legend: - = unimplemented, read as '0'.

CLKSL1:CLKSL0 : ADC Conversion clock source select bits.

CKSL1	CKSL0	Conversion clock
0	0	System clock / 2 (fastest result, lowest quality)
0	1	System clock / 8
1	0	System clock / 32
1	1	System clock / 128 (slowest result, best quality)

Note : This clock is used to control the conversion precision and speed. The precision will be dropped off if faster conversion rate been used. The lowest conversion rate would be recommended in order to acquire most accurate data.

2.1.13 ADCON3 (AD converter Control Register3)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
1Dh (r/w)	ADCON3	-	-	-	-	ANISL3	ANISL2	ANISL1	ANISL0

Legend: - = unimplemented, read as '0'.

ANISL3:ANISL0 : Analog input select bits.

ANISL3	ANISL2	ANISL1	ANISL0	Analog input selection
0	0	0	0	All the ports are digital input
0	0	0	1	AN0
0	0	1	0	AN1
0	0	1	1	AN2
0	1	0	0	AN3
0	1	0	1	AN4
0	1	1	0	AN5
0	1	1	1	AN6
1	0	0	0	AN7
Other				No function, don't use.

Note : To minimize power consumption, all the I/O pins should be carefully managed before entering sleep mode.

2.1.14 ADDATL, ADDATH (AD conversion data high-byte and low-byte Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
1Eh (r)	ADDATL	D1	D0	-	-	-	-	-	-
1Fh (r)	ADDATH	D9	D8	D7	D6	D5	D4	D3	D2

Legend: - = unimplemented, read as '0'.

The ADDATL and ADDATH registers is ADC conversion result. When ADC conversion is completed, the result is loaded into ADDATL and ADDATH, the ADCEN bit will be cleared, and the ADCIF bit will be set (if ADCIE are set).

2.1.15 Software Controlled LCD Module

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
20h (r/w)	COMCON1	-	-	-	-	COM3E	COM2E	COM1E	COM0E
21h (r/w)	COMCON2	COMEN	-	-	COMIS1	COMIS0	COMCK2	COMCK1	COMCK0

Legend: - = unimplemented, read as '0'.

The pins IOB0~IOB3 on port B can be used as COM lines to drive an external LCD panels. To implement this function, the COMCON1 and COMCON2 registers used to setup the correct bias voltage on these pins.

2.1.15.1 COMCON1 (Software LCD COM Control Register1)

COM0E : IOB0 / COM0 Selection bit.
= 1, IOB0 is normal I/O.
= 0, IOB0 is COM0, 1/2 VDD output (in LCD mode).

COM1E : IOB1 / COM1 Selection bit.
= 1, IOB1 is normal I/O.
= 0, IOB1 is COM1, 1/2 VDD output (in LCD mode).

COM2E : IOB2 / COM2 Selection bit.
= 1, IOB2 is normal I/O.
= 0, IOB2 is COM2, 1/2 VDD output (in LCD mode).

COM3E : IOB3 / COM3 Selection bit.
= 1, IOB3 is normal I/O.
= 0, IOB3 is COM3, 1/2 VDD output (in LCD mode).

2.1.15.2 COMCON2 (Software LCD COM Control Register2)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
21h (r/w)	COMCON2	COMEN	-	-	COMIS1	COMIS0	COMCK2	COMCK1	COMCK0

Legend: - = unimplemented, read as '0'.

COMEN : COM module enable/disable bit.
= 1, Enable COM module.
= 0, Disable COM module.

COMIS1:COMIS0 : COMn operating current selection (VDD = 5V).

COMIS1	COMIS0	COMn operating current
0	0	25uA
0	1	50uA
1	0	100uA
1	1	200uA

COMCK2:COMCK0 : COMn turn-on time selection (interrupt).

COMCK2 : COMCK0			COMn Clock prescaler
0	0	0	System clock / 1024
0	0	1	System clock / 2048
0	1	0	System clock / 4096
0	1	1	System clock / 8192
1	0	0	System clock / 4
1	0	1	System clock / 8
1	1	0	System clock / 16
1	1	1	System clock / 32

2.1.16 SYSCLK (System Clock Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
22h (r/w)	SYSCLK	CLKS	-	-	-	-	-	IRCPD	ECLKPD

Legend: - = unimplemented, read as '0'.

The FM8P756 could be operated either dual or single clock system selected by configuration words. Please refer to 2.14 for detail configuration selection description. This register is used to control the switch between different system clocks and power-down function of those clocks.

CLKS : System Clock Selection (only valid in dual clock mode)
= 1, System Clock is External OSC/LIRC.
= 0, System Clock is Internal 8MHz or 4MHz RC.

IRCPD : Internal RC Power down Control (only valid in dual clock mode)
= 1, Internal 8MHz or 4MHz RC Power Down.
= 0, Internal 8MHz or 4MHz RC Power ON.
Note: Make sure the system clock been switch to external OSC/RC before power down internal 8MHz or 4MHz RC.

ECLKPD : External clock (OSC/LIRC) Power down Control (only valid in dual clock mode)
= 1, External OSC/LIRC Power Down.
= 0, External OSC/LIRC Power ON.
Note: Make sure the system clock been switch to internal 8MHz or 4MHz RC before power down external OSC/LIRC.

2.1.17 CLOCON (Clock output Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
23h (r/w)	CLOCON	CLOEN	-	EXCLK	DINV	DUTY	CLOPS2	CLOPS1	CLOPS0

Legend: - = unimplemented, read as '0'.

The FM8P756 provides one system clock output with prescaler function.

CLOEN : System Clock output function selection
= 1, IOA5 is Clock Output.
= 0, IOA5 is normal I/O.

EXCLK : External clock (IOA2/TMCKI) function selection
= 1, IOA2 is external clock input of timer.
= 0, IOA2 is normal I/O.

DINV : System Clock output Duty invert selection bit.
If DUTY bit = 1:
= 1, 1/4 duty output
= 0, keep 3/4 duty output

else:
Ignore.

DUTY : System Clock output duty selection bit.
= 1, 3/4 duty output.
= 0, 1/2 duty output.

CLOPS2:CLOPS0 : Clock Output prescaler setting

CLOPS2 : CLOPS0			Clock Output prescaler ratio	
			DUTY = 0	DUTY = 1
0	0	0	1:1	1:2
0	0	1	1:2	1:4
0	1	0	1:4	1:8
0	1	1	1:8	1:16
1	0	0	1:16	1:32
1	0	1	1:32	1:64
Other			No function, don't use.	

2.1.18 APHCON, BPHCON, CPHCON (Port A, Port B, Port C Pull-high Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
25h (r/w)	APHCON	-	PHA6	PHA5	PHA4	PHA3	PHA2	PHA1	PHA0
26h (r/w)	BPHCON	-	-	PHB5	PHB4	PHB3	PHB2	PHB1	PHB0
27h (r/w)	CPHCON	PHC7	PHC6	PHC5	PHC4	PHC3	PHC2	PHC1	PHC0

Legend: - = unimplemented, read as '0'.

Those registers are used to setup pull-high resistor enable/disable of each IO pins.
= 1, Pull-high resistor enable.
= 0, Pull-high resistor disable.

2.1.19 INTPA (Port A Interrupt / Wakeup control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
28h (r/w)	INTPA	PA7IEN	PA6IEN	PA5IEN	PA4IEN	PA3IEN	PA2IEN	PA1IEN	PA0IEN

This register is used to enable/disable the interrupt/wakeup function of Port A. Please refer to 2.8.1 for detail description of External Interrupt and Wake up function.
= 1, Selected IO interrupt/wakeup enable.
= 0, Selected IO interrupt/wakeup disable.

2.1.20 WDTCON (Watchdog Timer Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
29h (r/w)	WDTCON	WDTEN	I_WDT	I_TWDT	-	-	WDTPS2	WDTPS1	WDTPS0

Legend: - = unimplemented, read as '0'.

The FM8P756 builds in a watchdog timer with two different modes, normal watchdog reset and internal watchdog wakeup. The watchdog timer is controlled by this register (WDTCON). Please refer to 2.6 for detail Watchdog Timer description.

WDTEN : Watchdog Timer Enable/ Disable.
= 1, WDT Enable.
= 0, WDT disable.

I_WDT : Internal Watchdog Wakeup mode selection.
= 1, Internal Watchdog Wakeup Enable.
= 0, Internal Watchdog Wakeup Disable.

I_TWDT : Watchdog Timer Stable time required when operating in I_WDT mode (I_WDT bit = 1).
= 1, 1.25ms.
= 0, 5ms (default).

WDTPS2:WDTPS0 : Watchdog timer prescaler setting

WDTPS2 : WDTPS0			WDT prescaler rate
0	0	0	1:1 (20mS)
0	0	1	1:2 (40mS)
0	1	0	1:4 (80mS)
0	1	1	1:8 (160mS)
1	0	0	1:16 (320mS)
1	0	1	1:32 (640mS)
1	1	0	1:64 (1.28S)
1	1	1	1:128 (2.56S)

2.1.21 TAB_BNK (Table Look-up function Bank select Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
2Ah (r/w)	TB_BNK	-	-	-	-	-	BNK2	BNK1	BNK0

Legend: - = unimplemented, read as '0'.

The FM8P756 provides a table look-up function and the bank selection of ROM data is controlled by this register. Please refer to 2.10 for detail operation of look-up table function.

BNK2:BNK0 : Page selection of Look-up table

BNK2 : BNK0			BANK select
0	0	0	000 XXXX XXXX Table location
0	0	1	001 XXXX XXXX Table location
0	1	0	010 XXXX XXXX Table location
	|		|
1	1	1	111 XXXX XXXX Table location

2.1.22 ACC (Accumulator)

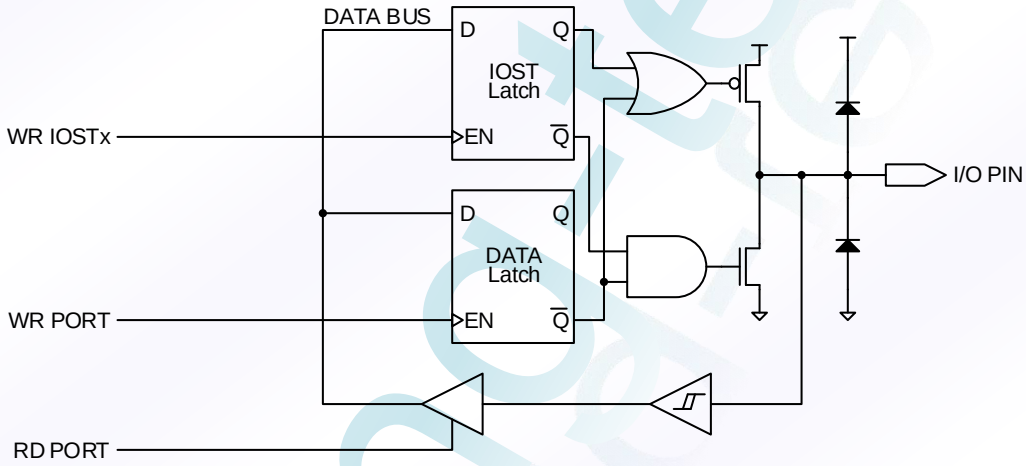
Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (r/w)	ACC	Accumulator							

Accumulator is an internal data transfer, or instruction operand holding. It cannot be addressed.

2.2 I/O Ports

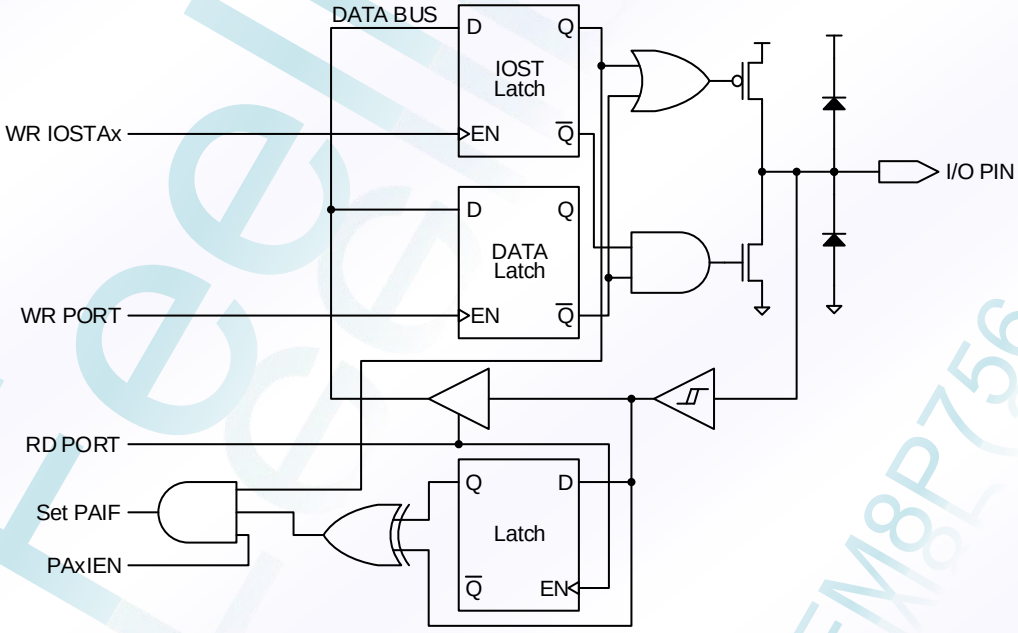
There are totally 21 bi-directional tri-state I/O ports and one (IOA7) input only. All I/O pins (IOA<6:0>, IOB<5:0> and IOC<7:0>) have specified data direction control registers (IOSTA, IOSTB and IOSTC) which can configure these pins as output or input.
All the IO pins can also enable or disable a weak internal pull-high by setting APHCON, BPHCON and CPHCON. This weak pull-high will be automatically turned off when the pin is configured as an output pin.
VR pin is reference voltage input pin of the ADC module, this pin does not have I/O function.
The Configuration Words can set IOA7 to Reset functions. When acting as Reset functions the pins will read as "0" during port read.
Please note, IOB2 and VR voltage on these pins must not exceed VDD, otherwise it will cause the pin breakdown.

Figure 2.3: Block Diagram of I/O Pins
IOB5, IOC7 ~ IOC0:



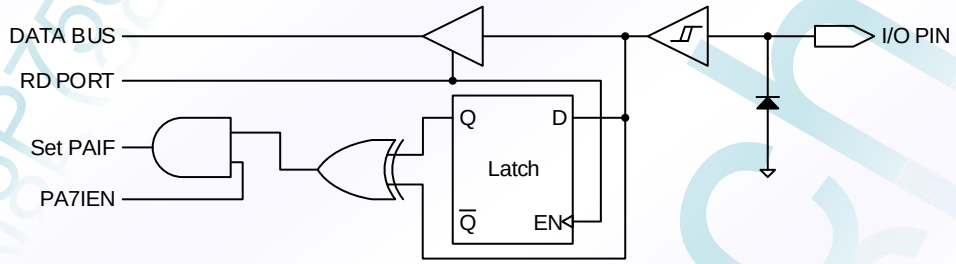
Pull-high / ADC / LCD are not shown in this figure

IOA6 ~ IOA0:



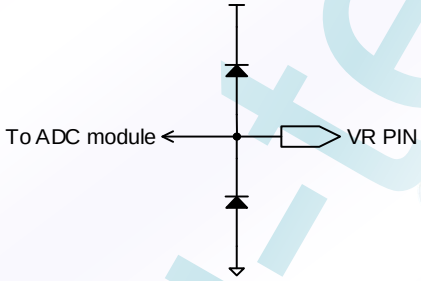
Pull-high/ADC/OSC are not shown in this figure

IOA7:



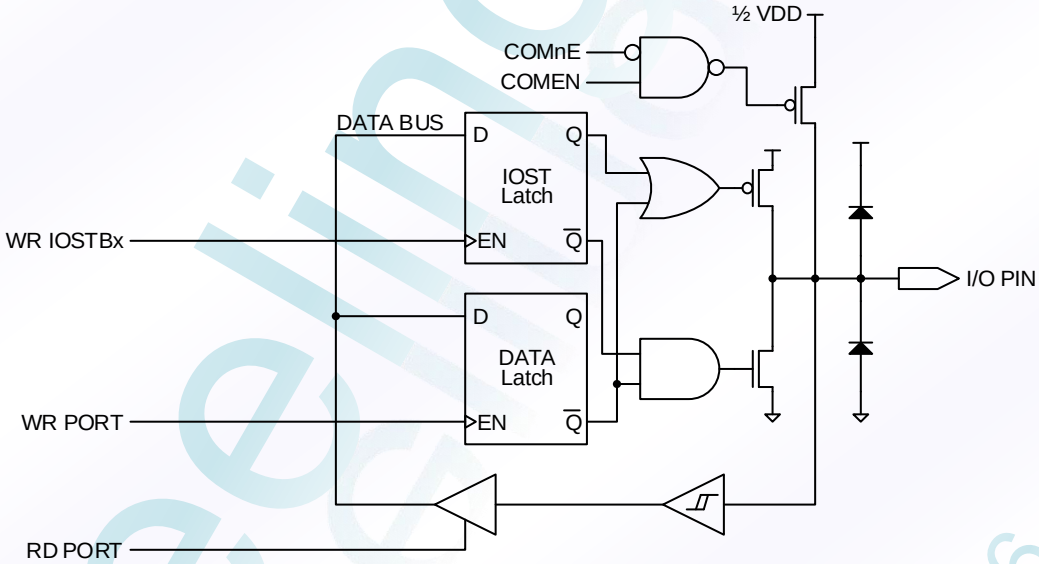
Voltage on this pin must not exceed VDD.

VR:



Voltage on this pin must not exceed VDD.

IOB0 ~ IOB3:

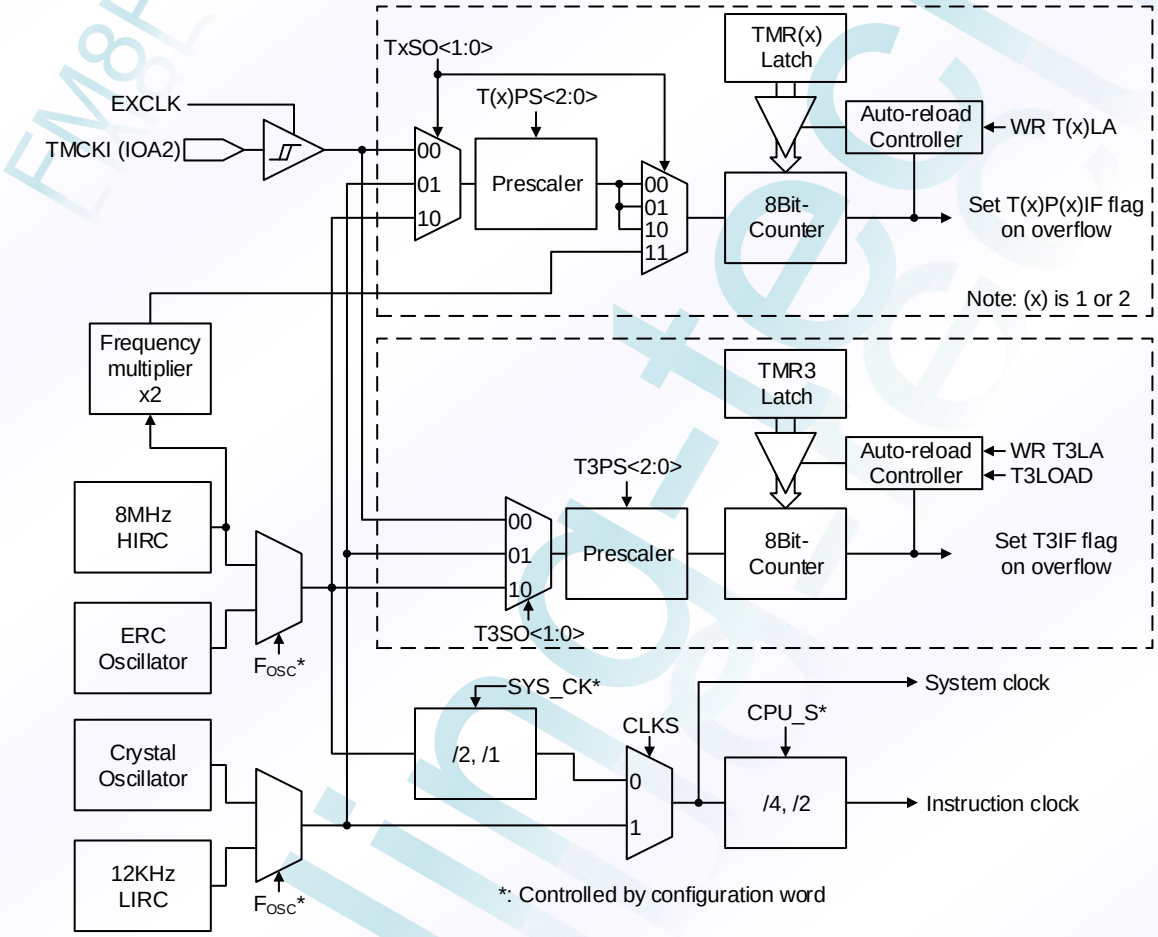


Pull-high is not shown in this figure

2.3 Timer/Event Counter (TMR1, TMR2, TMR3)

The FM8P756 contains three 8-bit down-counts Timers/Counters. All these timers have auto reload function, TMR1 and TMR2 can be to perform PWM function.

Figure 2.4: Simple Block Diagram of the Timer 1 ~ 3



2.3.1 Clock Source

Timer1 and Timer2 has four clock sources can be selected, Timer3 has three clock sources can be selected.

2.3.1.1 TMCKI (IOA2)

The event counter mode would be activated when the source of TMCKI (IOA2) used. At this mode, the rising/ falling edge of the event could also be selected separately.

2.3.1.2 Crystal or External RC Oscillator

In this mode, the timer clock source from Crystal / ERC oscillator module. Oscillator module operating modes are defined by the Fosc bit in the configuration word.
Please note that, in this case, the clock input to the timer in two paths, and therefore will have the following composition:

Table 2.1: Selection of Timer 1 ~ 3 Clock source

Fosc mode of Configuration word	Timer 1 ~ 3 Clock
HIRC	Only HIRC 8 MHz
HIRC & LIRC	HIRC 8 MHz or LIRC 12 KHz
HIRC & XT or HIRC & LF	HIRC 8 MHz or Crystal oscillator source
ERC	Only External RC oscillator source
LIRC	Only LIRC 12 KHz
XT or LF	Only Crystal oscillator source

Since the oscillator module is controlled by the FOSC bit, if need a combination of multiple clock sources, the need to carefully choose the configuration word FOSC operating mode.

2.3.1.3 Internal 8MHz RC Oscillator

In this mode, timer clock source from internal 8MHz RC oscillator. Please note that this clock source can only be used in the following modes:

Table 2.2: Selection of 8 MHz HIRC clock source

Fosc mode of Configuration word	Timer 1 ~ 3 Clock
HIRC	HIRC 8 MHz can be selected
HIRC & LIRC	
HIRC & XT or HIRC & LF	
ERC or LIRC or XT or LF	HIRC 8 MHz are shutdown

2.3.1.4 Internal 8MHz RC Oscillator *2

In this mode, the IRC frequency is multiplied by 2, as the timer clock source, this clock source using the same Opportunity and Table 2.2.

Note : This mode only for Timer1 and Timer2.

2.3.2 Prescaler

Each timer contains a 3-bits prescaler which can scale the timer or counter from 1:1 to 1:128.

TxPS2	TxPS1	TxPS0	TMRx Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.4 Pulse Width Modulation (PWM)

FM8P756 provides two PWM output shared with TMR1 and TMR2. When PWM1 or PWM2 selected, TMR1/TMR2 will be the duty of PWM1/PWM2.
PWM1 and PWM2 period is fixed resolution of 8-bits; duty time output a maximum resolution of 8-bits (normal mode) or 6-bits (extended mode).
The PWM outputs are on the IOA4/ADC4/INT4/PWM1, and IOB4/ADC5/PWM2 pins.
The user needs to set the T1MOD bit (PWM1CON<7>) to enable the PWM1 output. When T1MOD bit is set, the IOA4/ADC4/INT4/PWM1 pin is configured as PWM1 output and forced as an output, irrespective of the data direct bit (IOSTA<6>). When the T1MOD is clear, the pin behaves as a I/O pin.
Similarly, the T2MOD bit (PWM2CON<7>) controls the configuration of the IOB4/ADC5/PWM2 pin.

The FM8P756 PWM has two modes of operation; PWM1 and PWM2 have normal mode, and the extension mode, detailed description as follows:

2.4.1 Normal PWM mode

In the Normal PWM mode, it is a general purpose PWM mode; this mode can be used in the PWM1 and PWM2.

The PWM1 period time is fixed; period time can be calculated as follows:

$$\text{Period time of PWM1} = 256 * \text{TMR1 Prescal rate} * \frac{1}{\text{Clock source frequency}}$$

The duty cycle of PWM1 is determined by the 8-bit value T1LA, PWM1 duty time is as follows:

$$\text{Duty time of PWM1} = (\text{T1LA}+1) * \text{TMR1 Prescal rate} * \frac{1}{\text{Clock source frequency}}$$

or

$$\text{T1LA} = \frac{\text{Duty time} * \text{Clock source frequency}}{\text{TMR1 Prescal rate}}$$

PWM1 and PWM2 structure is the same. Therefore, these formulas can be used directly in PWM2.

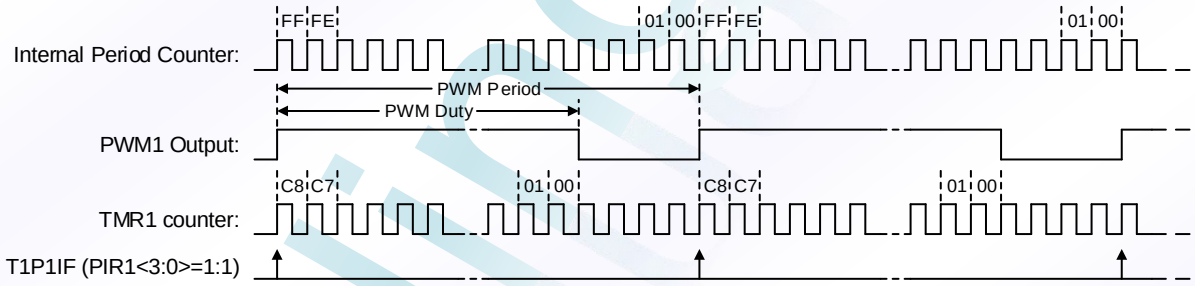
Example 2.2: PWM1 Setting (Normal mode)

Address	Code			
NA	#include	<8P756.ASH>		
		…		
		//Set PWM1 Duty		
n		MOVIA	0x32	
n+1		MOVAR	T1CON	;CLK source is Crystal, Prescaler 1:4
				;Period time = 256*4*(1/16MHz) = 64uS
n+2		MOVIA	0x80	
n+3		MOVAR	PWM1CON	;Set to Normal PWM, interrupt rate 1:1
n+4		MOVIA	0xC8	
n+5		MOVAR	T1LA	;Set Duty (0xC8 down count to 0x00)
				;Duty time = (0xC8+1)*4*(1/16MHz) = 50.25uS
n+6		BSR	T1CON,T1EN_B	;Start PWM1
		//Interrupt setting, not required		
n+7		MOVIA	0x81	
n+8		MOVAR	INTEN	;Enable global & PWM1 interrupt
n+9		MOVIA	0x76	;Clear interrupt flag
n+10		MOVAR	INTFLAG	;Clear T1P1IF(PWM1) flag

Note: 1. The PWM duty (F_{OSC}/255 max) must be smaller than PWM period (F_{OSC}/256). In this example, the frequency of external OSC is approximately 16MHz.

2. The PWM duty has built-in controller circuit, user can directly change, and the new value will be automatically loaded to the next cycle.

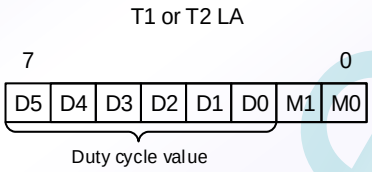
Figure 2.5: Normal PWM Output Waveform



2.4.2 Extension PWM mode

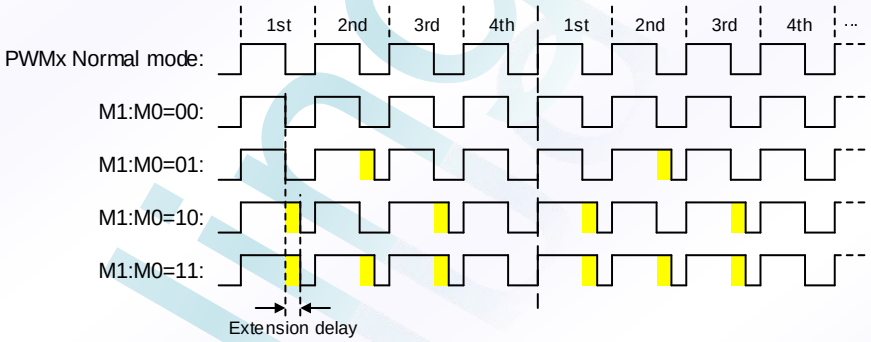
In the extension PWM mode, PWM module will increase the delay to Duty cycle. This mode has three modes, can be select by T1LA <1:0> (PWM1) or T2LA <1:0> (PWM2). Therefore, in the extension mode, duty cycle maximum resolution is 6-bits.
The PWM1 or PWM2 duty cycle is set by T1LA <7:2> or T2LA <7:2>.
This mode can be used in the PWM1 and PWM2.

Figure 2.6: T1 or T2 LA bits allocation in the Extension PWM mode



M1 : M0		Stretched cycle number
0	0	None (Same as Normal mode)
0	1	Only 2nd
1	0	1st and 3rd
1	1	1st, 2nd and 3rd

Figure 2.7: Extension PWM Output Waveform



Extension mode duty time can be calculated as follows:

$$\text{Duty time of PWM1} = (\text{T1LA}+1) * \text{TMR1 Prescal rate} * \frac{1}{\text{Clock source frequency}}$$

or

$$\text{T1LA} = \frac{\text{Duty time} * \text{Clock source frequency}}{\text{TMR1 Prescal rate}}$$

Extension delay time is as follows:

$$\text{Extension delay time} = \text{TMR1 Prescal rate} * \frac{1}{\text{Clock source frequency}}$$

PWM1 and PWM2 structure is the same. Therefore, these formulas can be used directly in PWM2.

Example 2.3: PWM1 Setting (Extension mode)

Address	Code			
NA	#include	<8P756.ASH>		
		…		
		//Set PWM1 Duty		
n		MOVIA	0x32	
n+1		MOVAR	T1CON	;CLK source is Crystal, Prescaler 1:4
				;Period time = 256*4*(1/16MHz) = 64uS
n+2		MOVIA	0xA0	
n+3		MOVAR	PWM1CON	;Set to Extension PWM, interrupt rate 1:1
n+4		MOVIA	0xC9	
n+5		MOVAR	T1LA	;Set Duty (0x32 down count to 0x00)
				;Duty time = (0x32+1)*4*(1/16MHz) = 12.75uS
n+6		BSR	T1CON,T1EN_B	;Start PWM1
		//Interrupt setting, not required		
n+7		MOVIA	0x81	
n+8		MOVAR	INTEN	;Enable global & PWM1 interrupt
n+9		MOVIA	0x76	;Clear interrupt flag
n+10		MOVAR	INTFLAG	;Clear T1P1IF(PWM1) flag

Note: 1. The PWM duty (F_{OSC}/255 max) must be smaller than PWM period (F_{OSC}/256). In this example, the frequency of external OSC is approximately 16MHz.

2. The PWM duty has built-in controller circuit, user can directly change, and the new value will be automatically loaded to the next cycle.

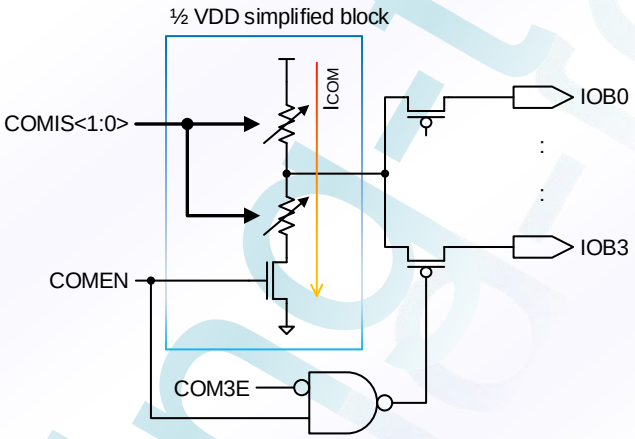
2.5 Software controlled LCD

The FM8P756 have the software controlled LCD driving external LCD panels. The common pins for LCD driving, COM0~COM3, are pin shared with certain pin on IOB0~IOB3 port. The LCD signals (COM and SEG) are generated using the application program.
The LCD driver function is controlled using the COMCON1 and COMCON2 to controlling the overall on/off function, Also controls the bias voltage setup function. This enables the LCD COM driver to generate the necessary VDD/2 voltage levels for LCD 1/2 bias operations.

2.5.1 1/2 VDD Bias

The chip provides 1/2 VDD bias in IOB0 ~ IOB3. User needs to set the COMIS<1:0> bits set I_{COM} current. To make the I/O Output 1/2 VDD bias, must be setting COMEN bit to “1”.
When COMEN bit is "1", COM0E direct control IOB0 pin, users only need to control IOB0 and COM0E two bits, IOSTB0 does not affect the status of IOB0.
Similarly, COM3E ~ COM1E bits control the corresponding IOB3 ~ IOB1 pin.

Figure 2.8: Simplified Block Diagram of COM pins



IOB0~IOB2 some circuit are not shown in this figure

Table 2.3: COM 3~0 Pin Function

COMEN	COMnE	Pin Function	IOB3 ~ 0
0	X	I/O	0 or 1
1	0	COMn	1/2 VDD
1	1	I/O	0 or 1

Note: In the case of unused, the user must turn-off 1/2 VDD bias (setting COMEN bit to “0”), reducing current consumption.

2.5.2 COMCK

The chip provides one set of dividers can be set, the user can use this divider to generate an interrupt triggers signal to generate LCD waveform by software program. If this interrupt source used in another application, COMEN bit must be set to "1".

2.6 Watch Dog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. So the WDT will still run even if the clock on the OSCI and OSCO pins is turned off, such as in SLEEP mode.
The WDT can be disabled by clearing the control bit WDTEN (WDTCON <7>) to "0".

The WDT has a typical time-out period of 20 mS (without prescaler). This period of this timer may be variant slightly because of temperature, voltage, and process variation. If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT controlled by the WDTCON register <2:0>. Thus, the longest time-out period is approximately 2.56 seconds.
The CLRWDT instruction clears the WDT and prevents it from timing out and generating a device reset.
The SLEEP instruction also resets the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

There are two type of watchdog timer mode could be selected by I_WDT (WDTCON <6>). When I_WDT bit disable, normal watchdog timer reset is selected. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset and the $\overline{TO}$ bit (STATUS<4>) will be cleared.
If I_WDT bit enabled, the internal watchdog timer wakeup will be used. The system wakeups from sleep, then jumps into interrupt vector with external interrupt request PAIF (INTFLAG<5>) and continues from next instruction instead of triggering a reset event. There is a stabilization time required for internal watchdog wakeup could be selected by I_ TWDT (WDTCON<5>). The default value of this stabilization timer is 5ms.

Example 2.4: Internal Watchdog Wakeup

Address	Code			
NA	#include	<8P756.ASH>		
0x003		…		
0x004		… (Backup status code)		1. WDT Wakeup
		…		;User WDT Wakeup ISR code
		MOVIA	0x57	
		MOVAR	INTFLAG	;Clear PAIF flag(Note1)
		… (Restore status code)		
		RETFIE		
		2. Return from ISR		
n		MOVIA	0xA0	
n+1		MOVAR	INTEN	;Enable global & Port A interrupt
n+2		CLRWDT		
n+3		MOVIA	0xE7	
n+4		MOVAR	WDTCON	;Sleep: 2.56S + Wakeup: 5mS
n+5		…		
n+6		…		
n+7		SLEEP		
n+8		NOP		
		…		

Note : 1. BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).
2. Interrupt backup / restore status code are not shown in this example.

Example 2.5: Typical Watchdog Reset

Address	Code			
NA	#include	<8P756.ASH>		
0x000		…		
		…		WDT Reset
n		CLRWDT		
n+1		MOVIA	0x87	
n+2		MOVAR	WDTCON	;Sleep: 2.56S + Wakeup:20mS
n+3		…		
n+4		…		
n+5		SLEEP		
n+6		NOP		
n+7		…		
n+8		…		

2.7 Reset

FM8P756 device may be RESET in one of the following ways:

1. Power-on Reset (POR)
2. Brown-out Reset (BOR)
3. RSTB Pin Reset
4. WDT time-out Reset

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a “reset state” on Power-on Reset, RSTB or WDT Reset.

A Power-on RESET pulse is generated on-chip when Vdd rise is detected. To use this feature, the user merely ties the RSTB pin to Vdd.

On-chip Low Voltage Detector (LVDT) places the device into reset when Vdd is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation Vdd range. Brown-out RESET is typically used in AC line or heavy loads switched applications.

A RSTB or WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

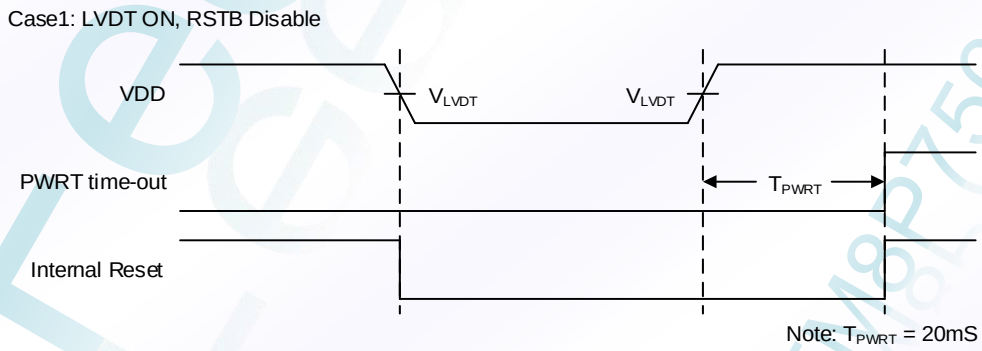
The $\overline{TO}$ and $\overline{PD}$ bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

2.7.1 Power-up Reset Timer(PWRT)

The Power-up Reset Timer provides a nominal 20ms delay after Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset. The device is kept in reset state as long as the PWRT is active.

The PWDT delay will vary from device to device due to Vdd, temperature, and process variation.

Figure 2.9: Reset Timing



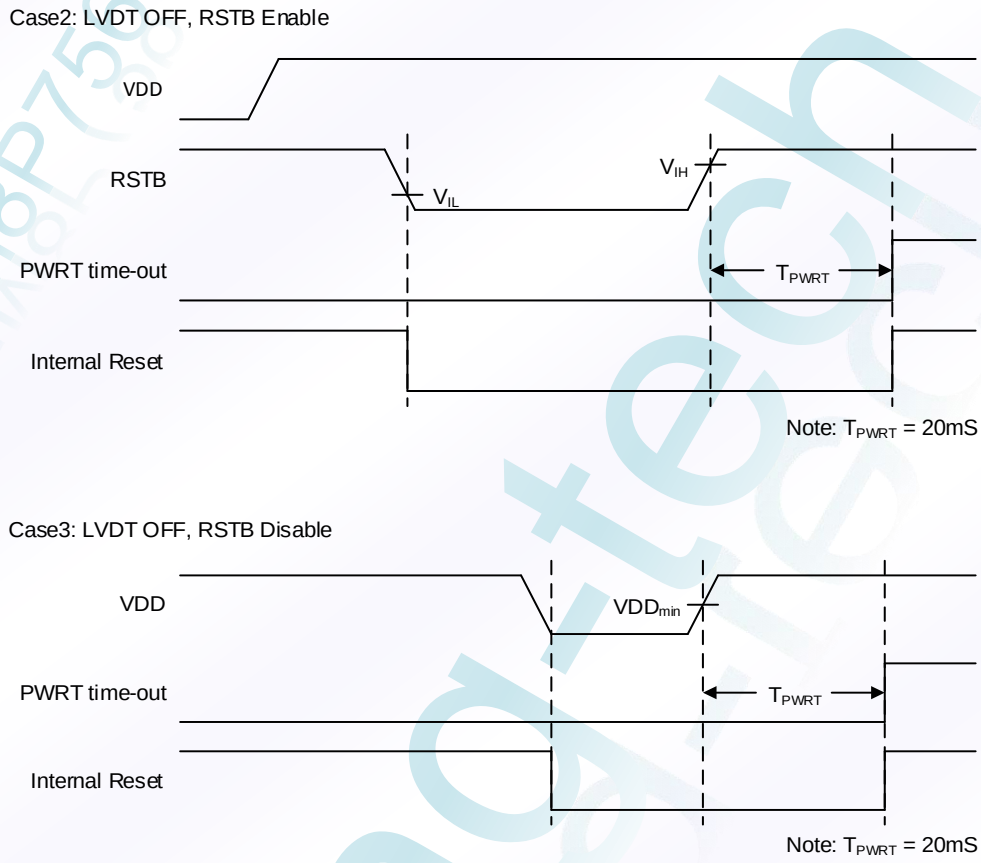


Figure 2.10: Simplified Block Diagram of on-chip Reset Circuit

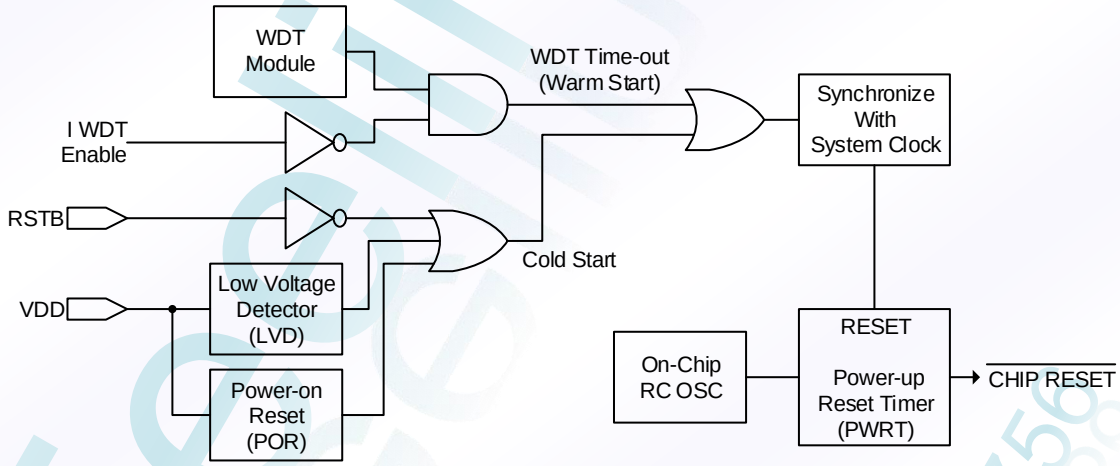


Table 2.4: Reset Conditions for Operational Registers

Register	Address	Power-on Reset Brown-out Reset	WDT Reset RSTB Reset
ACC	N/A	xxxx xxxx	uuuu uuuu
INDF	00h	xxxx xxxx	uuuu uuuu
PCL	01h	0000 0000	0000 0000
PCHBUF	02h	---- -000	---- -000
STATUS	03h	---1 1xxx	---# #xxx
FSR	04h	xxxx xxxx	uuuu uuuu
IOSTA	05h	-111 1111	-111 1111
PORTA	06h	xxxx xxxx	uuuu uuuu
IOSTB	07h	--11 1111	--11 1111
PORTB	08h	--xx xxxx	--uu uuuu
IOSTC	09h	1111 1111	1111 1111
PORTC	0Ah	xxxx xxxx	uuuu uuuu
T1CON	10h	0-00 0000	0-00 0000
PWM1CON	11h	000- 0000	000- 0000
T1LA	12h	1111 1111	1111 1111
T2CON	13h	0-00 0000	0-00 0000
PWM2CON	14h	000- 0000	000- 0000
T2LA	15h	1111 1111	1111 1111
T3CON	16h	0-00 0000	0-00 0000
T3LA	17h	1111 1111	1111 1111
T3CNT	18h	1111 1111	1111 1111
INTEN	19h	0000 -000	0000 -000
INTFLAG	1Ah	-000 -000	-000 -000
ADCON1	1Bh	0--- -000	0--- -000
ADCON2	1Ch	---- --00	---- --00
ADCON3	1Dh	---- 0000	---- 0000
ADDATL	1Eh	00-- ----	00-- ----
ADDATH	1Fh	0000 0000	0000 0000
COMCON1	20h	---- 0000	---- 0000
COMCON2	21h	0--0 0000	0--0 0000
SYSCLK	22h	0--- --00	0--- --00
CLOCON	23h	0-00 0000	0-00 0000
APHCON	25h	-000 0000	-000 0000
BPHCON	26h	--00 0000	--00 0000
CPHCON	27h	0000 0000	0000 0000
INTPA	28h	0000 0000	0000 0000
WDTCON	29h	100- -111	100- -111
TAB_BNK	2Ah	---- -000	---- -000
T1CNT	2Bh	1111 1111	1111 1111
T2CNT	2Ch	1111 1111	1111 1111
General Purpose Registers	40h ~ 9Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, # = refer to the following table for possible values.

Table 2.5: $\overline{TO}$ and $\overline{PD}$ Status after Reset

$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	0	WDT timer overflow from sleep mode
0	1	WDT timer overflow from normal mode
1	0	Set ‘low” at RESETB from sleep mode
1	1	Power on reset
u	u	Set “low” at RESETB from normal mode

Legend: u = unchanged.

Table 2.6: $\overline{TO}$ and $\overline{PD}$ Status after Reset

Event	$\overline{TO}$	$\overline{PD}$
Power-on	1	1
WDT Time-out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Legend: u = unchanged.

2.8 Interrupt

The FM8P756 has four kinds of interrupt sources:
1. 8 External IOA<0:7> pin changed interrupt
2. 3 Timers underflow interrupt (or PWM interrupt)
3. ADC conversion completion interrupt
4. LCD COM interrupt

INTFLAG is the interrupt flag register that recodes the interrupt requests to the relative flags.
A global interrupt enable bit, GIE (INTEN<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be enabled/ disabled through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.
When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts, and the next instruction will be fetched from address 004h. The interrupt flag bits must be cleared by software before re-enabling GIE bit to avoid recursive interrupts.
The RETFIE instruction exits the interrupt routine and set the GIE bit to re-enable interrupt.
The flag bit in INTFLAG register is set by interrupt event regardless of the status of its mask bit.

2.8.1 PORTA<0:7> External Interrupt and Wakeup Function

The external interrupt on PORTA<0:7> are selected by INTPA<0:7> and PAIE (INTEN<5>). When the device is in normal mode and the specified IO status changed, the interrupt event will be triggered and the program will jump to 004h.
When the device is in sleep mode, those interrupts can also be used as an external wakeup signal. The device will restart system clock and the program will jump to 004h after startup timer timeout.

Example 2.6: External IOA0 pin change interrupt

Address	Code		
NA	#include	<8P756.ASH>	
0x003	…		1. IOA0 pin change
0x004	… (Backup status code)		
	…		;User Port A pin change ISR code
	MOVIA	0x57	
	MOVAR	INTFLAG	;Clear PAIF flag(Note1)
	… (Restore status code)		
	RETFIE		
	2. Return from ISR		
n	MOVIA	0xFF	
n+1	MOVAR	IOSTA	;Set Port A as input
n+2	MOVIA	0xA0	
n+3	MOVAR	INTEN	;Enable global & Port A interrupt
n+4	MOVIA	0x57	
n+5	MOVAR	INTFALG	;Clear PAIF flag(Note1)
n+6	MOVR	PORTA,A	;Update Port A pin status
n+7	MOVIA	0x01	
n+8	MOVAR	INTPA	;Set IOA0 pin change
	…		
	…		
	…		

Note : 1. BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).
2. Interrupt backup / restore status code is not shown in this example.

Example 2.7: External IOA0 pin change wakeup interrupt

Address	Code		
NA	#include	<8P756.ASH>	
0x003	…		
0x004	… (Backup status code)		1. IOA0 pin change
	…		; User Port A pin change wakeup ISR code
	MOVIA	0x57	
	MOVAR	INTFLAG	;Clear PAIF flag(Note1)
	… (Restore status code)		
	RETFIE		
	2. Return from ISR		
n	MOVIA	0xFF	
n+1	MOVAR	IOSTA	;Set Port A as input
n+2	MOVIA	0xA0	
n+3	MOVAR	INTEN	;Enable global & Port A interrupt
n+4	MOVIA	0x57	
n+5	MOVAR	INTFALG	;Clear PAIF flag(Note1)
n+6	MOVR	PORTA,A	;Update Port A pin status
n+7	MOVIA	0x01	
n+8	MOVAR	INTPA	;Set IOA0 pin change wakeup
n+9	SLEEP		
n+10	NOP		
	…		

Note : 1. BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).
2. Interrupt backup / restore status code is not shown in this example.

2.8.2 Timer1~3 Interrupt's

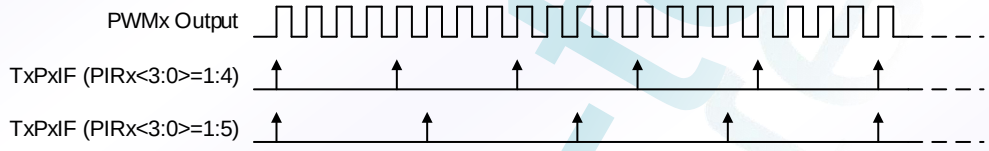
2.8.2.1 Timer 1 interrupt

At Timer mode, an underflow (00h → FFh) in the TMR1 counter will set the flag bit T1P1IF (INTFLAG<0>).
At PWM mode, the end of each PWM period cycle to generate an interrupt. The interrupt rate can be adjusted by PWM1CON <3:0>. See Figure 2.11 for detail description.
The T1P1IF bit can be cleared by software. This interrupt can be disabled by clearing T1P1IE bit (INTEN<0>).

2.8.2.2 Timer 2 interrupt

At Timer mode, an underflow (00h → FFh) in the TMR2 counter will set the flag bit T2P2IF (INTFLAG<1>).
At PWM mode, the end of each PWM period cycle to generate an interrupt. The interrupt rate can be adjusted by PWM2CON <3:0>. See Figure 2.11 for detail description.
The T2P2IF bit can be cleared by software. This interrupt can be disabled by clearing T2P2IE bit (INTEN<1>).

Figure 2.11: PWM Interrupt Waveform



2.8.2.3 Timer 3 interrupt

An underflow (00h → FFh) in the TMR3 counter will set the flag bit T3IF (INTFLAG<2>). And the T3IF bit can be cleared by software. This interrupt can be disabled by clearing T3IE bit (INTEN<2>).

2.8.3 ADC conversion completion interrupt

When the A/D conversion is completed, the flag bit ADCIF (INTFLAG <6>) will be set. And the ADCIF bit can be cleared by software. This interrupt can be disabled by clearing ADCIE bit (INTEN<6>).

2.8.4 LCD COM interrupt

When the divider overflow occurs, the flag bit COMIF (INTFLAG <4>) will be set. And the COMIF bit can be cleared by software. This interrupt can be disabled by clearing COMIE bit (INTEN<4>).

2.9 Analog to Digital Converter (ADC)

This analog to digital converter has 8 channels 10bits (8+2) resolution. The ADC is controlled by three control register, ADCON1, ADCON2, and ADCON3.

Example 2.8: Analog to Digital Conversion (Channel0 AD conversion)

Address	Code			
NA	#include	<8P756.ASH>		
		…		
n		BTRSC	ADCON1,ADCEN_B	
n+1		GOTO	$-1	; Make Sure no ADC is processing
n+2		MOVIA	0x37	
n+3		MOVAR	INTFLAG	; Clear ADCIF flag(Note)
n+4		MOVIA	0x00	
n+5		MOVAR	ADCON1	; Select ADC Channel 0 (IOA0) conversion
n+6		MOVIA	0x03	
n+7		MOVAR	ADCON2	; Set AD conversion rate: System clock / 128
n+8		MOVIA	0x01	
n+9		MOVAR	ADCON3	; Set AN0 analog input
n+10		BSR	ADCON1,ADCEN_B	; ADC conversion start
n+11		BTRSS	INTFLAG,ADCIF_B	
n+12		GOTO	$-1	; Wait AD end of conversion
n+13		MOVR	ADDATH,A	; Read ADC high byte data
n+14		MOVAR	…	; Transfer ADC value to other register.
n+15		MOVR	ADDATL,A	; Read ADC low byte data
n+16		MOVAR	…	; Transfer ADC value to other register.
		…		

Note : BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).

2.10 Look-Up Table Function

The Look-up Table function is built-in to access the data table within entire ROM area. The TAB_BNK register is used to address the high byte of the location of required ROM. The instructions TABL and TABH are used to read low byte and high byte of the addressed ROM. The result of instructions will be stored at ACC register. Please refer to the following example for detail.

Example 2.9: Look-up Table

Address	Code			
NA	#include	<8P756.ASH>		
		…		
n		MOVIA	0x03	
n+1		MOVAR	0x5B	;Save offset value 03H to register 0x5B (low bit address)
n+2		MOVIA	0x07	
n+3		MOVAR	TAB_BNK	; Save offset value 07H to TAB_BNK (high bit address)
n+4		TABL	0x5B	; Read Low byte 0x703 ROM Data, and saved
				; it to ACC. (ACC=0xAA)
n+5		MOVAR	….	; Transfer value to other register.
n+6		TABH	0x5B	; Read High byte 0x703 ROM Data, and saved
				; it to ACC. (ACC=0x55)
n+7		MOVAR	…	; Transfer value to other register.
n+8		…		
0x700		DW	0x1122	
0x701		DW	0x3344	
0x702		DW	0x5566	
0x703		DW	0x55AA	
…		…		

Required sequence

2.11 Hexadecimal Convert to Decimal (HCD)

Decimal format is another number format for FM8P756. When the content of the data memory has been assigned as decimal format, it is necessary to convert the results to decimal format after the execution of ALU instructions. When the decimal converting operation is processing, all of the operand data (including the contents of the data memory (RAM), accumulator (ACC), immediate data, and look-up table) should be in the decimal format, or the results of conversion will be incorrect.
Instruction DAA can convert the ACC data from hexadecimal to decimal format after any addition operation and restored to ACC.
The conversion operation is illustrated in Example 2.10.

Example 2.10: DAA CONVERSION

Address	Code			
NA	#include	<8P756.ASH>		
n		…		
n+1		MOVIA	0x90	;Set immediate data = decimal format number “90” (ACC ← 90h)
n+2		MOVAR	0x40	;Load immediate data “90” to data memory address 40H
n+3		MOVIA	0x10	;Set immediate data = decimal format number “10” (ACC ← 10h)
n+4		ADDAR	0x40,A	;Contents of the data memory address 40H and ACC are binary-added
				;the result loads to the ACC (ACC ← A0h, C ← 0)
n+5		DAA	0x40,A	;Convert the content of ACC to decimal format, and restored to ACC
				;The result in the ACC is “00” and the carry bit C is “1”. This represents
				;the decimal number “100”
n+6		…		

Instruction DAS can convert the ACC data from hexadecimal to decimal format after any subtraction operation and restored to ACC.
The conversion operation is illustrated in Example 2.11.

Example 2.11: DAS CONVERSION

Address	Code			
NA	#include	<8P756.ASH>		
n		…		
n+1		MOVIA	0x10	;Set immediate data = decimal format number “10” (ACC ← 10h)
n+2		MOVAR	0x40	;Load immediate data “90” to data memory address 40H
n+3		MOVIA	0x20	;Set immediate data = decimal format number “20” (ACC ← 20h)
n+4		SUBAR	0x40,A	;Contents of the data memory address 40H and ACC are binary-subtracted
				;the result loads to the ACC (ACC ← F0h, C ← 0)
n+5		DAS	0x40,A	;Convert the content of ACC to decimal format, and restored to ACC
				;The result in the ACC is “90” and the carry bit C is “0”. This represents
				;the decimal number “ -10”
n+6		…		

2.12 Dual Clock Function

The chip can be operated in three different dual clock function, users need to use it, and the configuration word must be set to one of following:

- HIRC & LIRC
- HIRC & XT
- HIRC & LF

If not in these states, will not be able to use dual clock function. By default, the system is the use of internal HIRC frequency as the clock source, and the two oscillator circuit is in the enable state. If not used, turn off unused oscillator power (via SYSCLK), can be reduce unnecessary current consumption.
When you want to switch clock source, recommend follow these steps:

1. Turn-on another oscillator power.
2. Wait oscillator to stable (XT and LF mode requires this step).
3. Set WDT prescaler to 1:128 and Clear Watch-dog (avoid watchdog overflow).
4. Set or Clear CLKS bit (SYSCLK <7>) to switch to another clock source.
5. Wait two NOP instruction (Required sequence).
6. Clear Watch-dog and set back to original settings.
7. If original oscillator not used, turn-off it.

Since the oscillator from the off state to the normal output clock oscillator needs some time to wait for a stable, at each oscillation mode, we recommend waiting time should be greater than the following table:

Table 2.7: Recommend typical wait time

Situation	Typical waiting time
Crystal → HIRC	10uS
HIRC → Crystal (4 to 20 MHz)	1.5mS
HIRC → Crystal (32 KHz)	5 ~ 370mS
HIRC → LIRC	1.5mS

Note: 1. This table is for reference only.
2. Quartz crystal characteristics vary according to type, package and manufacturer, the users must be carefully tested and verified.
3. RC oscillator mode will change depending on the operating voltage, the user must carefully tested and verified.

Example 2.12: Switching from HIRC to External clock (or LIRC)

Address	Code			
NA	#include	<8P756.ASH>		
		…		
n		BCR	SYSCLK,ECLKPD_B	;Turn-on External oscillator
n+1		CALL	Delay	;Wait Crystal oscillator to stable
		MOVIA	0x87	
		MOVAR	WDTCON	;If Watch-dog enable, recommend set to 1:128
n+2		CLRWDT		;If Watch-dog enable, clean it!
n+3		BSR	SYSCLK,CLKS_B	;Switching from HIRC to External clock
n+4		NOP		Required sequence
n+5		NOP		
n+6		CLRWDT		;If Watch-dog enable, clean it!
n+7		BSR	SYSCLK,IRCPD_B	;Turn-off HIRC oscillator (if unused)
n+8		MOVIA	0xnn	
n+9		MOVAR	WDTCON	;Set back original settings (if Watch-dog used)
		…		

Similarly, switching from External clock (or LIRC) to HIRC also this procedure.

2.13 Oscillator Configurations

FM8P756 can be operated in five different combinations of oscillator modes. Users can program Configuration Words (F_{OSC}) to select the appropriate modes. The five different system clock modes are combination of the following oscillators:

- LF: Low Frequency Crystal Oscillator
- XT: Crystal/Resonator Oscillator
- ERC: External Resistor/ Voltage Controlled Oscillator
- HIRC: High speed Internal Resistor/Capacitor Oscillator
- LIRC: Low speed Internal Resistor/Capacitor Oscillator

In LF, or XT modes, a crystal or ceramic resonator in connected to the OSCI and OSCO pins to establish oscillation. When in LF, or XT modes, the devices can have an external clock source drive the OSCI pin.
The ERC device option offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext), the operating temperature, and the process parameter.
The IRC option offers largest cost savings for timing insensitive applications.

Figure 2.12: XT or LF Oscillator Modes (Crystal Operation or Ceramic Resonator)

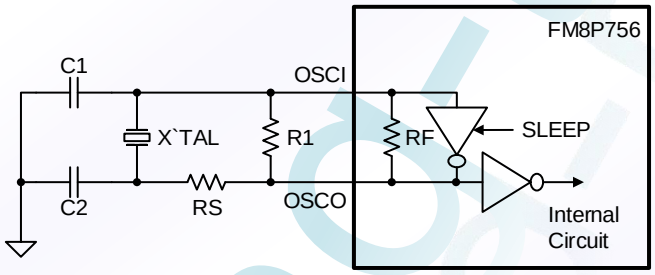


Figure 2.13: XT or LF Oscillator Modes (External Clock Input Operation)

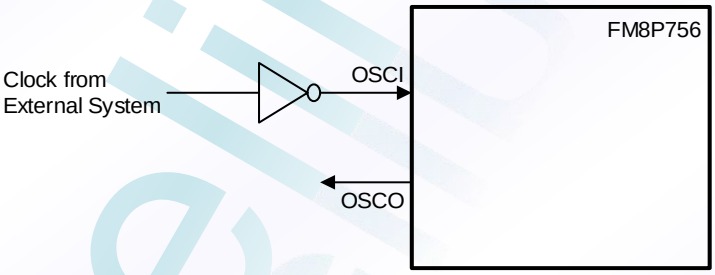
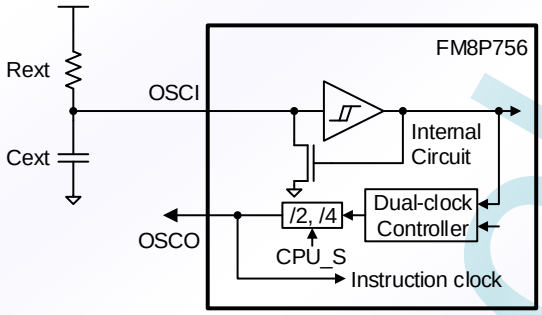


Figure 2.14: ERC Oscillator Mode (External RC Oscillator)

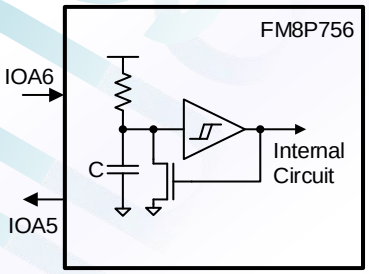


The typical oscillator frequency vs. external resistor is as following table
When Cext = 0.01uf (103)

5V		3V	
Rext	Frequency	Rext	Frequency
4.3M	32 KHz	3.6M	32 KHz
210K	500 KHz	238K	500 KHz
108K	1.0 MHz	116K	1.0 MHz
56K	2.0 MHz	59K	2.0 MHz
30K	4.0 MHz	30K	4.0 MHz
16K	8.0 MHz	16K	8.0 MHz
11K	12.0 MHz	11K	12.0 MHz

Note: Values are provided for design reference only.

Figure 2.15: HIRC/LIRC Oscillator Mode (Internal R, Internal C Oscillator)



2.14 Configuration Words

Table 2.8: Configuration Words

Name	Description
Fosc	Oscillator Selection Bit → HIRC (8 MHz or 4 MHz) mode (default) → HIRC (8 MHz or 4 MHz) & LIRC (12 KHz) mode → HIRC (8 MHz or 4 MHz) & XT crystal mode → HIRC (8 MHz or 4 MHz) & LF crystal mode → ERC mode → LIRC (12 KHz) mode → XT crystal mode → LF crystal mode Note: LIRC 12 KHz is an uncalibrated low frequency oscillator.
WDTEN	Watchdog Timer Enable Bit → WDT enabled (default) → WDT disabled
LVDT	Low Voltage Detector Selection Bit → LVDT = 2.2V → LVDT = 2.6V → LVDT = 3.7V (default)
RSTBIN	IOA7/RSTB Pin Selection Bit → RSTB pin is selected (default) → IOA7 pin is selected
OSCD	Instruction Period Selection Bit → four oscillator periods (4T) (default) → two oscillator periods (2T)
SYS_CK	System Clock Selection bit → 8 MHz → 4 MHz
OSCOUT	IOA5/OSCO Pin Selection Bit for ERC mode → OSCO pin is selected (default) → IOA5 pin is selected
PROTECT	Code Protection Bit → NO, OTP code protection off (default) → YES, OTP code protection on

Table 2.9: Selection of IOA5/OSCI and IOA6/OSCO Pin

Mode of oscillation	IOA6/OSCI	IOA5/OSCO
HIRC/LIRC	Force to IOA6	Force to IOA5
ERC	Force to OSCI	IOA5/OSCO selected by OSCOUT bit
XT, LF	Force to OSCI	Force to OSCO

3.0 INSTRUCTION SET

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	**R, bit**	Clear bit in R	0 → R<b>	1	-
BSR	**R, bit**	Set bit in R	1 → R<b>	1	-
BTRSC	**R, bit**	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2(1)	-
BTRSS	**R, bit**	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2(1)	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$,$\overline{PD}$
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$,$\overline{PD}$
TABL	**R**	Read low byte ROM table to (acc) ROM table address={TB_BNK,index of R}	ACC=ROM{BANK index: R}[7:0]	2	-
TABH	**R**	Read high byte ROM table to (acc) ROM table address={TB_BNK,index of R}	ACC=ROM{BANK index : R}[15:8]	2	-
DAA	**R, d**	Adjust data format of register from HEX to DEC after any addition operation	R(hex) → dest (dec)	1	C
DAS	**R, d**	Adjust data format of register from HEX to DEC after any subtraction operation	R(hex) → dest (dec)	1	C
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
RETF		Return from interrupt	Top of Stack → PC,	2	-
CLRA		Clear ACC	00h → ACC	1	Z
CLRR	**R**	Clear R	00h → R	1	Z
MOVAR	**R**	Move ACC to R	ACC → R	1	-
MOVR	**R, d**	Move R	R → dest	1	Z
MOV2	**R, d**	Move R	R → dest	1	-
DECR	**R, d**	Decrement R	R - 1 → dest	1	Z
DECRSZ	**R, d**	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2(1)	-
INCR	**R, d**	Increment R	R + 1 → dest	1	Z
INCRSZ	**R, d**	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2(1)	-
ADDAR	**R, d**	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	**R, d**	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ADCAR	**R, d**	Add ACC and R with Carry	R + ACC + C → dest	1	C, DC, Z
SBCAR	**R, d**	Subtract ACC from R with Carry	R + $\overline{ACC}$ + C → dest	1	C, DC, Z
ANDAR	**R, d**	AND ACC with R	ACC and R → dest	1	Z
IORAR	**R, d**	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	**R, d**	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	**R, d**	Complement R	$\overline{R}$→ dest	1	Z
RL	**R, d**	Rotate left R	R<6:0> → dest<7:1>, R<7>→ dest<0>	1	-
RLR	**R, d**	Rotate left R through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RL0	**R, d**	Rotate left R through 0	R<6:0> → dest<7:1>, 0 → dest<0>	1	-

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
RL1	**R, d**	Rotate left R through 1	R<6:0> → dest<7:1>, 1 → dest<0>	1	-
RR	**R, d**	Rotate right R	R<7:1> → dest<6:0>, R<0> → dest<7>	1	-
RRR	**R, d**	Rotate right R through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
RR0	**R, d**	Rotate right R with 0	0 → dest<7>, R<7:1> → dest<6:0>,	1	-
RR1	**R, d**	Rotate right R with 1	1 → dest<7>, R<7:1> → dest<6:0>,	1	-
SWAPR	**R, d**	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	**I**	Move Immediate to ACC	I → ACC	1	-
ADDIA	**I**	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	**I**	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA	**I**	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA	**I**	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA	**I**	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA	**I**	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL	**I**	Call subroutine	PC + 1 → Top of Stack, I → PC<10:0> I <10:8> → PCHBUF<2:0>	2	-
GOTO	**I**	Unconditional branch	I → PC<10:0> I <10:8> → PCHBUF<2:0>	2	-
TMSZA		If (ACC) =0, skip next instruction	Skip if ACC = 0	1/2(1)	-
TMSZR	**R**	If (R) =0, skip next instruction	Skip if R = 0	1/2(1)	-
TMSNZR	**R**	If (R) ≠ 0, skip next instruction	Skip if R ≠ 0	1/2(1)	-
TMCOMP	**R**	If (acc) =(R), skip next instruction	Skip if (acc) =(R)	1/2(1)	-
TMCOMPB	**R**	If (acc) ≠(R), skip next instruction	Skip if (acc) ≠ (R)	1/2(1)	-

Note: 1. 2 cycles for skip, else 1 cycle.
2. bit : Bit address within an 8-bit register R
R : Register address (00h to BFh)
I : Immediate data
ACC :Accumulator
d : Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
dest : Destination
PC : Program Counter
WDT :Watchdog Timer Counter
GIE : Global interrupt enable bit
$\overline{TO}$: Time-out bit
$\overline{PD}$: Power-down bit
C : Carry bit
DC : Digital carry bit
Z : Zero bit

ADCAR **Add ACC and R with Carry**

Syntax: ADCAR R, d
Operands: 0≤R≤0xBF
d∈ [0,1]
Operation: R + ACC + C → dest
Status Affected: C, DC, Z
Description: Add the contents of the ACC register and register 'R' with Carry. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles: 1

ADDAR **Add ACC and R**

Syntax: ADDAR R, d
Operands: 0≤R≤0xBF
d∈ [0,1]
Operation: ACC + R → dest
Status Affected: C, DC, Z
Description: Add the contents of the ACC register and register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles: 1

ADDIA **Add ACC and Immediate**

Syntax: ADDIA I
Operands: 0≤I≤0xFF
Operation: ACC + I → ACC
Status Affected: C, DC, Z
Description: Add the contents of the ACC register with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles: 1

ANDAR **AND ACC and R**

Syntax: ANDAR R, d
Operands: 0≤R≤0xBF
d∈ [0,1]
Operation: ACC and R → dest
Status Affected: Z
Description: The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles: 1

ANDIA **AND Immediate with ACC**

Syntax: ANDIA I
Operands: 0≤I≤0xFF
Operation: ACC AND I → ACC
Status Affected: Z
Description: The contents of the ACC register are AND'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles: 1

BCR	**Clear Bit in R**
Syntax:	BCR R, b
Operands:	0≤R≤0xBF 0≤b≤7
Operation:	0 → R<b>
Status Affected:	None
Description:	Clear bit 'b' in register 'R'.
Cycles:	1

BSR	**Set Bit in R**
Syntax:	BSR R, b
Operands:	0≤R≤0xBF 0≤b≤7
Operation:	1 → R<b>
Status Affected:	None
Description:	Set bit 'b' in register 'R'.
Cycles:	1

BTRSC	**Test Bit in R, Skip if Clear**
Syntax:	BTRSC R, b
Operands:	0≤R≤0xBF 0≤b≤7
Operation:	Skip if R<b> = 0
Status Affected:	None
Description:	If bit 'b' in register 'R' is 0 then the next instruction is skipped. If bit 'b' is 0 then next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead making this a 2-cycle instruction.
Cycles:	1/2

BTRSS	**Test Bit in R, Skip if Set**
Syntax:	BTRSS R, b
Operands:	0≤R≤0xBF 0≤b≤7
Operation:	Skip if R<b> = 1
Status Affected:	None
Description:	If bit 'b' in register 'R' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.
Cycles:	1/2

CALL	**Subroutine Call**
Syntax:	CALL I
Operands:	0≤I≤0x7FF
Operation:	PC + 1 → Top of Stack, I → PC<10:0> I <10:8> → PCHBUF<2:0>
Status Affected:	None
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>.
Cycles:	2

CLRA	Clear ACC
Syntax:	CLRA
Operands:	None
Operation:	00h → ACC; 1 → Z
Status Affected:	Z
Description:	The ACC register is cleared. Zero bit (Z) is set.
Cycles:	1

CLRR	Clear R
Syntax:	CLRR R
Operands:	$0 \leq R \leq 0xBF$
Operation:	00h → R; 1 → Z
Status Affected:	Z
Description:	The contents of register 'R' are cleared and the Z bit is set.
Cycles:	1

CLRWDT	Clear Watchdog Timer
Syntax:	CLRWDT
Operands:	None
Operation:	00h → WDT; 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. The status bits $\overline{TO}$ and $\overline{PD}$ will be set.
Cycles:	1

COMR	Complement R
Syntax:	COMR R, d
Operands:	$0 \leq R \leq 0xBF$ $d \in [0,1]$
Operation:	$\overline{R}$ → dest
Status Affected:	Z
Description:	The contents of register 'R' are complemented. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DAA	Adjust ACC's data format from HEX to DEC
Syntax:	DAA R, d
Operands:	$0 \leq R \leq 0xBF$ $d \in [0,1]$
Operation:	R(hex) → dest(dec)
Status Affected:	C
Description:	Convert the register data from hexadecimal to decimal format after any addition operation. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DAS	Adjust ACC's data format from HEX to DEC
Syntax:	DAS R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R(hex) → dest(dec)
Status Affected:	C
Description:	Convert the register data from hexadecimal to decimal format after any subtraction operation. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECR	Decrement R
Syntax:	DECR R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R - 1 → dest
Status Affected:	Z
Description:	Decrement of register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECRSZ	Decrement R, Skip if 0
Syntax:	DECRSZ R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R - 1 → dest; skip if result =0
Status Affected:	None
Description:	The contents of register 'R' are decrement. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'. If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a two-cycle instruction.
Cycles:	1/2

GOTO	Unconditional Branch
Syntax:	GOTO I
Operands:	0≤I≤0x7FF
Operation:	I → PC<10:0> I <10:8> → PCHBUF<2:0>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>.
Cycles:	2

INCR	Increment R
Syntax:	INCR R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R + 1 → dest
Status Affected:	Z
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

INCRSZ	Increment R, Skip if 0
Syntax:	INCRSZ R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R + 1 → dest, skip if result = 0
Status Affected:	None
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is the result is stored back in register 'R'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a two-cycle instruction.
Cycles:	1/2

IORAR	OR ACC with R
Syntax:	IORAR R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	ACC or R → dest
Status Affected:	Z
Description:	Inclusive OR the ACC register with register 'R'. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

IORIA	OR Immediate with ACC
Syntax:	IORIA I
Operands:	0≤I≤0xFF
Operation:	ACC or I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are OR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

MOVAR	Move ACC to R
Syntax:	MOVAR R
Operands:	0≤R≤0xBF
Operation:	ACC → R
Status Affected:	None
Description:	Move data from the ACC register to register 'R'.
Cycles:	1

MOVIA	Move Immediate to ACC
Syntax:	MOVIA I
Operands:	0≤I≤0xFF
Operation:	I → ACC
Status Affected:	None
Description:	The 8-bit immediate 'I' is loaded into the ACC register. The don't cares will assemble as 0s.
Cycles:	1

MOVR	**Move R**
Syntax:	MOVR R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R → dest
Status Affected:	Z
Description:	The contents of register 'R' is moved to destination 'd'. If 'd' is 0, destination is the ACC register. If 'd' is 1, the destination is file register 'R'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Cycles:	1

MOV2	**Move R**
Syntax:	MOV2 R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R → dest
Status Affected:	None
Description:	The contents of register 'R' is moved to destination 'd'. If 'd' is 0, destination is the ACC register. If 'd' is 1, the destination is file register 'R'. The zero status flag <Z> is not affected.
Cycles:	1

NOP	**No Operation**
Syntax:	NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Cycles:	1

RETF	**Return from Interrupt**
Syntax:	RETF
Operands:	None
Operation:	Top of Stack → PC
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). The 'GIE' bit would NOT be set to 1. This is a two-cycle instruction.
Cycles:	2

RETFIE	**Return from Interrupt, Set 'GIE' Bit**
Syntax:	RETFIE
Operands:	None
Operation:	Top of Stack → PC 1 → GIE
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). The 'GIE' bit is set to 1. This is a two-cycle instruction.
Cycles:	2

RETIA	**Return with Immediate in ACC**
Syntax:	RETIA I
Operands:	0≤I≤0xFF
Operation:	I → ACC; Top of Stack → PC
Status Affected:	None
Description:	The ACC register is loaded with the 8-bit immediate 'I'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RETURN	**Return from Subroutine**
Syntax:	RETURN
Operands:	None
Operation:	Top of Stack → PC
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RL	**Rotate Left R**
Syntax:	RL R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R<6:0> → dest<7:1>, R<7>→ dest<0>
Status Affected:	None
Description:	The contents of register 'R' are rotated left one bit. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RL0	**Rotate Left R with 0**
Syntax:	RL0 R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R<6:0> → dest<7:1>, 0 → dest<0>
Status Affected:	None
Description:	The contents of register 'R' are rotated left one bit to the left and bit0 fills with "0". If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RL1	**Rotate Left R with 1**
Syntax:	RL1 R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R<6:0> → dest<7:1>, 1 → dest<0>
Status Affected:	None
Description:	The contents of register 'R' are rotated left one bit to the left and bit0 fills with "1". If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RLR	**Rotate Left R through Carry**
Syntax:	RLR R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R<7> → C; R<6:0> → dest<7:1>; C → dest<0>
Status Affected:	C
Description:	The contents of register 'R' are rotated left one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RR	**Rotate Right R**
Syntax:	RR R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	R<7:1> → dest<6:0>, R<0> → dest<7>
Status Affected:	None
Description:	The contents of register 'R' are rotated right one bit. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

RR0	**Rotate Right R with 0**
Syntax:	RR0 R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	0 → dest<7>, R<7:1> → dest<6:0>
Status Affected:	None
Description:	The contents of register 'R' are rotated right one bit and bit7 fills with "0". If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

RR1	**Rotate Right R with 1**
Syntax:	RR1 R, d
Operands:	0≤R≤0xBF d∈ [0,1]
Operation:	1 → dest<7>, R<7:1> → dest<6:0>
Status Affected:	None
Description:	The contents of register 'R' are rotated right one bit and bit7 fills with "1". If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

RRR	Rotate Right R through Carry
Syntax:	RRR R, d
Operands:	0≤R≤0xBF d∈[0,1]
Operation:	C → dest<7>; R<7:1> → dest<6:0>; R<0> → C
Status Affected:	C
Description:	The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

SLEEP	Enter SLEEP Mode
Syntax:	SLEEP
Operands:	None
Operation:	00h → WDT; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT is cleared. The processor is put into SLEEP mode.
Cycles:	1

SBCAR	Subtract ACC from R with Carry
Syntax:	SBCAR R, d
Operands:	0≤R≤0xBF d∈[0,1]
Operation:	R + $\overline{ACC}$ + C → dest
Status Affected:	C, DC, Z
Description:	Add the 2's complement data of the ACC register from register 'R' with Carry. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBAR	Subtract ACC from R
Syntax:	SUBAR R, d
Operands:	0≤R≤0xBF d∈[0,1]
Operation:	R - ACC → dest
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBIA	Subtract ACC from Immediate
Syntax:	SUBIA I
Operands:	0≤I≤0xFF
Operation:	I - ACC → ACC
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

SWAPR	**Swap nibbles in R**
Syntax:	SWAPR R, d
Operands:	0≤R≤0xBF
	d∈[0,1]
Operation:	R<3:0> → dest<7:4>;
	R<7:4> → dest<3:0>
Status Affected:	None
Description:	The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0 the result is placed in ACC register. If 'd' is 1 the result in placed in register 'R'.
Cycles:	1

TABL	**Table Look-up Low Byte**
Syntax:	TABL R
Operands:	0≤R≤0xBF
Operation:	ACC=ROM{TB_BNK index : R}[7:0]
Status Affected:	None
Description:	Read low byte ROM table to (ACC)
	ROM table address={TB_BNK index : R}
Cycles:	2

TABH	**Table Look-up High Byte**
Syntax:	TABH R
Operands:	0≤R≤0xBF
Operation:	ACC=ROM{TB_BNK index : R}[15:8]
Status Affected:	None
Description:	Read High byte ROM table to (ACC)
	ROM table address={TB_BNK index : R}
Cycles:	2

TMCOMP	**Test ACC and R, Skip if equal**
Syntax:	TMCOMP R
Operands:	0≤R≤0xBF
Operation:	Skip if ACC = R
Status Affected:	None
Description:	If ACC is equal to R then the next instruction is skipped.
	If ACC is equal to R then next instruction fetched during the current instruction execution is discarded, a NOP is executed instead and making this a 2-cycle instruction.
Cycles:	1/2

TMCOMPB	**Test ACC and R, Skip if not equal**
Syntax:	TMCOMPB R
Operands:	0≤R≤0xBF
Operation:	Skip if ACC ≠ R
Status Affected:	None
Description:	If ACC is not equal to R then the next instruction is skipped.
	If ACC is not equal to R then next instruction fetched during the current instruction execution is discarded, a NOP is executed instead and making this a 2-cycle instruction.
Cycles:	1/2

TMSZA	**Test ACC, Skip if equal to 0**
Syntax:	TMSZA
Operands:	
Operation:	Skip if ACC = 0
Status Affected:	None
Description:	If ACC is equal to 0 then the next instruction is skipped. If ACC is equal to 0 then next instruction fetched during the current instruction execution is discarded, a NOP is executed instead and making this a 2-cycle instruction.
Cycles:	1/2

TMSNZR	**Test R, Skip if not equal to 0**
Syntax:	TMSNZR R
Operands:	$0 \leq R \leq 0xBF$
Operation:	Skip if R ≠ 0
Status Affected:	None
Description:	If R is not equal to 0 then the next instruction is skipped. If R is not equal to 0 then next instruction fetched during the current instruction execution is discarded, a NOP is executed instead and making this a 2-cycle instruction.
Cycles:	1/2

TMSZR	Test R, Skip if equal to 0
Syntax:	TMSZR R
Operands:	$0 \leq R \leq 0xBF$
Operation:	Skip if R = 0
Status Affected:	None
Description:	If R is equal to 0 then the next instruction is skipped. If R is equal to 0 then next instruction fetched during the current instruction execution is discarded, a NOP is executed instead and making this a 2-cycle instruction.
Cycles:	1/2

XORAR	Exclusive OR ACC with R
Syntax:	XORAR R, d
Operands:	$0 \leq R \leq 0xBF$ $d \in [0,1]$
Operation:	ACC xor R → dest
Status Affected:	Z
Description:	Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

XORIA	**Exclusive OR Immediate with ACC**
Syntax:	XORIA I
Operands:	$0 \leq I \leq 0xFF$
Operation:	ACC xor I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-40℃ to +85℃
Store Temperature	-65℃ to +150℃
DC Supply Voltage (Vdd)	0V to +6.0V
Input Voltage with respect to Ground (Vss)	-0.3V to (Vdd + 0.3)V

5.0 OPERATING CONDITIONS

DC Supply Voltage	+2.2V to +5.5V
Operating Temperature	-40℃ to +85℃

6.0 ELECTRICAL CHARACTERISTICS

6.1 ELECTRICAL CHARACTERISTICS of FM8P756A/B/C/D/E/F/G

Ta=25℃

Under Operating Conditions, at four clock instruction cycles and WDT & LVDT are disabled

Sym	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	0Hz ~ 4MHz		2.2	5.5	V
		4MHz ~ 8MHz		2.4	5.5	
		8MHz ~ 10MHz		2.6	5.5	
		10MHz ~ 12MHz		2.8	5.5	
		12MHz ~ 16MHz		3.4	5.5	
		16MHz ~ 20MHz		4.0	5.5	
T_{PWR}	Power rising time	Vdd=0V to Vdd	0.8		2.6	ms/V
F_{XT}	X'tal oscillation range	XT mode, Vdd=5V, Fcpu=Fosc/2			20	MHz
		XT mode, Vdd=3V, Fcpu=Fosc/2			15	
F_{LF}	X'tal oscillation range	LF mode, Vdd=5V, Fcpu=Fosc/2			4000	KHZ
		LF mode, Vdd=3V, Fcpu=Fosc/2			1000	
F_{ERC}	RC oscillation range	ERC mode, Vdd=5V, Fcpu=Fosc/2			15	MHz
		ERC mode, Vdd=3V, Fcpu=Fosc/2			7	
V_{IH}	Input high voltage	With schmitter				V
		I/O ports	0.7Vdd		Vdd	
		RSTB pin	0.8Vdd		Vdd	
V_{IL}	Input low voltage	With schmitter				V
		I/O ports	Vss		0.2Vdd	
		RSTB pin	Vss		0.2Vdd	
I_{IL}	Input Leakage Current	Vin=5V, Vdd=5V			1	uA
		Vin=0V, Vdd=5V			1	
I_{OH}	IO Drive Current	VOH=4.5V, Vdd=5V		8		mA
		VOH=4V, Vdd=5V		15		
I_{OL}	IO Sink Current	VOL=0.5V, Vdd=5V		14		mA
		VOL=0.75V, Vdd=5V		21		
R_{PH}	Pull-high resister	Input pin at Vss, vdd=5V	65	145	195	KΩ
		Input pin at Vss, vdd=3V	125	290	375	
I_{WDT}	WDT current	Vdd=5V		8		uA
		Vdd=3V		2		
T_{WDT}	WDT period	Vdd=3V		24		mS
		Vdd=5V		20		
I_{LVDT}	LVDT current	LVDT=3.7V, vdd=5V		2		uA
		LVDT=2.6V, vdd=5V		3		
		LVDT=2.6V, vdd=3V		0.5		
		LVDT=2.2V, vdd=5V		3		
		LVDT=2.2V, vdd=3V		0.5		
V_{LVDT}	LVDT voltage	LVDT=3.7V	3.5	3.7	3.9	V
		LVDT=2.6V	2.4	2.6	2.8	
		LVDT=2.2V	2.0	2.2	2.4	
V_{AD}	A/D input Voltage		0		Vdd	V
R_{AD}	Resolution				10	Bits

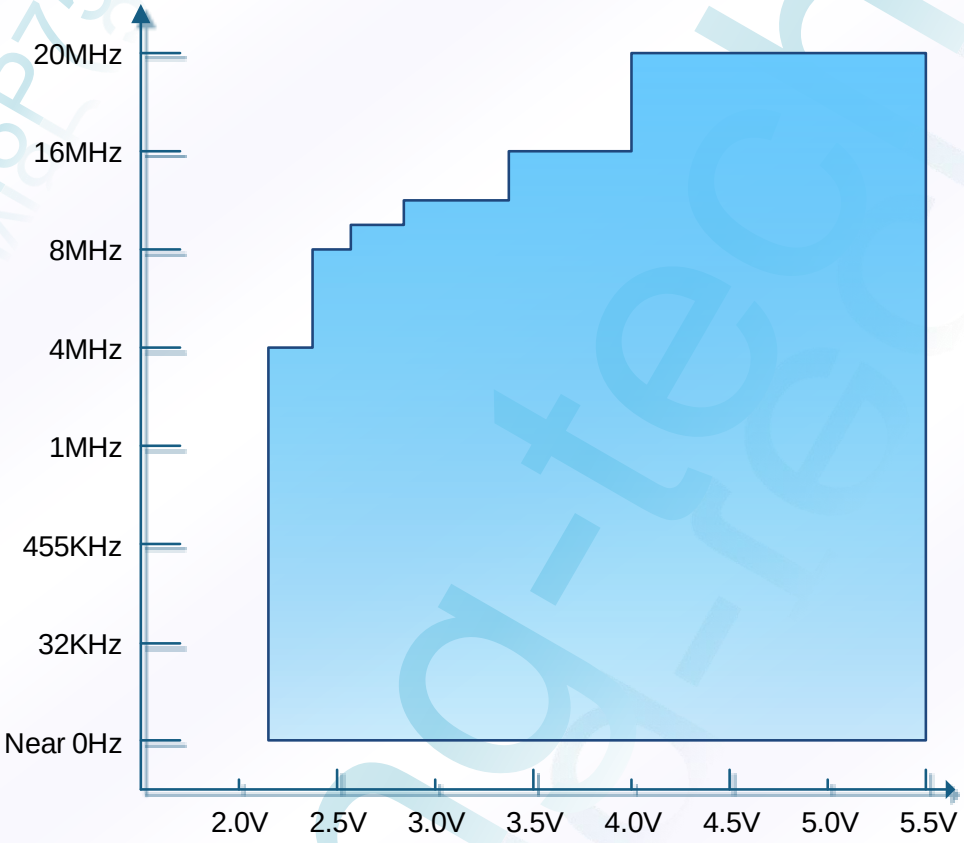
Sym	Description	Conditions	Min.	Typ.	Max.	Unit
DNL	A/D Differential Non-Linear			1		LSB
INL	A/D Integral Non-Linear			2		LSB
I_{ADC}	A/D Operation Current	Vdd=5V, 4 clock instruction		470		uA
		Vdd=5V, 2 clock instruction		440		
		Vdd=3V, 4 clock instruction		80		
		Vdd=3V, 2 clock instruction		40		
T_{AD}	A/D clock period		8			us
T_{ADC}	A/D Conversion Time			25		T_{AD}
T_{ADCS}	A/D Sampling Time			8		T_{AD}
I_{SB}	Power down current	Sleep mode, Vdd=5V, WDT disable, LVDT off			1	uA
		Sleep mode, Vdd=3V, WDT disable, LVDT off			1	
I_{COM}	COM Operating current	Vdd=5V, COMIS[1:0] = 0 0	17.5	25	32.5	uA
		Vdd=5V, COMIS[1:0] = 0 1	35	50	65	
		Vdd=5V, COMIS[1:0] = 1 0	70	100	130	
		Vdd=5V, COMIS[1:0] = 1 1	140	200	260	
V_{COM}	1/2 bias voltage range	Vdd=5V, No load	0.475	0.5	0.525	VDD
I_{DD}	Operating current	IRC mode, vdd=5V, 4 clock instruction				mA
		SYS_CK=8 MHz		2.27		
		SYS_CK=4 MHz		1.63		
		IRC mode, vdd=5V, 2 clock instruction				
		SYS_CK=8 MHz		3.64		
		SYS_CK=4 MHz		2.28		
		IRC mode, vdd=3V, 4 clock instruction				
		SYS_CK=8 MHz		1.15		
		SYS_CK=4 MHz		0.80		
		IRC mode, vdd=3V, 2 clock instruction				
		SYS_CK=8 MHz		1.62		
		SYS_CK=4 MHz		1.13		
I_{DD}	Operating current	XT mode, vdd=5V, 4 clock instruction				mA
		20 MHz		4.92		
		16 MHz		3.99		
		12 MHz		3.18		
		4 MHz		1.40		
		XT mode, vdd=5V, 2 clock instruction				
		20 MHz		6.88		
		16 MHz		5.95		
		12 MHz		5.03		
		4 MHz		2.08		

Sym	Description	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	XT mode, vdd=3V, 4 clock instruction				mA
		20 MHZ		1.9		
		16 MHz		1.64		
		12 MHz		1.40		
		4 MHz		0.56		
		XT mode, vdd=3V, 2 clock instruction				
		20 MHZ		-		
		16 MHz		-		
		12 MHz		1.96		
		4 MHz		0.88		
I_{DD}	Operating current	LF mode, Vdd=5V, 4 clock instruction				uA
		32 KHz		35		
		LF mode, Vdd=5V, 2 clock instruction				
		32 KHz		40.8		
I_{DD}	Operating current	LF mode, Vdd=3V, 4 clock instruction				uA
		32 KHz		8.8		
		LF mode, Vdd=3V, 2 clock instruction				
		32 KHz		11.4		
I_{DD}	Operating current	LIRC mode, Vdd=5V, 4 clock instruction				uA
		Near 12 KHz		13		
		LIRC mode, Vdd=5V, 2 clock instruction				
		Near 12 KHz		15		
I_{DD}	Operating current	LIRC mode, Vdd=3V, 4 clock instruction				uA
		Near 12 KHz		3		
		LIRC mode, Vdd=3V, 2 clock instruction				
		Near 12 KHz		4		

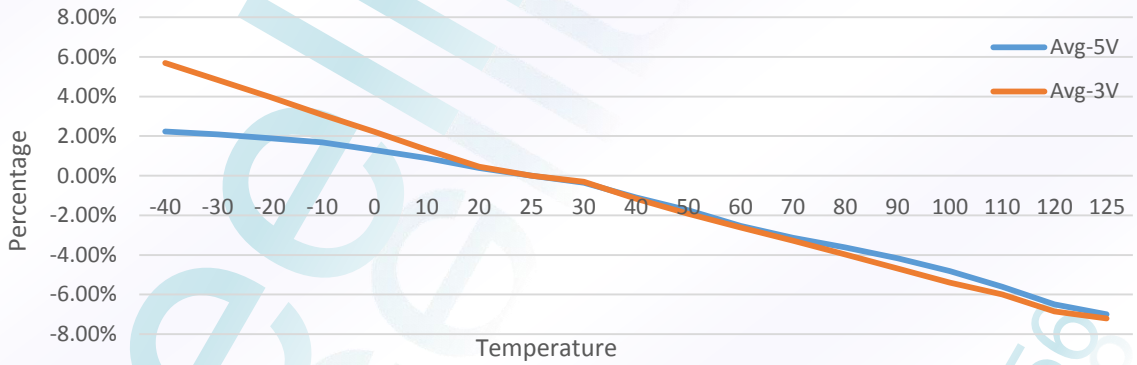
Note: LIRC 12 KHz is an uncalibrated low-frequency oscillator, current is for reference only.

6.2 ELECTRICAL CHARACTERISTICS Charts of FM8P756A/B/C/D/E/F/G

6.2.1 Operator Frequency vs. Operator voltage (Ta=25℃, 2 clock instruction)

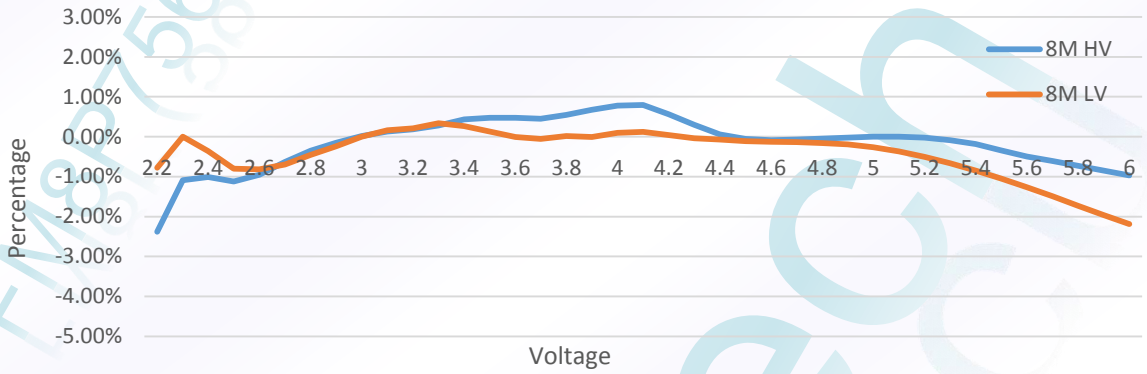


6.2.2 Internal 8MHz RC vs. Temperature



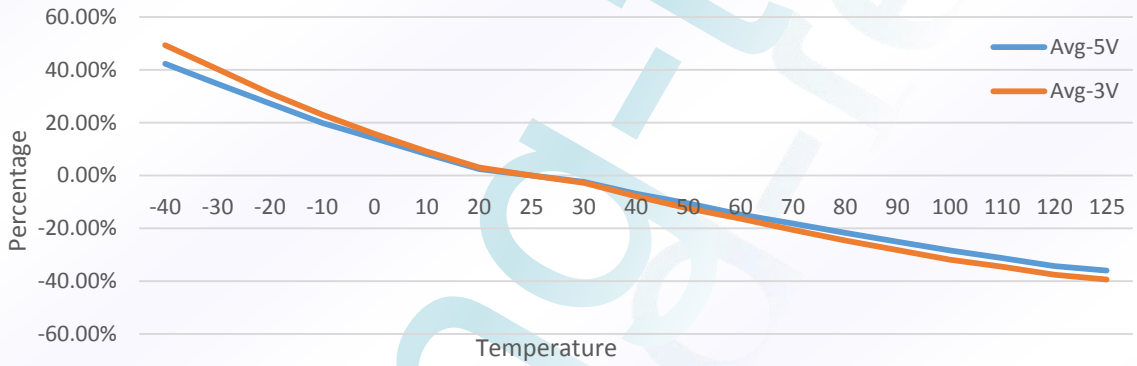
Note: Curves are for design reference only.

6.2.3 Internal 8MHz RC vs. Supply Voltage (Ta=25℃)



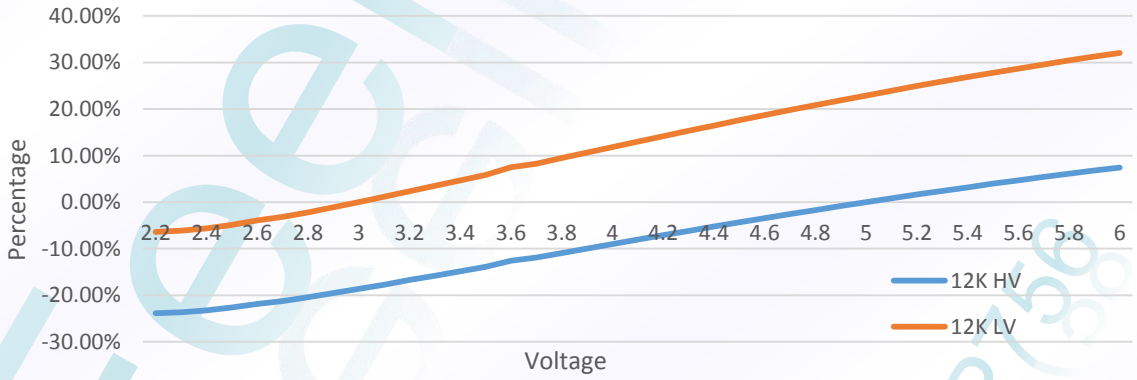
Note: Curves are for design reference only.

6.2.4 Internal 12KHz RC vs. Temperature



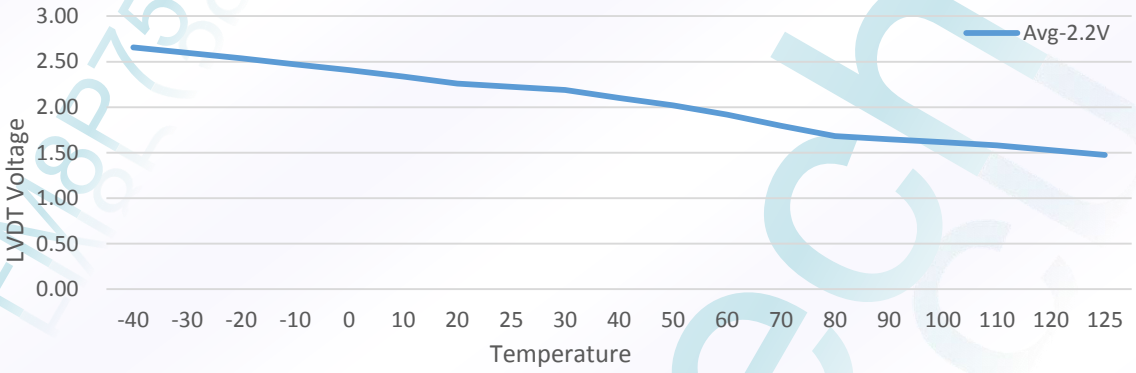
Note: 1. Curves are for design reference only.
2. 12 KHz is an uncalibrated low-frequency oscillator

6.2.5 Internal 12KHz RC vs. Supply Voltage (Ta=25℃)



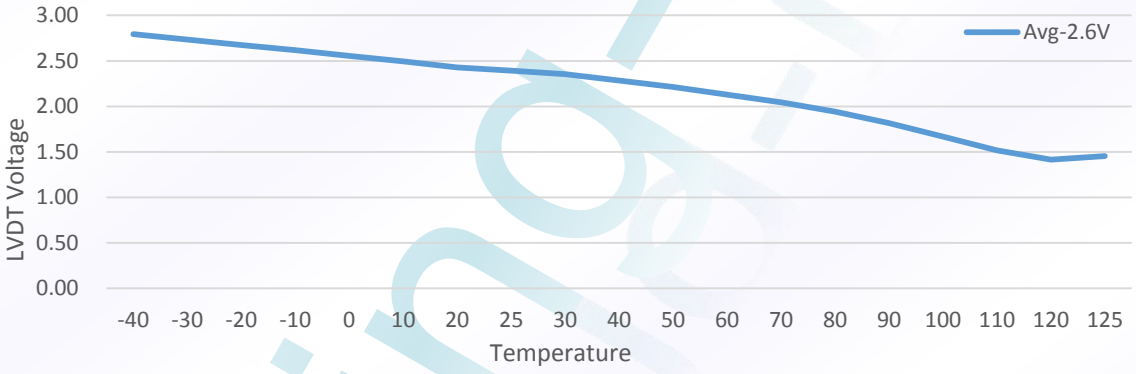
Note: 1. Curves are for design reference only.
2. 12 KHz is an uncalibrated low-frequency oscillator

6.2.6 Low Voltage Detect (LVDT=2.2V) vs. Temperature



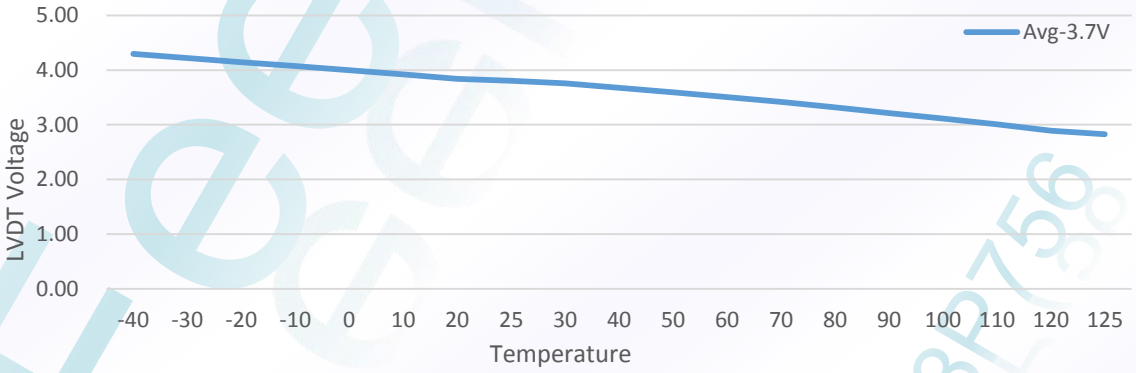
Note: Curves are for design reference only.

6.2.7 Low Voltage Detect (LVDT=2.6V) vs. Temperature



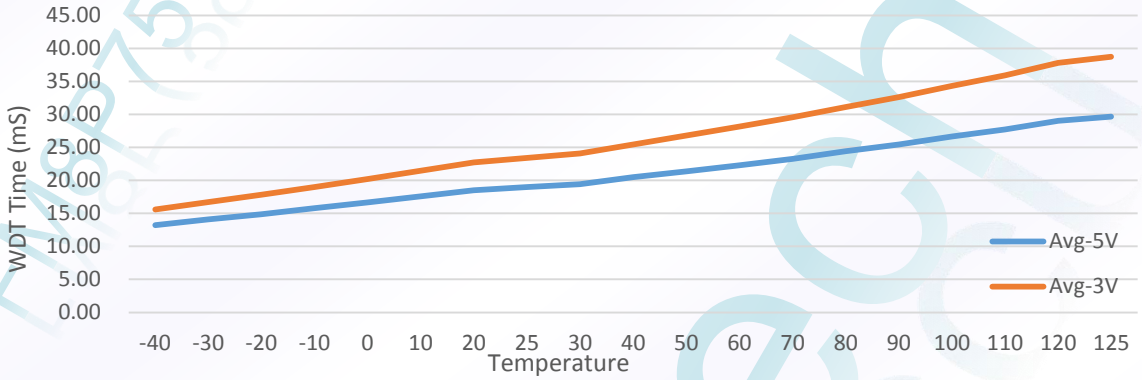
Note: Curves are for design reference only.

6.2.8 Low Voltage Detect (LVDT=3.7V) vs. Temperature



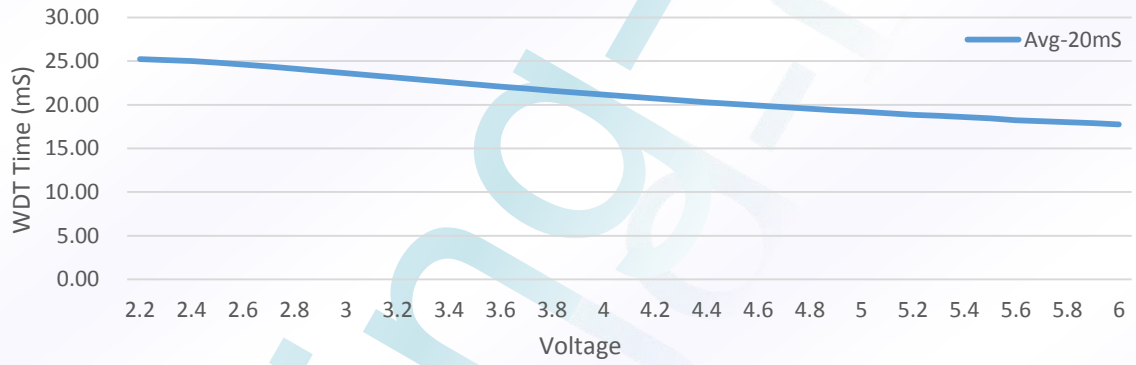
Note: Curves are for design reference only.

6.2.9 WDT 20mS Reset time vs. Temperature



Note: Curves are for design reference only.

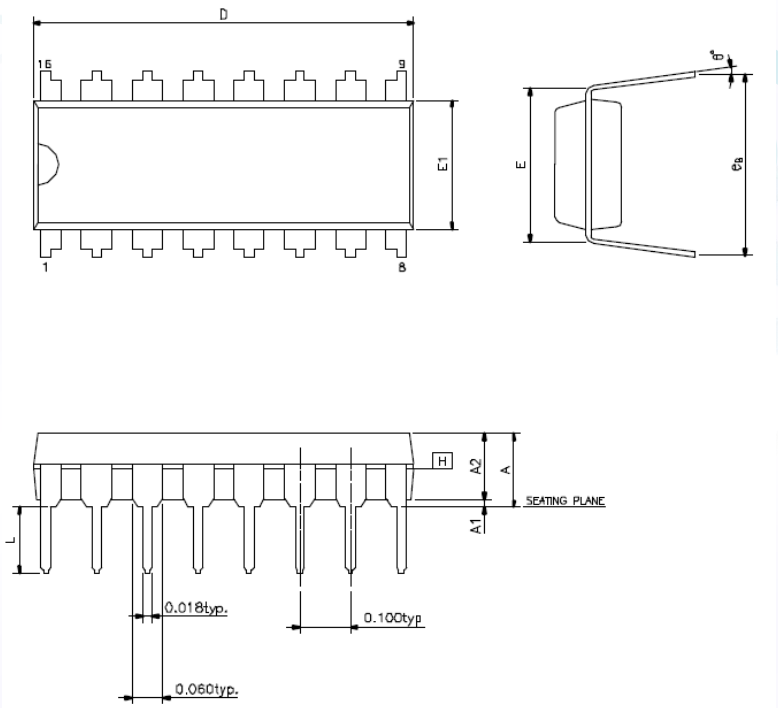
6.2.10 WDT 20mS Reset time vs. Supply Voltage (Ta=25℃)



Note: Curves are for design reference only.

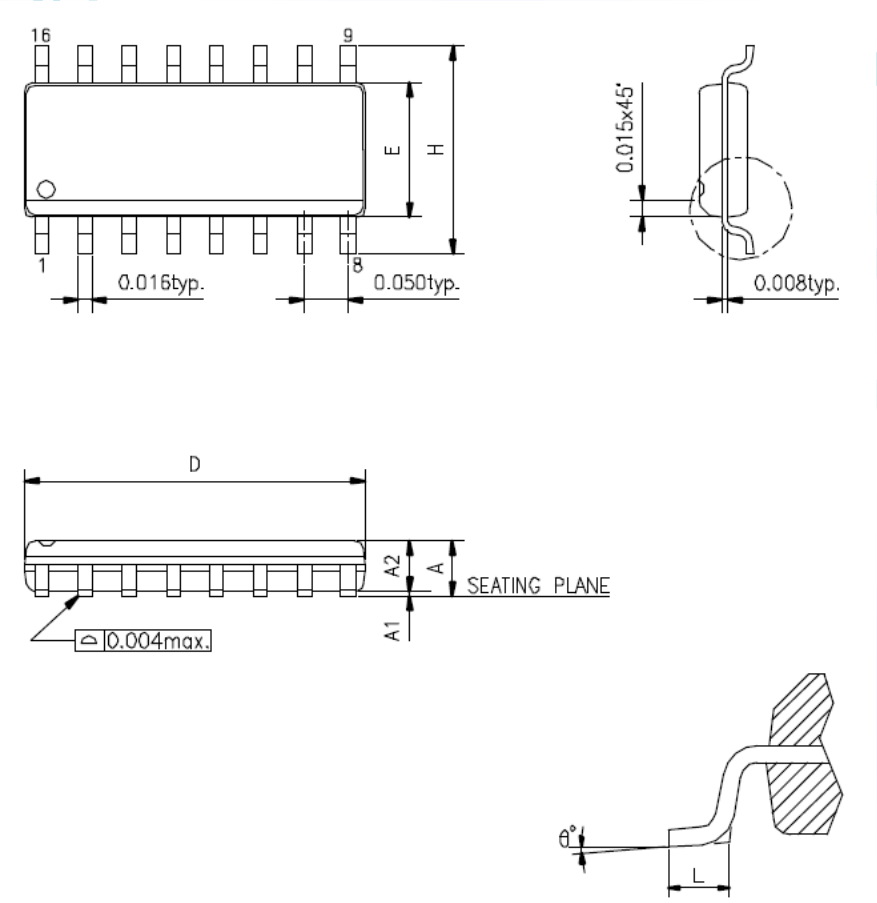
7.0 PACKAGE DIMENSION

7.1 16-PIN PDIP 300mil



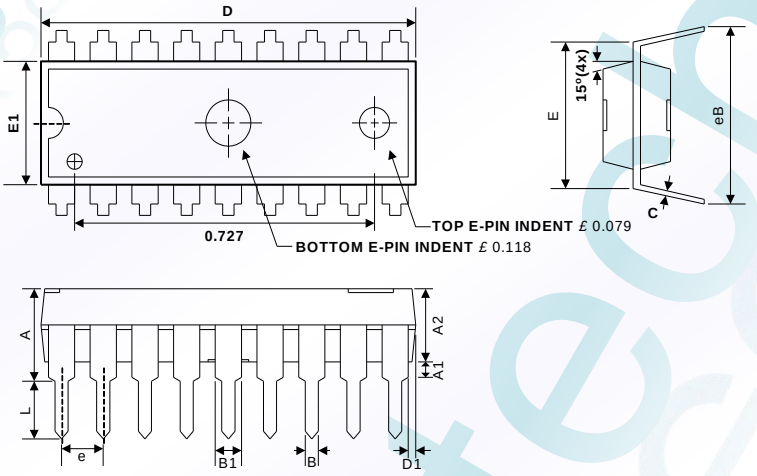
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E		0.300 BSC	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

7.2 16-PIN SOP 150mil



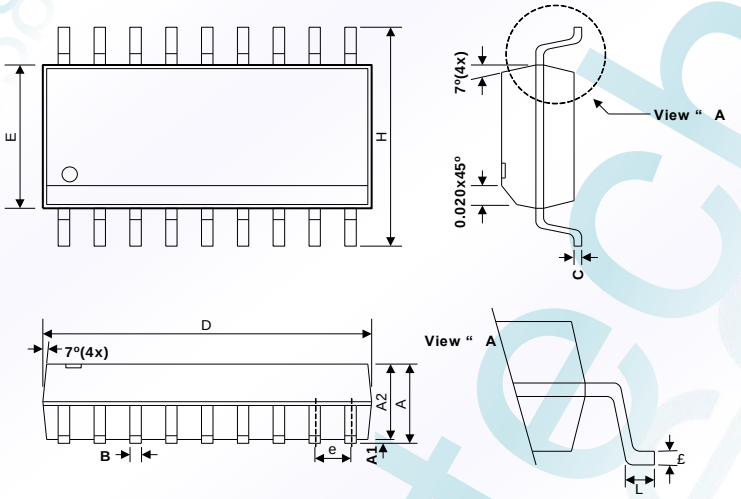
Symbols	Dimension In Inches	
	Min	Max
A	0.053	0.069
A1	0.004	0.010
A2	0.049	0.065
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0°	8°

7.3 18-PIN PDIP 300mil



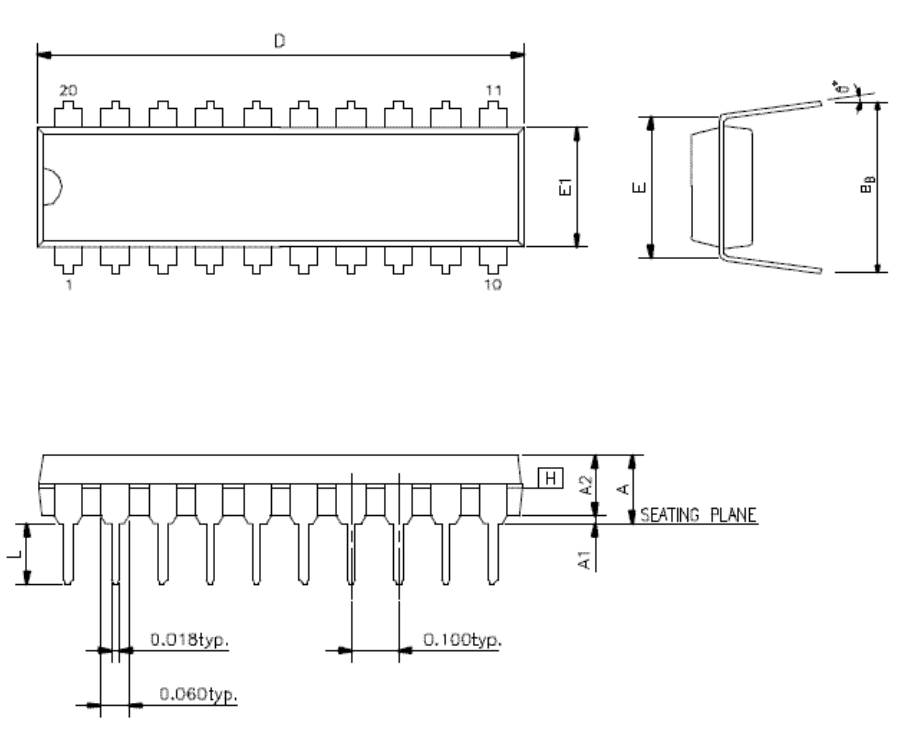
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.180
A1	0.05	-	-
A2	-	0.130	0.140
B	0.014	0.018	0.022
B1	0.050	0.060	0.070
C	0.008	0.010	0.013
D	0.894	0.904	0.910
D1	0.017	0.022	0.027
E	0.300	-	0.325
E1	0.252	0.256	0.262
e	-	0.100	-
L	0.125	-	-

7.4 18-PIN SOP 300mil



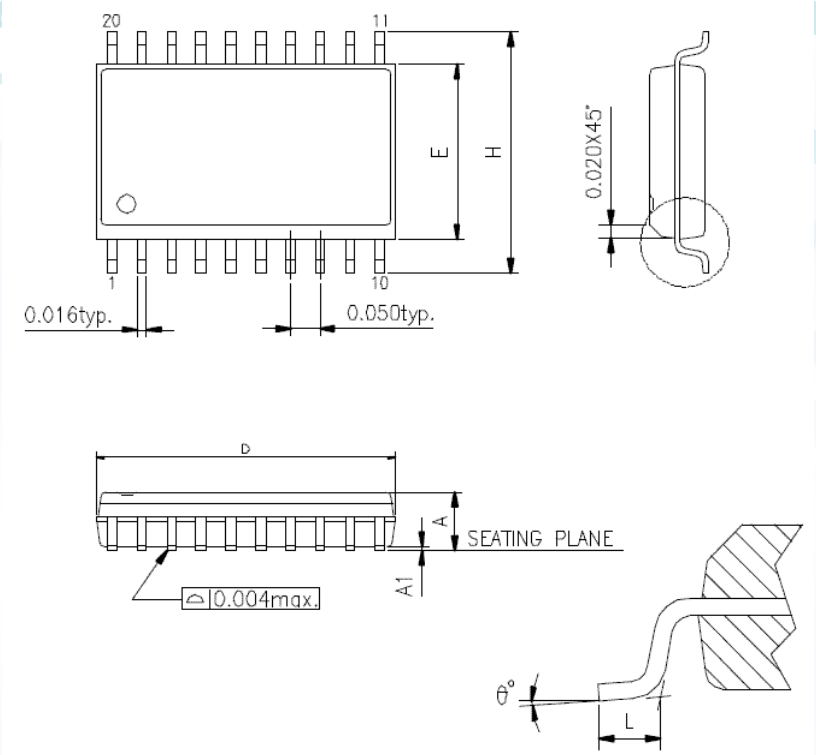
Symbols	Dimension In Inches		
	Min	Nom	Max
A	0.093	0.098	0.104
A1	0.04	-	0.012
A2	-	0.091	-
B	0.013	0.016	0.020
C	0.007	0.009	0.011
D	0.447	-	0.463
E	0.291	0.295	0.299
e	-	0.050	-
H	0.394	0.406	0.419
L	0.015	0.032	0.050
θº	0º	-	8º

7.5 20-PIN PDIP 300mil



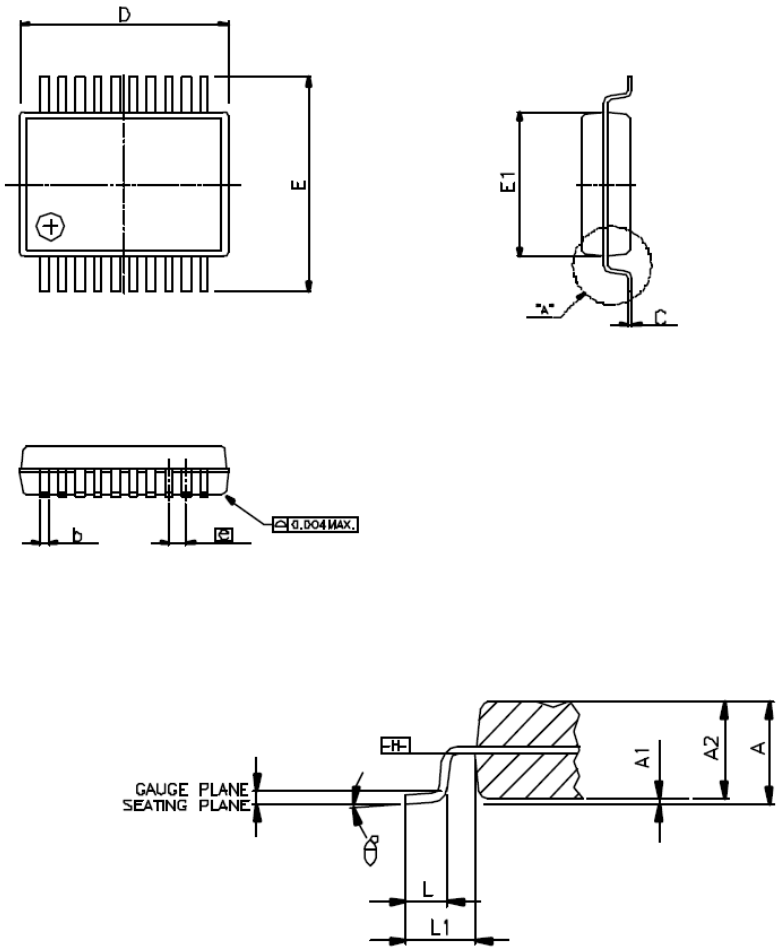
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.98	1.030	1.060
E		0.300 BSC	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

7.6 20-PIN SOP 300mil



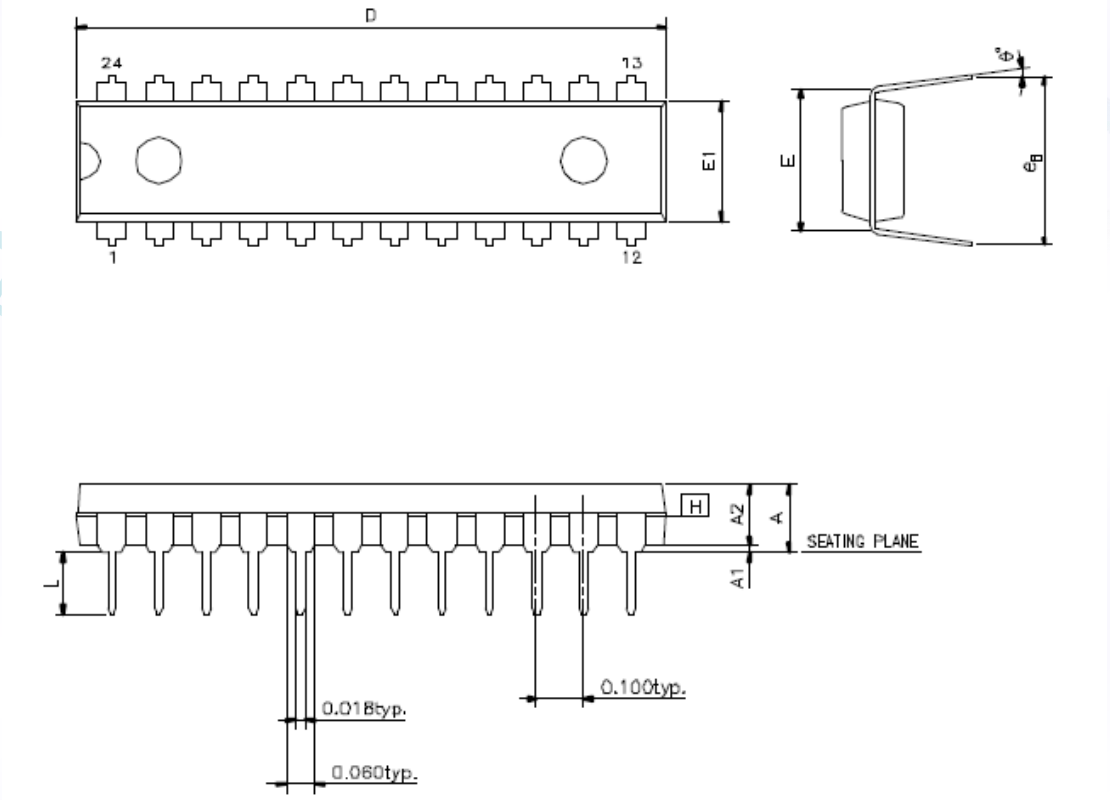
Symbols	Dimension In Inches		
	Min	Nom	Max
A	0.093	-	0.104
A1	0.004	-	0.012
D	0.496	-	0.508
E	0.291	-	0.299
H	0.394	-	0.419
L	0.016	-	0.050
θ°	0°	-	8°

7.7 20-PIN SSOP 209 mil



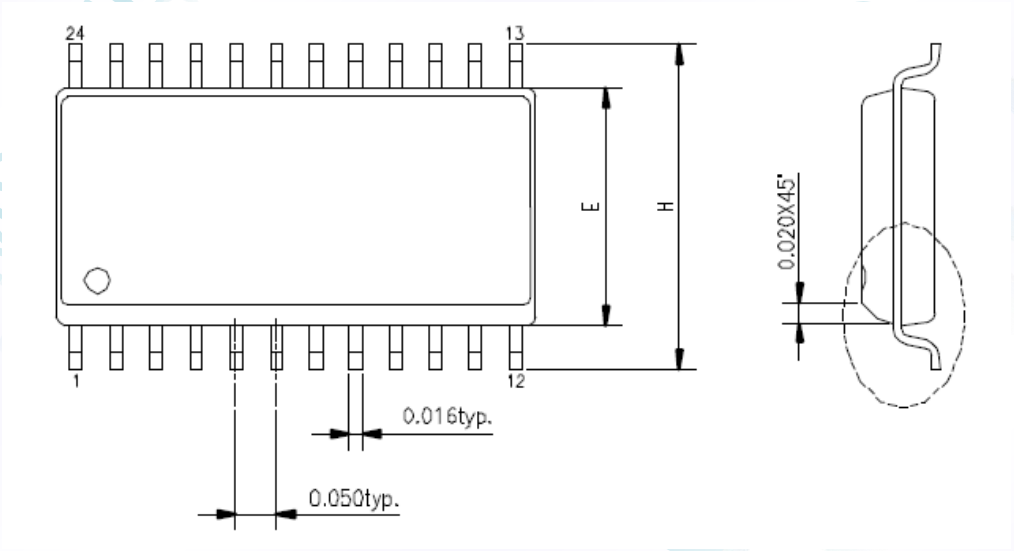
Symbols	Dimension In Millimeters		
	Min	Nom	Max
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.21
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65	-
L	0.55	0.75	0.95
L1	-	1.25	-
θ°	0°	4°	8°

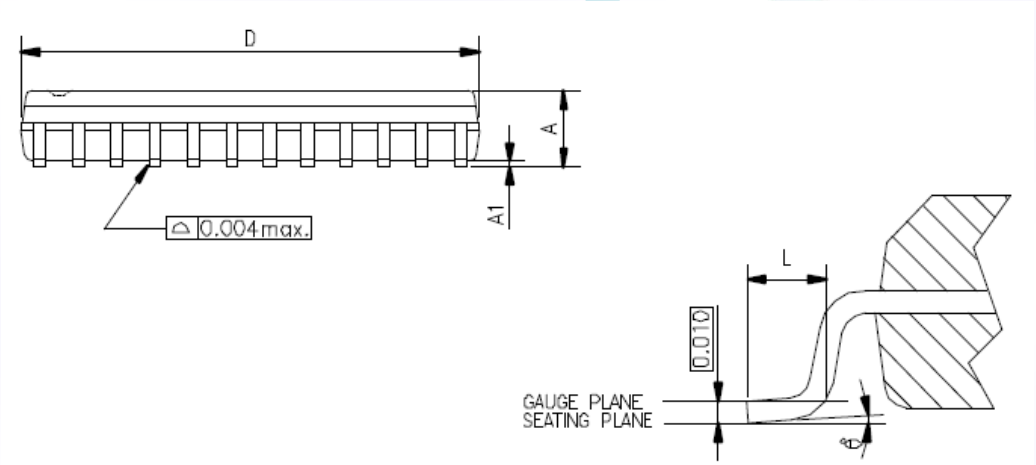
7.8 24-PIN Skinny PDIP 300mil



Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E	0.300 BSC.		
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

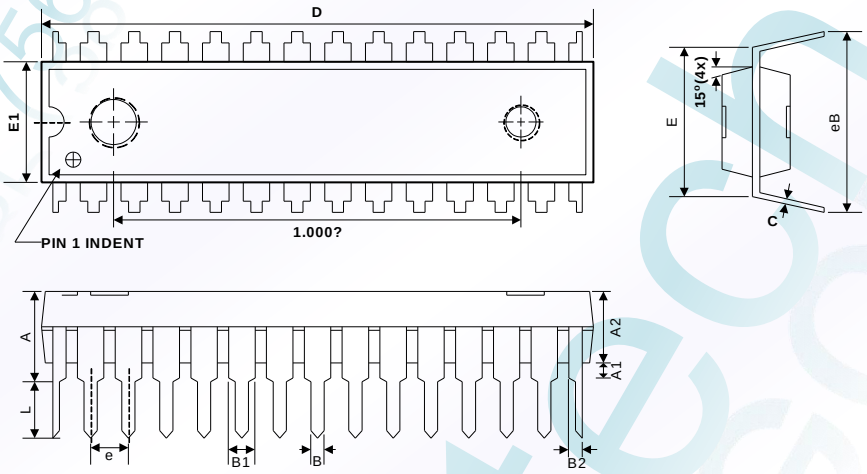
7.9 24-PIN SOP 300mil





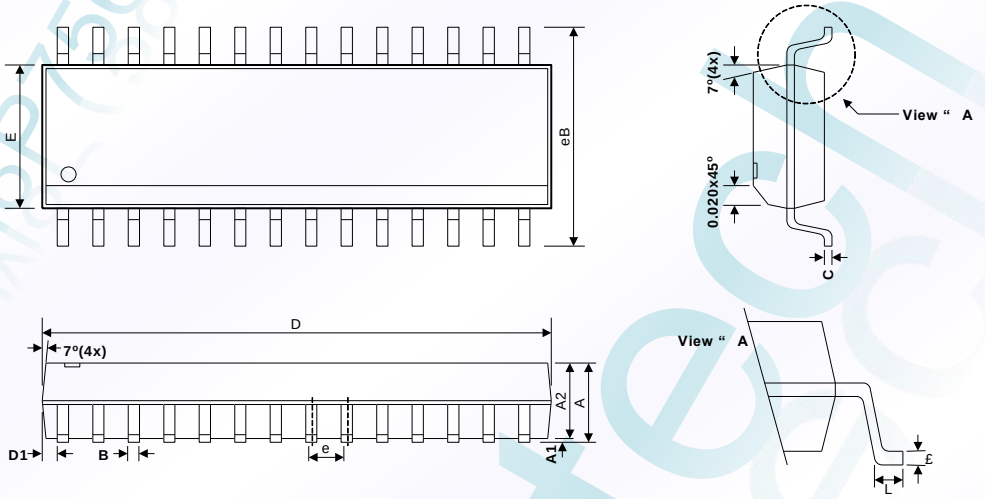
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.104
A1	0.004	-	-
D	0.599	0.600	0.624
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0°	4°	8°

7.10 28-PIN Skinny PDIP 300mil



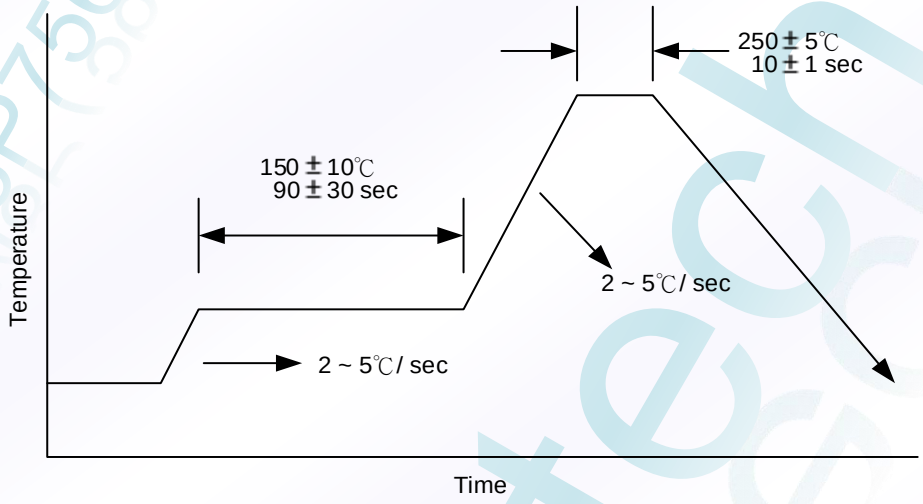
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.180
A1	0.015	-	-
A2	-	0.130	0.140
B	0.0040	-	0.065
B1	0.016	-	0.023
B2	0.028	-	0.044
C	0.008	0.010	0.013
D	1.383	1.385	1.395
E	0.310	0.327	0.330
E1	0.284	0.288	0.296
e	-	0.100	-
L	0.125	-	-
eB	0.340	-	0.380

7.11 28-PIN SOP 300mil



Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	0.098	0.108
A1	0.006	-	-
A2	0.087	0.091	0.097
B	0.012	0.016	0.020
C	0.008	0.010	0.012
D	0.700	0.705	0.725
E	0.290	0.295	0.300
e	0.048	0.050	0.052
eB	0.404	0.410	0.416
L	0.025	-	-
θ	0°	4°	8°
D1	0.014	0.020	-

8.0 PACKAGE IR Re-flow Soldering Curve



9.0 ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size	SAMPLE Stock
FM8P756AM	SKINNY-DIP	24	300 mil	No stock
FM8P756AD	SOP	24	300 mil	Available
FM8P756BP	DIP	20	300 mil	No stock
FM8P756BD	SOP	20	300 mil	Available
FM8P756BR	SSOP	20	209 mil	Available
FM8P756CP	DIP	16	300 mil	No stock
FM8P756CD	SOP	16	150 mil	Available
FM8P756DM	SKINNY-DIP	28	300 mil	Available
FM8P756DD	SOP	28	300 mil	Available
FM8P756EM	SKINNY-DIP	24	300 mil	No stock
FM8P756ED	SOP	24	300 mil	Available
FM8P756FP	DIP	18	300 mil	No stock
FM8P756FD	SOP	18	300 mil	Available
FM8P756GP	DIP	20	300 mil	No stock
FM8P756GD	SOP	20	300 mil	Available