Filtronic

FMA246

Preliminary Datasheet v3.0

HIGH GAIN X-BAND MMIC AMPLIFIER

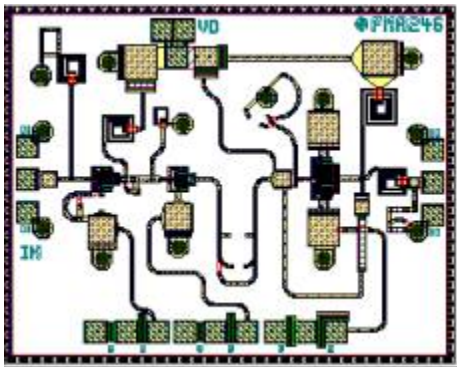
FEATURES:

- 8.0 – 14.0 GHz Operating Bandwidth
- 2.5 dB Noise Figure
- 30 dB Small-Signal Gain
- 19 dm Output Power
- +6V Single Bias Supply
- Adjustable Operating Current
- DC De-coupled Input and Output Ports

GENERAL DESCRIPTION:

The FMA246 is a 3-stage, reactively matched pHEMT high-gain MMIC amplifier designed for use over the 8 to 14 GHz bandwidth. The supply voltage can be varied from +3V to +6V if needed. Operating current can be adjusted using the source resistor ladders located along the bottom edge, by bonding a particular pad to ground. The amplifier is unconditionally stable over all load states (-45 to +85°C), and conditionally stable if the input port is open-circuited.

LAYOUT:



TYPICAL APPLICATIONS:

- Low noise front end amplifiers
- General X-Band gain block

ELECTRICAL SPECIFICATIONS[1]:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency Bandwidth	BW		8	N/A	14	GHz
Small Signal Gain	S21	VDD = +6 V IDD ≈ 60% IDSS	27	29	31	dB
Operating Current	IOP	VDD = +6V	105	150	195	mA
Small Signal Gain Flatness	ΔS21	VDD = +6 V IDD ≈ 60% IDSS[2]		± 0.6	± 1.0	dB
Noise Figure	NF	VDD = +6 V IDD ≈ 60% IDSS[2]	-	2.5	2.8	dB
3rd Order Intermodulation Distortion	IMD	VDD = +6 V IDD ≈ 60% IDSS[2] POUT = +9 dBm SCL	-	-44	-	dBc
Power at 1dB Compression	P1dB	VDD = +6 V IDD ≈ 60% IDSS[2]	18	20	-	dBm
Input Return Loss	S11	VDD = +6 V IDD ≈ 60% IDSS[2]	-	-10	-8	dB
Output Return Loss	S22	VDD = +6 V IDD ≈ 60% IDSS[2]	-	-16	-9	dB
Reverse Isolation	S12	VDD = +6 V IDD ≈ 60% IDSS[2]	-	-60	-50	dB

Note: 1. $T_{Ambient}$ = 22°C; Continuous operation at IDSS is not recommended

2. 60%IDSS is achieved by bonding pads "D", "G", and "K" (shown on page 2) to ground to drive the 1st, 2nd and 3rd stage amplifiers at 50%IDSS, 50%IDSS, and 75%IDSS respectively.

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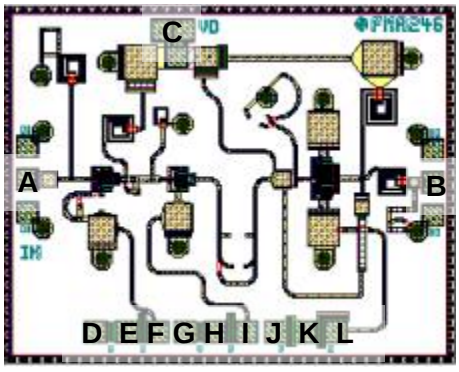
ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Supply Voltage	VDD	For any operating current	8V
Supply Current	IDD	For VDD < 7V	75% IDSS
RF Input Power	PIN	For standard bias conditions	-8dBm
Storage Temperature	TSTG	Non-Operating Storage	-40°C to 150°C
Total Power Dissipation[2,3]	PTOT	See De-Rating Note below	1400mW
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[4]		2 or more Max. Limits	80%

Notes:
[1]$T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
[2]Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) – P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power
[3]Total Power Dissipation to be de-rated as follows above 22°C:
P_{TOT}= 1.4 - (0.004W/°C) x $T_{CARRIER}$
where $T_{CARRIER}$= carrier or heatsink temperature above 22°C
(coefficient of de-rating formula is the Thermal Conductivity)
Example: For a 55°C carrier temperature: P_{TOT} = 1.4 - (0.004 x (55 – 22)) = 1.26W
[4]Users should avoid exceeding 80% of 2 or more Limits simultaneously
[5]For optimum heatsinking eutectic die attach is recommended; conductive epoxy die attach is acceptable with some degradation in thermal de-rating performance (P_{TOT} = 550mW)
[6]Thermal Resistivity: The nominal value of 250°C/W is stated for the input stage, which will reach temperature limits before the output stage. The aggregate MMIC thermal resistivity is approximately 80°C/W.

PAD LAYOUT:



Note: Co-ordinates are referenced from the bottom left hand corner of the die to the centre of bond pad opening

	PAD NAME	DESCRIPTION	PIN COORDINATES (µm)
A	IN	RFIN	104, 836
B		ROUT	1962, 822
C	VD	Drain Voltage	770, 1522
D-F		Stage 1: Source bias resistors	415/556/696,143
G-I		Stage 2: Source bias resistors	821/962/1102,143
J-L		Stage 3: Source bias resistors	1234/1374/1513, 143

DIE SIZE (µm)	DIE THICKNESS (µm)	MIN. BOND PAD PITCH (µm)	MIN. BOND PAD OPENING (µm x µm)
1624 x 2050	100	100	100 x 100

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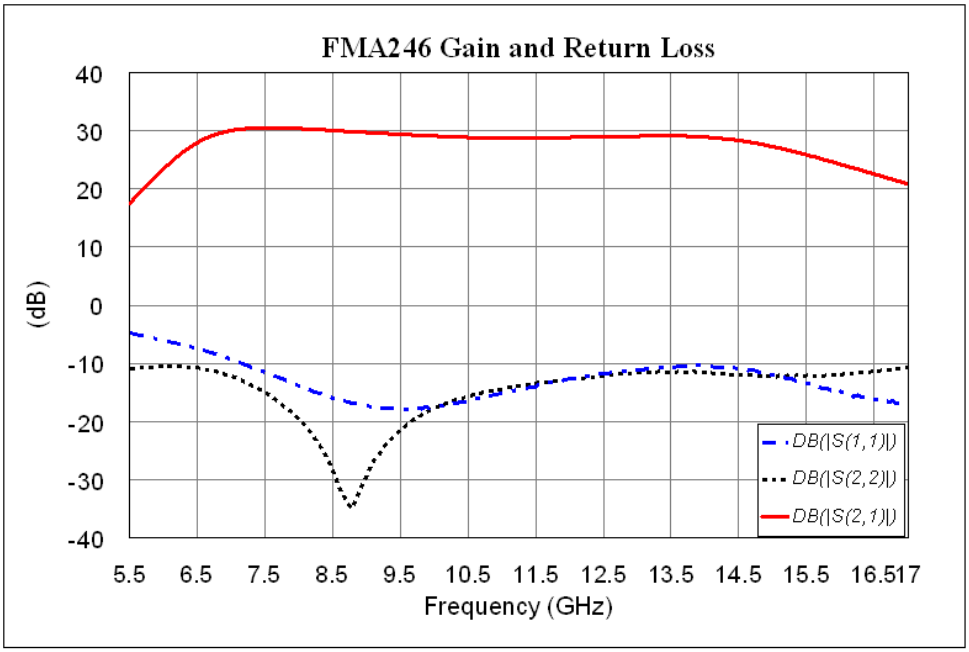
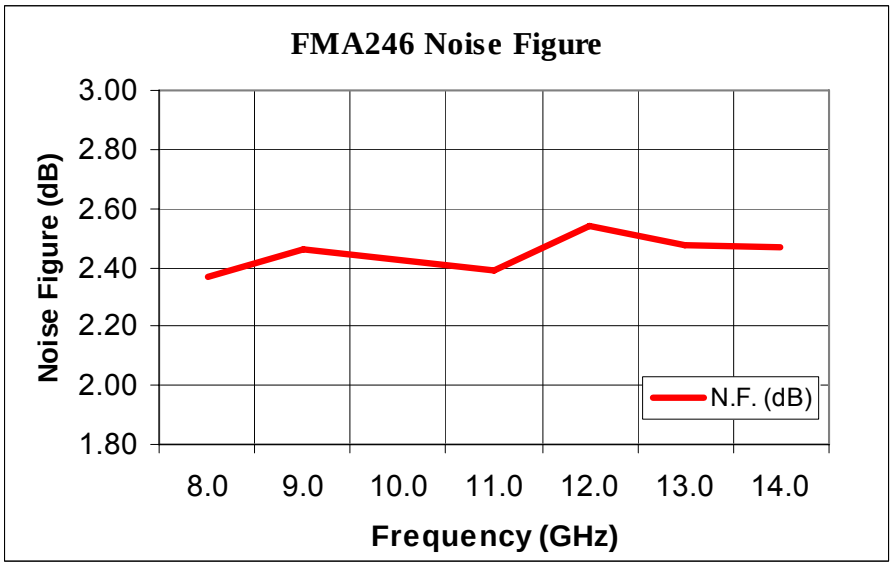
TYPICAL MEASURED PERFORMANCE:

Note: Measurement Conditions $T_{AMBIENT}$ = 22°C unless otherwise stated; (V_{DD} = +6V, I_{DD} = I_{OP})





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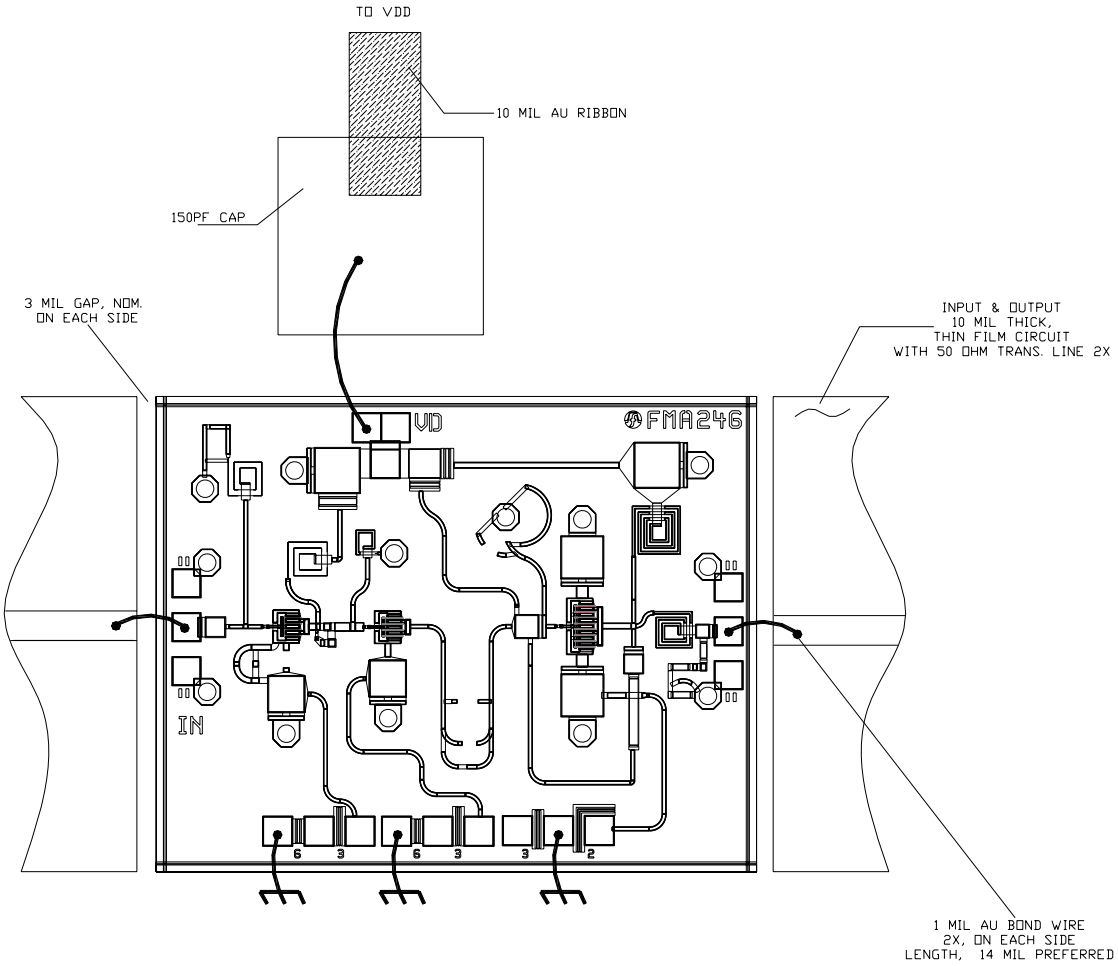
RECOMMENDED ASSEMBLY SCHEMATIC:



Note:
[1]The supply de-coupling capacitor (150 pF recommended value) should be placed as close to the MMIC as practical.
[2]The configuration shown below will result in operating current bias levels of approximately (for each stage) 50% / 50% / 75%, which is the standard recommended bias setting for the MMIC. For lower current operation, the 3rd stage can be set to 50% by bonding to the pad just to the left of the pad that is bonded in the drawing below (marked "3"), in the right-most set of three bias pads. These number markings are the resistor values (Ohms) between the pads.

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PREFERRED ASSEMBLY INSTRUCTIONS:

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The back of the die is metallised and the recommended mounting method is by the use of conductive epoxy. Epoxy should be applied to the attachment surface uniformly and sparingly to avoid encroachment of epoxy on to the top face of the die and ideally should not exceed half the chip height. For automated dispense Ablestick LMISR4 is recommended and for manual dispense Ablestick 84-1 LMI or 84-1 LMIT are recommended. These should be cured at a temperature of 150°C for 1 hour in an oven especially set aside for epoxy curing only. If possible the curing oven should be flushed with dry nitrogen. For eutectic die attach the maximum time at 280-300°C is 60 seconds, and should be kept to a minimum.

This part has gold (Au) bond pads requiring the use of gold (99.99% pure) bondwire. It is recommended that 25.4µm diameter gold wire be used. Recommended lead bond technique is thermocompression wedge bonding with 0.001" (25µm) diameter wire. The bond tool force shall be 35-38 gram. Bonding stage temperature shall be 230-240°C, heated tool (150-160°C) is recommended. Ultrasonic or thermosonic bonding is *not* recommended.

Bonds should be made from the die first and then to the mounting substrate or package. The physical length of the bondwires should be minimised especially when making RF or ground connections.

HANDLING PRECAUTIONS:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters, noise parameters and device model are available on request.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
FMA246	Die

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