FMH47N60S1FD

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FUJI POWER MOSFET

Super J-MOS series

N-Channel enhancement mode power MOSFET

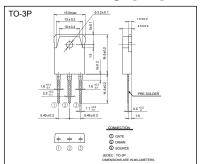
Features

Pb-free lead terminal RoHS compliant

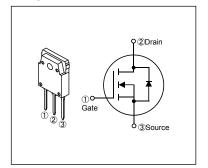
Applications

For switching

Outline Drawings [mm]



Equivalent circuit schematic



■ Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain Source Voltage	V _{DS}	600	V	
Drain-Source Voltage	V _{DSX}	600	V	V _{GS} =-30V
Continuous Drain Current	Io	±47	Α	Tc=25°C Note*1
Continuous Drain Current		±29.7	Α	Tc=100°C Note*1
Pulsed Drain Current	I _{DP}	±141	Α	Note*1
Gate-Source Voltage	V _{GS}	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	Iar	9.5	А	Note *2
Non-Repetitive Maximum Avalanche Energy	Eas	1689.9	mJ	Note *3
Maximum Drain-Source dV/dt	dV⊳s/dt	50	kV/µs	V _{DS} ≤ 600V
Peak Diode Recovery dV/dt	dV/dt	25	kV/µs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/µs	Note *5
Maximum Dawar Dissination	P₀	2.5	W	T _a =25°C
Maximum Power Dissipation		390	VV	Tc=25°C
One and it is an all Changes Towns and the same	T _{ch}	150	°C	
Operating and Storage Temperature range	T _{stg}	-55 to +150	°C	

Eas limited by maximum channel temperature and avalanche current. Note *4 : IF \le -ID, -di/dt=100A/ μ s, VDs peak \le 600V, Tch \le 150°C.

Note *5 : IF \leq -ID, dV/dt=25kV/ μ s, VDs peak \leq 600V, Tch \leq 150°C.

■ Electrical Characteristics at T_c=25°C (unless otherwise specified) Static Ratings

Parameter	Symbol	Conditions	,	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA V _{GS} =0V		600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	I _D =2mA V _{DS} =V _{GS}		3	4	5	V
Zero Gate Voltage Drain Current	loss	V _{DS} =600V V _{GS} =0V	T _{ch} =25°C	-	-	25	μА
		V _{DS} =480V V _{GS} =0V	T _{ch} =125°C	-	250	-	
Gate-Source Leakage Current	Igss	V _{GS} = ± 30V V _{DS} =0V		-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	I _D =23.5A V _{GS} =10V		-	0.062	0.074	Ω
Gate resistance	R _G	f=1MHz, open drain		-	1.1	-	Ω

Note *1 : Limited by maximum channel temperature. Note *2 : $T_{ch} \le 150^{\circ}C$, See Fig.1 and Fig.2 Note *3 : Starting $T_{ch} = 25^{\circ}C$, Ias=5.7A, L=95.4mH, VDD=60V, RG=50 Ω , See Fig.1 and Fig.2

Dynamic Ratings

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	G fs	I _D =23.5A V _{DS} =25V	17	35	-	S
Input Capacitance	Ciss	V _{DS} =400V	-	3600	-	
Output Capacitance	Coss	V _{GS} =0V	-	105	-	
Reverse Transfer Capacitance	Crss	f=250kHz	-	7.5	-	
Effective output capacitance, energy related (Note *6)	C _{o(er)}	V _{DS} =0V V _{DS} =0400V	-	275	-	pF
Effective output capacitance, time related (Note *7)	C _{o(tr)}	V _{GS} =0V V _{DS} =0400V ID=constant	-	945	-	
Turn-On Time	t _{d(on)}		-	146	-	
Turn-On Time	tr	V _{DD} =400V, V _{GS} =10V I _D =23.5A, R _G =13Ω	-	32	-	ns
Turn-Ott Time	t _{d(off)}	See Fig.3 and Fig.4	-	169	-	
	t _f		-	19	-	
Total Gate Charge	Q _G		-	127	-	
Gate-Source Charge	Q _{GS}	V _{DD} =400V, I _D =47A	-	33	-	nC
Gate-Drain Charge	Q _{GD}	─ V _{ss} =10V _ See Fig.5	-	55	-	nC
Drain-Source crossover Charge	Qsw		-	16	-	1

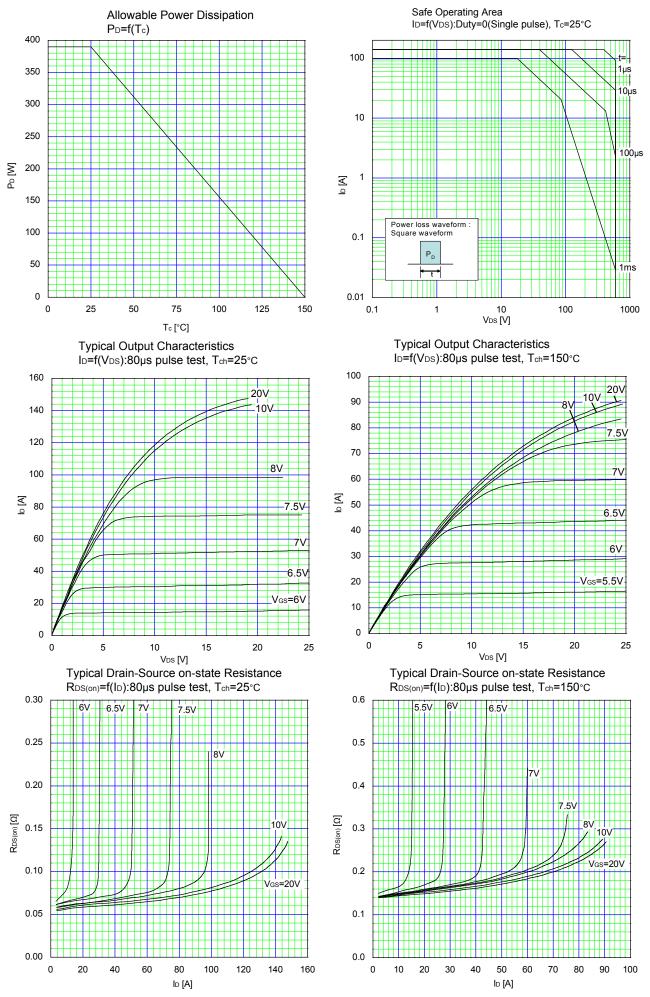
Note *6 : $C_{0(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while Vos is rising from 0 to 400V. Note *7 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while Vos is rising from 0 to 400V.

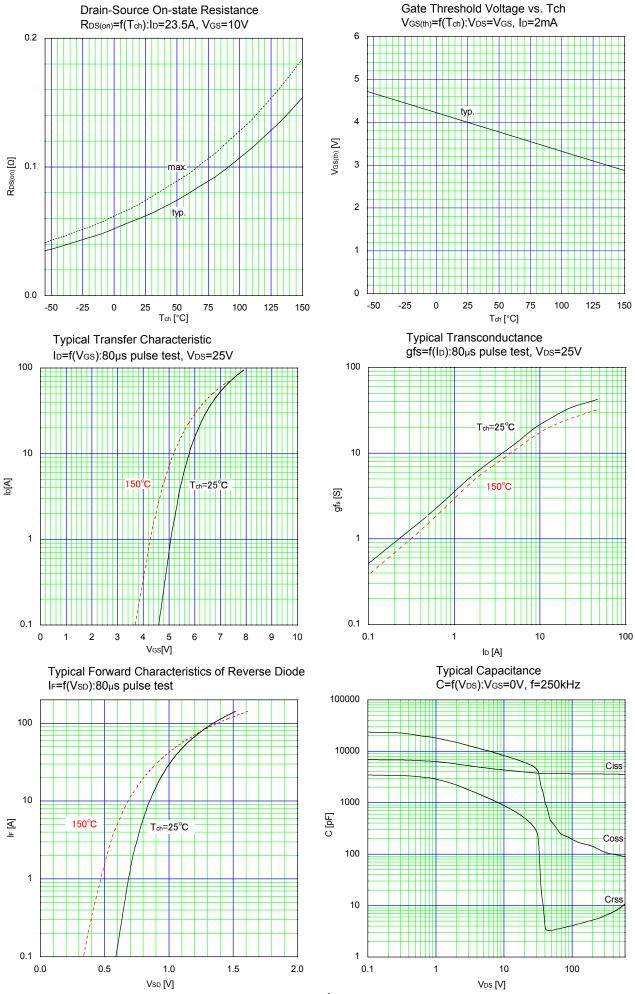
• Reverse Diode

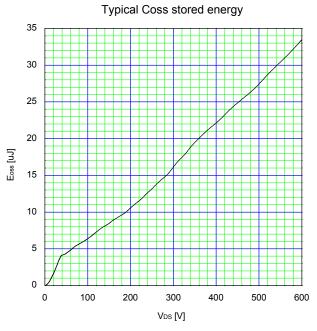
Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	lav	L=20.6mH,T _{ch} =25°C See Fig.1 and Fig.2	9.5	-	-	А
Diode Forward On-Voltage	V _{SD}	I _F =47A,V _{GS} =0V T _{ch} =25°C	-	1.1	1.35	V
Reverse Recovery Time	trr	I _F =47A, V _{DD} =400V -di/dt=100A/μs T _{ch} =25°C See Fig.6 and Fig.7	-	210	-	ns
Reverse Recovery Charge	Qrr		-	1.6	-	μC
Peak Reverse Recovery Current	Irp		-	15	-	А

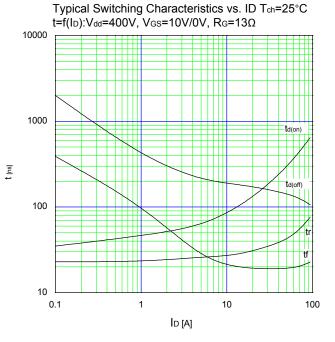
■ Thermal Resistance

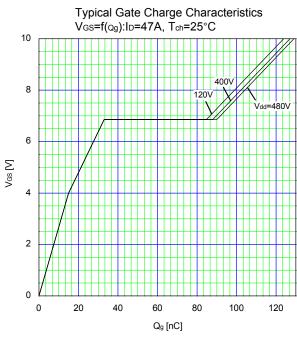
Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	R _{th(ch-c)}	-	-	0.32	°C/W
Channel to Ambient	R _{th(ch-a)}	-	-	50	°C/W

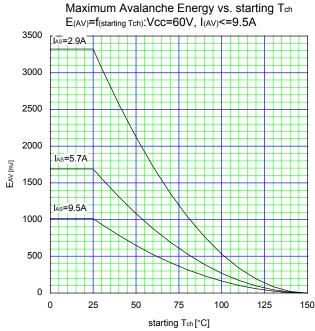


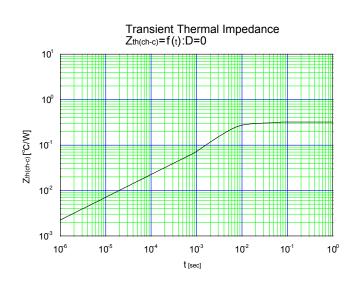












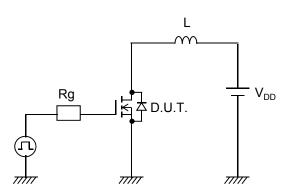


Fig.1 Avalanche Test circuit

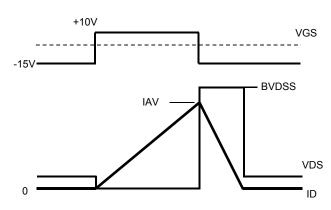


Fig.2 Operating waveforms of Avalanche Test

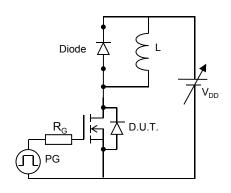


Fig.3 Switching Test circuit

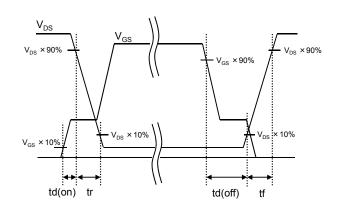


Fig.4 Operating waveform of Switching Test

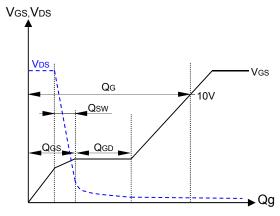


Fig.5 Operating waveform of Gate charge Test

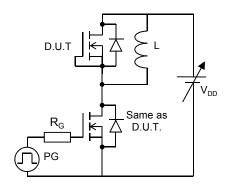


Fig.6 Reverse recovery Test circuit

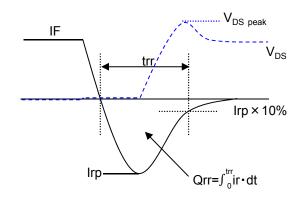
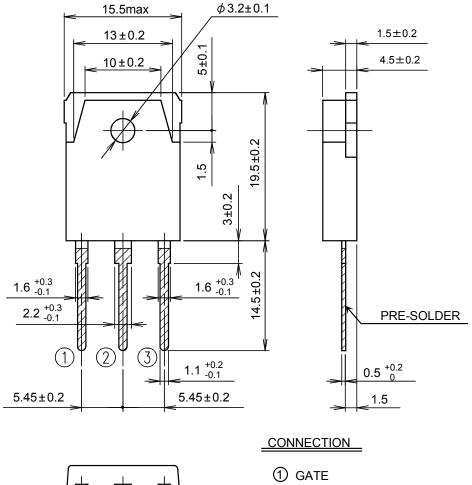


Fig.7 Operating waveform of Reverse recovery Test

Outview: TO-3P Package

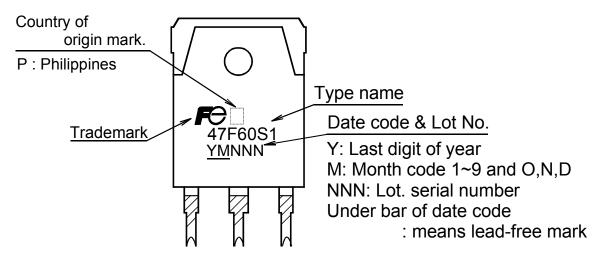


- + + +
- 2 DRAIN
- 3 SOURCE

JEDEC: TO-3P

DIMENSIONS ARE IN MILLIMETERS.

Marking



^{*} The font (font type,size) and the trademark-size might be actually different.

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