FMN4xT2TCK-25Ix Datasheet

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Document Title

Stacked Multi-Chip Product (NAND=4G, LPDDR2=2G)

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Nov. 1st, 2014	Preliminary
0.1	Revised IDD Specification of DRAM	Nov. 4th, 2014	
0.2	Revised IDD Specification of DRAM	Mar. 24th, 2015	
0.3	Revised Package Dimension (8.0mm X 10.5mm)	Jun. 2nd, 2015	Final

Stacked Multi-Chip Product(MCP)

1.8V NAND Flash Memory and Mobile DDR2

1. MCP Features

- Operating Temperature Range
  - Industrial Part : - 40°C ~ 85°C

- Package Type :
  - 162-ball FBGA, 11.5x13.0mm^2, 1.0T, 0.5mm Ball Pitch
  - 162-ball FBGA, 8.05x10.5mm^2, 0.8T, 0.5mm Ball Pitch
  - Lead & Halogen Free

◆ NAND

- Architecture (4G bits)
  - Input / Output Bus Width: 8-bits / 16-bits
  - Page size
    - X 8 : (2K+64spare) bytes (@1.8V)
    - X16 : (1K+32spare) words (@1.8V)
    - – Block size
    - X8 : (128K+4K) bytes
    - X16 : (64K+2K) words
    - – Plane Size: 2048 Blocks
    - – Device Size: 2 Planes per Device
- Page Read / Program
  - Random Read Time (tR): 30 µs (Max)
  - Sequential Access Time: 45 ns (Min)
  - Page Program: 300 µs (Typ)
- Block Erase / Multi-plane Erase
  - Block Erase time: 3.5 ms (Typ)
- Security
  - OTP area
  - Serial Number (unique ID)
  - Serial access : 45ns (1.8V)
- Supply Voltage
  - 1.8V device: VCC = 1.7V ~ 1.95V
- Reliability
  - 50,000 Program / Erase cycles (with 4-bit ECC per 528 bytes)
  - 10 Year Data retention

◆ DRAM

- VDD2 = 1.14–1.30V
- VDDCA/VDDQ = 1.14–1.30V
- VDD1 = 1.70–1.95V
- Interface : HSUL_12
- Data width : x32
- Clock frequency : 400 MHz
- Four-bit pre-fetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data(DQS/DQS#).
- DM masks write date at the both rising and falling edge of the data strobe
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Auto refresh and self refresh supported
- All bank auto refresh and per bank auto refresh supported
- Clock stop capability

- Low Power Features
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - PASR (Partial Array Self Refresh) power-saving mode.
  - DPD (Deep Power Down) Mode.
  - DS (Driver Strength) Control.

2. MCP Selection Guide

MCP Part Number2	Flash	LP-DRAM2	DRAM Freq.	Individual Datasheet		PKG Type
				Flash	LP-DRAM	
FMN4ST2TCK-25IF	4Gb x16	2Gb x32	400MHz	FMND4G16S3K	FMT8E32UAx-25Ix	162 ball
FMN4ET2TCK-25IF	4Gb x8	2Gb x32	400MHz	FMND4G08S3K	FMT8E32UAx-25Ix	162 ball
FMN4ST2TCK-25IG	4Gb x16	2Gb x32	400MHz	FMND4G16S3K	FMT8E32UAx-25Ix	162 ball(Small)
FMN4ET2TCK-25IG	4Gb x8	2Gb x32	400MHz	FMND4G08S3K	FMT8E32UAx-25Ix	162 ball(Small)

3. MCP Part Numbering System

F M N X X X X X X X-X X X X X

Fidelix Memory

Product Family
N : NAND + Mobile DRAM MCP

Flash Density/Org.
6 : 256M E: x8
5 : 512M S: x16
1 : 1G
2 : 2G
4 : 4G

SDR/DDR
S : SDR
D : DDR
T : DDR2

SDR/DDR Density/Org.
3 : 128M S: x16
6 : 256M T: x32
5 : 512M D: x32 (Double Stack)
1 : 1G
2 : 2G

Core/IO Voltage(Flash/DRAM)
A : 3.3V/1.8V
B : 1.8V/1.8V
C : 1.8V/1.2V

Generation
K

DRAM Speed
15 : 66MHz
12 : 83MHz
10 : 100MHz
75 : 133MHz
60 : 166MHz
50 : 200MHz
25 : 400MHz
18 : 533MHz

Temperature
C : 0℃~70℃
E : -25℃~85℃
I : -40℃~85℃

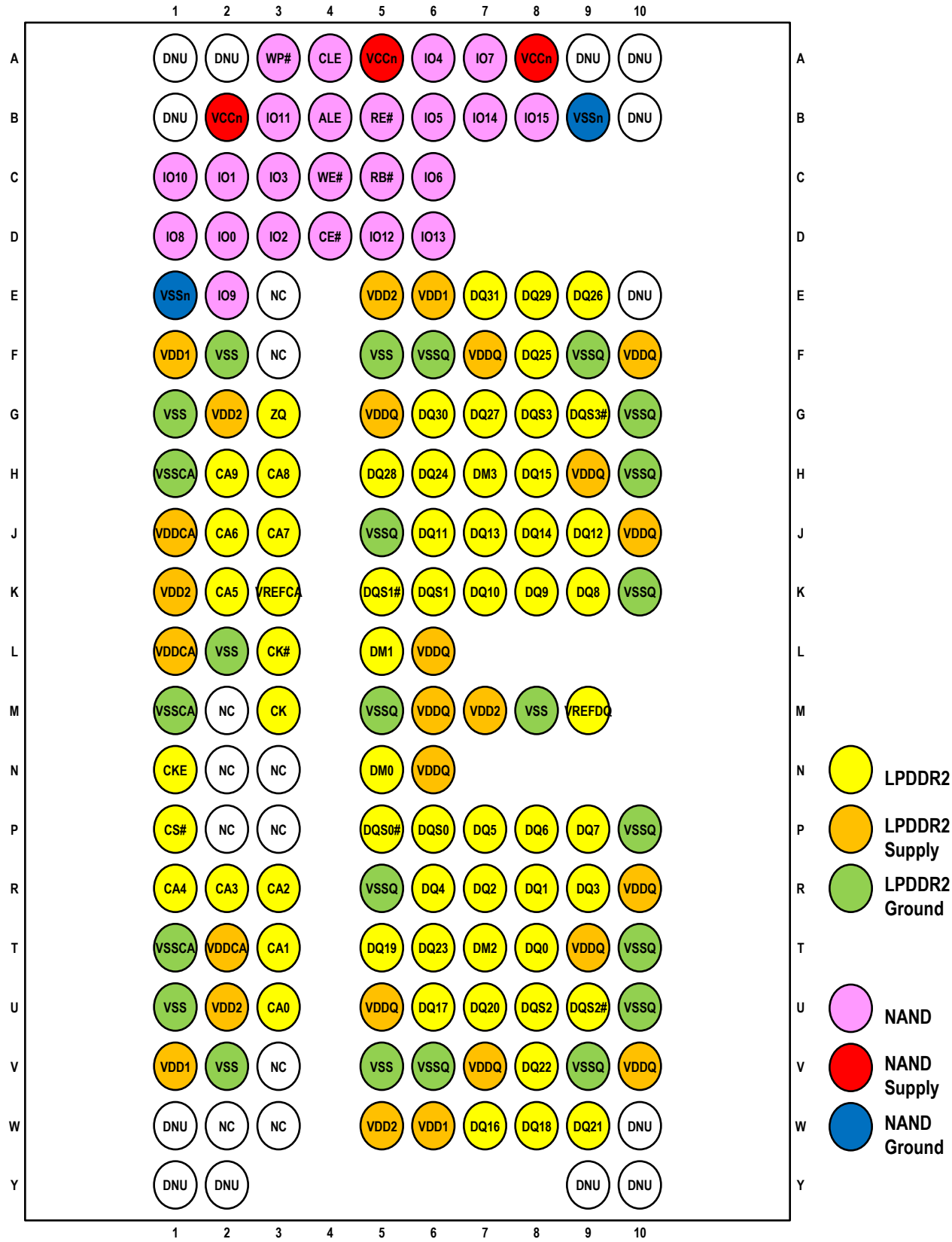
Package Type
A : 8x9mm^2, 130-ball FBGA, 1.0T max
B : 10.5x13mm^2, 137-ball FBGA,1.2T max
C : 10.5x13mm^2, 107-ball FBGA,1.2T max
D: 8x9mm^2, 130-ball FBGA, 1.2T max
E : 8x8mm^2, 121-ball FBGA, 0.86T max
F : 11.5x13.0mm^2, 162-ball FBGA, 1.0T max
G : 8x10.5mm^2, 162-ball FBGA, 0.8T max

Packing Type
R : Tape and Reel
Blank : Tray

4-1. MCP Package Pin Configuration (162-ball FBGA, Top View)

Pin Configuration – 162Ball MCP(X16/X32)

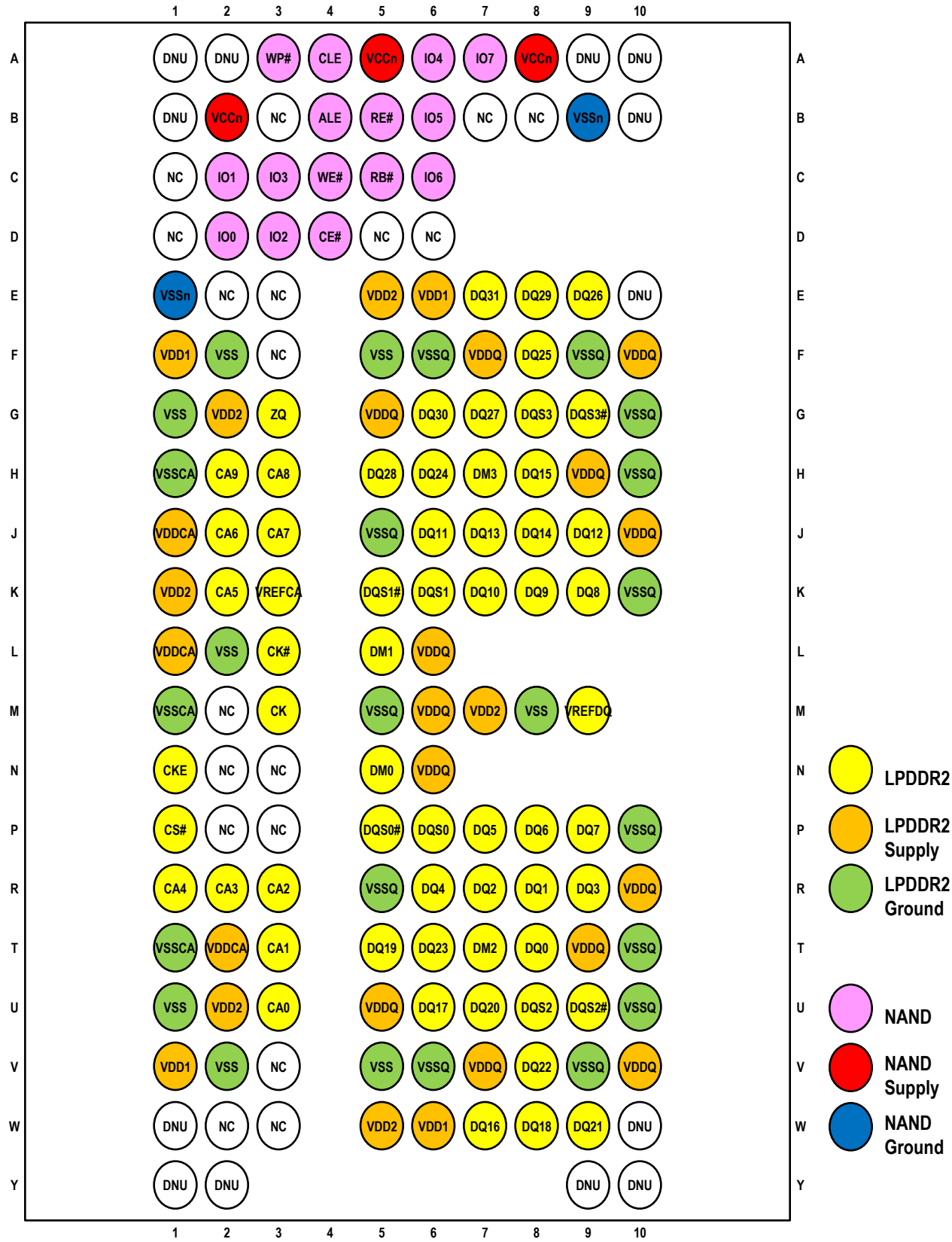
Top View (Ball Down)



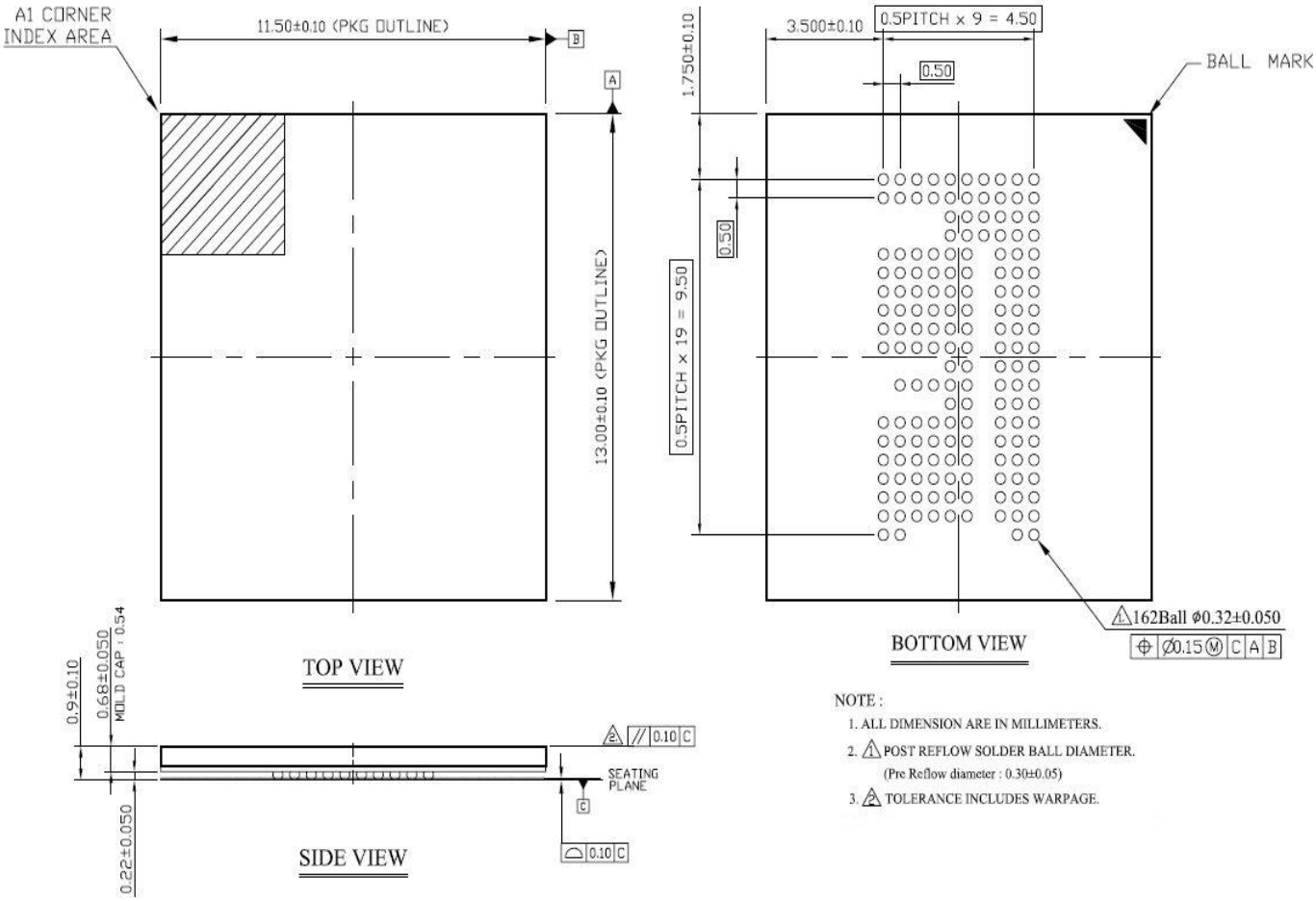
4-2. MCP Package Pin Configuration (162-ball FBGA, Top View)

Pin Configuration – 162Ball MCP(X8/X32)

Top View (Ball Down)

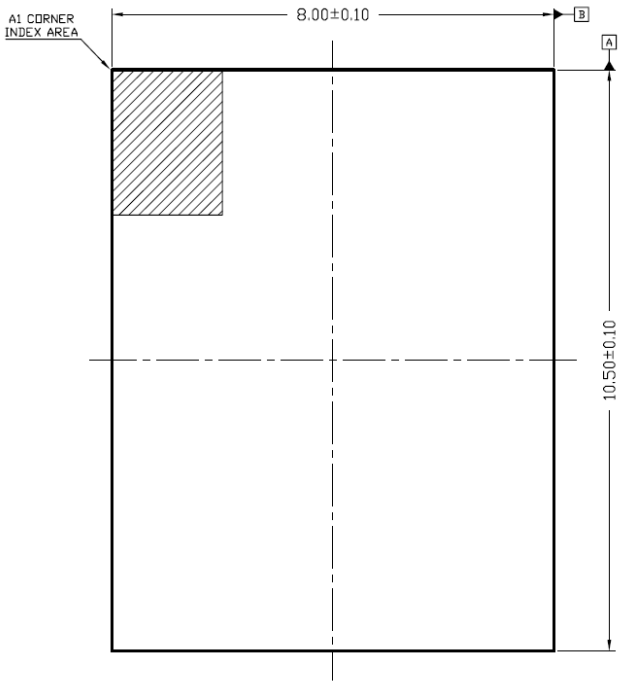


5-1. Package Dimension (11.5mm x 13.0mm) – 162Ball FBGA(X32)

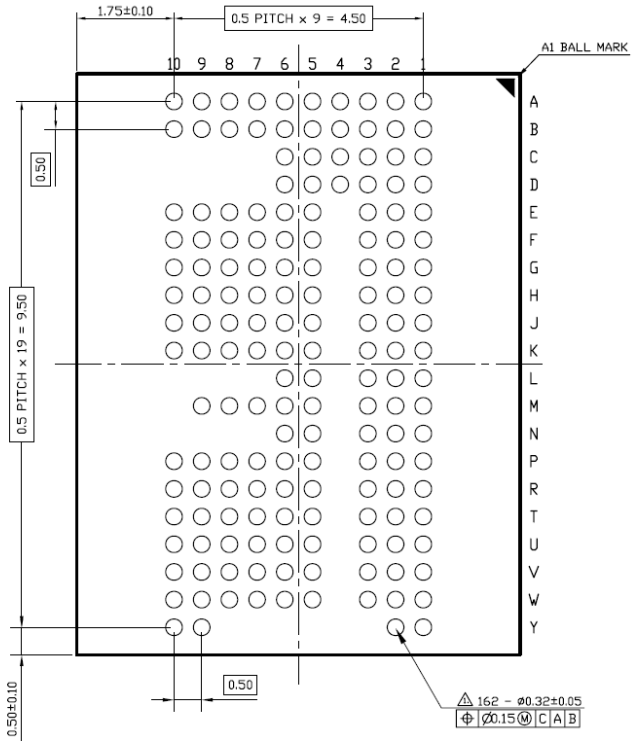


NOTE :
1. ALL DIMENSION ARE IN MILLIMETERS.
2. ⚠1 POST REFLOW SOLDER BALL DIAMETER.
(Pre Reflow diameter : 0.30±0.05)
3. ⚠2 TOLERANCE INCLUDES WARPAGE.

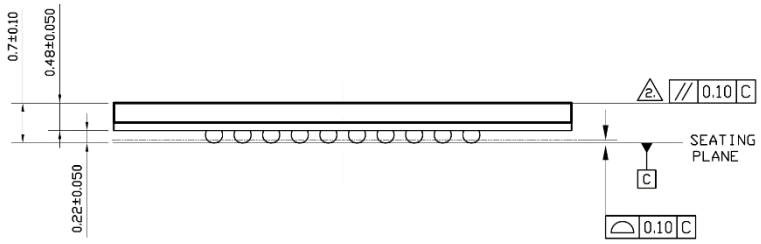
5-2. Package Dimension (8.0mm x 10.5mm) – 162Ball FBGA(X32)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE :

1. ALL DIMENSION ARE IN MILLIMETERS.
2. ⚠1 POST REFLOW SOLDER BALL DIAMETER. (Pre Reflow Diameter : 0.30±0.02)
3. ⚠2 TOLERANCE INCLUDES WARPAGE.

SLC NAND FLASH

(FMND4GxxS3K)

Document Title

4Gbit SLC NAND FLASH

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Sep. 1th , 2014	Preliminary

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Distinctive Characteristics

■ Density
– 4 G bits

■ Architecture
– Input / Output Bus Width: 8-bits / 16-bits
– Page size
X 8 : (2K+64spare) bytes (@1.8V)
X16 : (1K+32spare) words (@1.8V)
– Block size
X8 : (128K+4K) bytes
X16 : (64K+2K) words
– Plane Size: 2048 Blocks
– Device Size: 2 Planes per Device

■ Page Read / Program
– Random Read Time (tR): 30 µs (Max)
– Sequential Access Time: 45 ns (Min)
– Page Program: 300 µs (Typ)

■ Block Erase / Multi-plane Erase
– Block Erase time: 3.5 ms (Typ)

■ Command Set
– Open NAND Flash Interface (ONFI) 1.0 compliant

■ Security
– OTP area
– Serial Number (unique ID)

■ Supply Voltage
– 1.8V device: VCC = 1.7V ~ 1.95V

■ Operating Temperature
– Industrial: -40°C to 85°C

■ Reliability
– 50,000 Program / Erase cycles
(with 4-bit ECC per 528 bytes)
– 10 Year Data retention

1. SUMMARY DESCRIPTION

The Fidelix FMND4GxxS3K series is offered in 1.8 VCC and VCCQ power supply, and with x8 or x16 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. (2048 + 64 spare custom device) bytes or (1024 + 32 spare custom device) words.

Each block can be programmed and erased up to 50,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND flash devices, the implementation of an ECC is mandatory.

The chip supports CE# don't care function. This function allows the direct download of the code from the NAND flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.

In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages at a time (one per each plane) or to erase 2 blocks at a time (again, one per each plane). As a consequence, multi-plane architecture allows program/erase time to be reduced by 50%. The multi-plane operations are supported both with traditional and ONFI 1.0 protocol. Data in the page can be read out at 45nsec cycle time per byte.

The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.

The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data.

In addition, device supports ONFI 1.0 specification. The copy-back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. We don’t have EDC function in this device.

A write protect pin is available to provide hardware protection against program and erase operations. The devices feature an open-drain ready/busy output that identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to connect to a single pull-up resistor. The devices have a cache read feature that improves the read throughput for large files. During cache reading, the devices loads the data in a cache register while the previous data is transferred to the I/O buffers to be read. This feature is implemented according to ONFI 1.0 specification.

1.1 Pin Description

Pin Name	Description
I/O0 - I/O7 Or I/O8 - I/O15	**DATA INPUTS/OUTPUTS** The I/O pins is used to COMMAND LATCH cycle, ADDRESS INPUT cycle, and DATA in-out cycles during read / write operations. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
CE#	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, CE# low does not deselect the memory. The device goes into Stand-by mode when CE# goes High during the device is in Ready state. The CE# signal is ignored when device is in Busy state, and will not enter Standby mode even if the CE# goes high.
WE#	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**WRITE PROTECT** The WP# pin, when Low, provides a hardware protection against undesired write operations. Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.
RB#	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
V_{CC}	**SUPPLY VOLTAGE FOR IO BUFFER** The VCC supplies the power for all the operations. (Read, Write, and Erase).
V_{SS}	**GROUND**
NC	**NO CONNECTED / DON'T USE**

Table 1. Pin Description

Notes:

1. A 0.1uF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.2 Pin Diagram

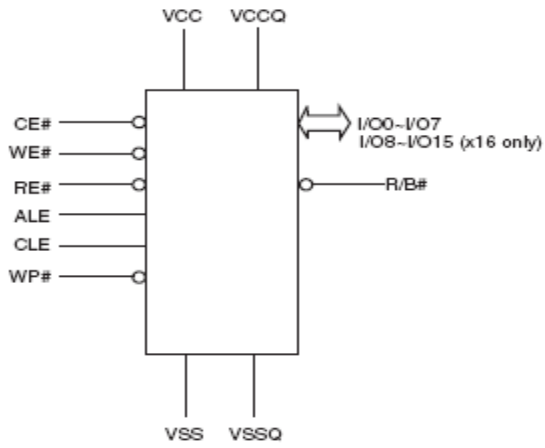


Figure 1. Pin Diagram

1.3 Block Diagram

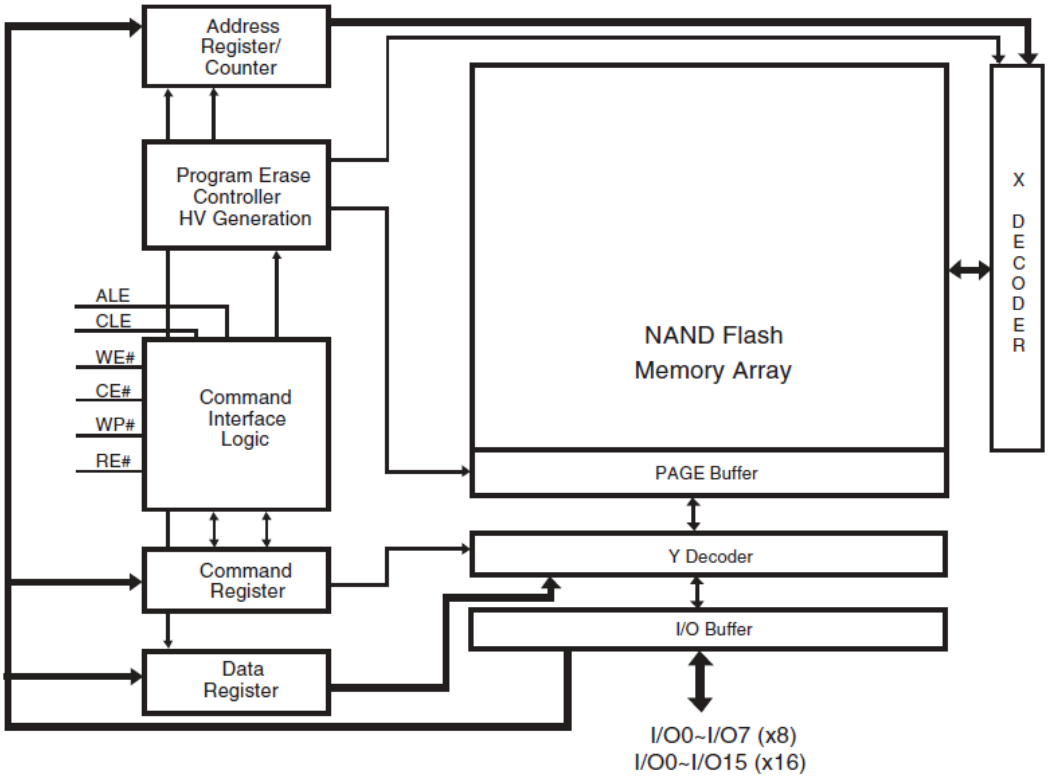


Figure 2. Block Diagram

1.4 Array Organization

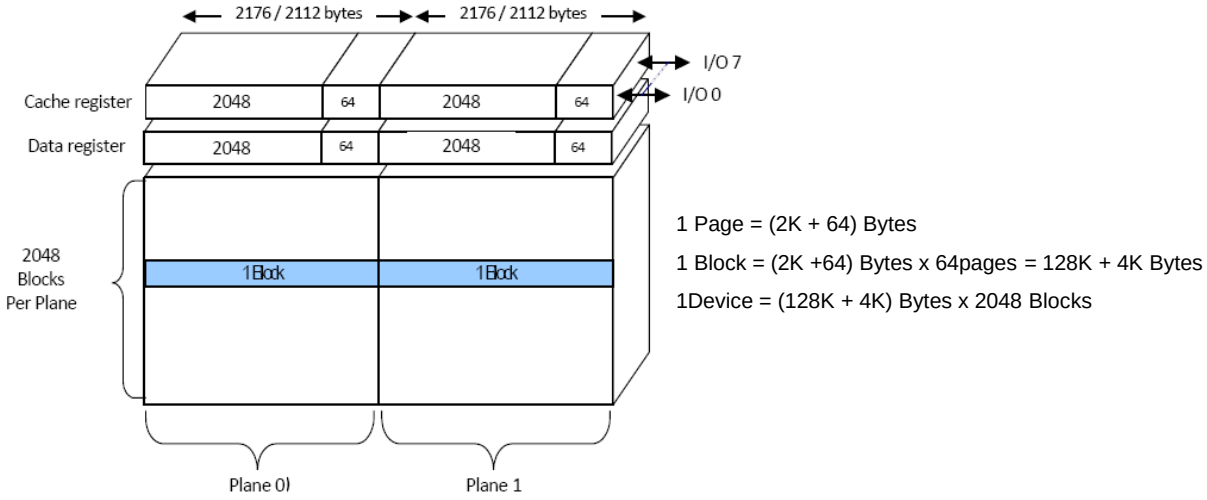


Figure 3. Array Organization – x8

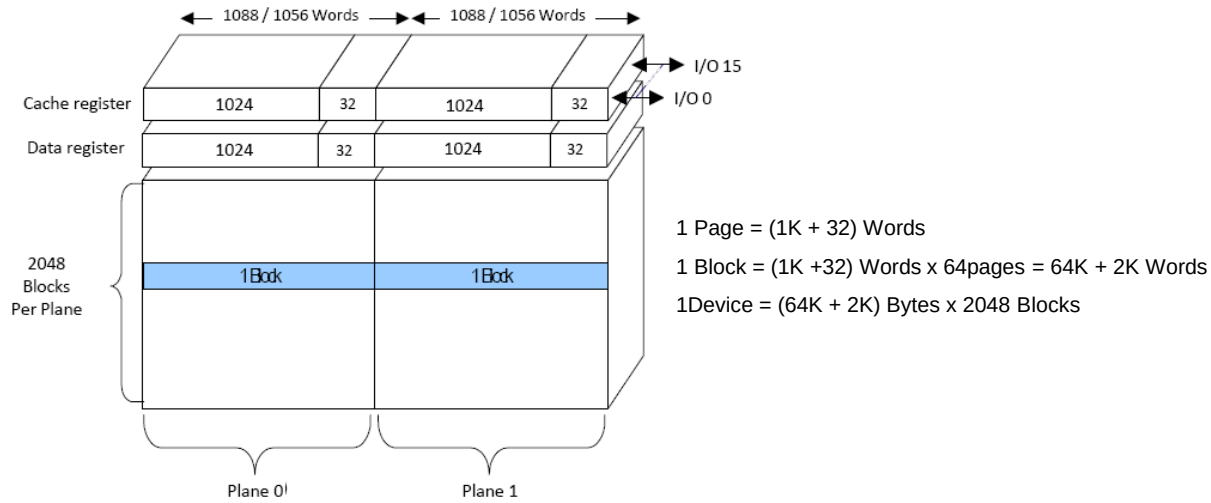


Figure 4. Array Organization - x16

1.5 Addressing

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th(*)Cycle	A28	A29	A30	A31	L(1)	L(1)	L(1)	L(1)

Table 2. Addressing – x8

(*): A30 for 8Gbit DDP(1CE). A30:A31 for 16Gbit QDP(1CE).
As far as the address bits are concerned, the following rules apply:
A0 -A11 : column address in the page
A12 -A17 : page address in the block
A18 : plane address (for multi-plane operations) / block address (for normal operations)
A19 -A31 : block address

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	L(1)	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26
5th(*)Cycle	A27	A28	A29	A30	L(1)	L(1)	L(1)	L(1)

Table 3. Addressing – x16

(*): A29 for 8Gbit DDP(1CE). A29:A30 for 16Gbit QDP(1CE)
As far as the address bits are concerned, the following rules apply:
A0 -A10 : column address in the page
A11 -A16 : page address in the block
A17 : plane address (for multi-plane operations) / block address (for normal operations)
A18 -A30 : block address

Notes:
1. L must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 5th cycle are Row Address.
4. I/O 8 -I/O 15 must be L.

1.6 Command Set

FUNCTION	1st Cycle	2nd Cycle	3nd Cycle	4th Cycle	Acceptable command during busy
PAGE READ	00h	30h	-	-	No
READ FOR COPY-BACK	00h	35h	-	-	No
SPECIAL READ FOR COPY BACK	00h	36h	-	-	No
READ ID	90h	-	-	-	No
READ ID2	30h-65h-00h	30h	-	-	No
RESET	FFh	-	-	-	Yes
PAGE PROGRAM(Start) CACHE PROGRAM(End)	80h	10h	-	-	No
CACHE PROGRAM(Start)	80h	15h	-	-	No
PAGE RE-PROGRAM	8Bh	10h	-	-	No
COPY BACK PROGRAM	85h	10h	-	-	No
(Traditional) MULTI PLANE PROGRAM	80h	11h	81h	10h	No
ONFI MULTIPLANE PROGRAM	**80h**	**11h**	**80h**	**10h**	**No**
MULTIPLANE PAGE RE-PROGRAM	8Bh	11h	8Bh	10h	No
(Traditional) MULTI PLANE CACHE PGM(start/cont)	80h	11h	81h	15h	No
ONFI MULTIPLANE CACHE PGM(start/cont)	**80h**	**11h**	**80h**	**15h**	**No**
(Traditional)MULTI PLANE CACHE PGM(end)	80h	11h	81h	10h	No
ONFI MULTIPLANE CACHE PGM(end)	**80h**	**11h**	**80h**	**10h**	**No**
(Traditional) MULTI PLANE COPY BACK PROGRAM	85h	11h	81h	10h	No
ONFI MULTI PLANE COPY BACK PROGRAM	**85h**	**11h**	**85h**	**10h**	**No**
BLOCK ERASE	60h	D0h	-	-	No
(Traditional) MULTI PLANE BLOCK ERASE	60h	60h	D0h	-	No
ONFI MULTIPLANE BLOCK ERASE	**60h**	**D1h**	**60h**	**D0h**	**No**
READ STATUS REGISTER	70h	-	-	-	Yes
READ STATUS ENHANCED	**78h**	-	-	-	**Yes**
RANDOM DATA INPUT	85h	-	-	-	No
RANDOM DATA OUTPUT	05h	E0h	-	-	No
CACHE READ (SEQUENTIAL)	31h	-	-	-	No
CACHE READ ENHANCED (RANDOM)	00h	31h	-	-	No
CACHE READ(End)	3Fh	-	-	-	No
READ PARAMETER PAGE	ECh	-	-	-	No
EXTENDED READ STATUS	F2/F3/F4/F5h				Yes

Table 4. Command Set

1.7 Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 Cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H [1)]	L	Rising	H	H		Address Input (5 Cycles)
L	L	L	Rising	H	H	Data Input	
L	L [1)]	L	H	Falling	X	Sequential Read and Data Output	
X	X	L [1)]	H	H	X	Data Output(suspended)	
L	L	L	H [3)]	H [3)]	X	During Read (Busy)	
X	X [1)]	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc [2)]	Stand-By	

Table 5. Mode Selection

Notes:
1. X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and Multi Plane Read Status can be inputted to the device.

2. Bus Operation

There are six standard bus operations that control the device: Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. Typically glitches less than 5ns on Chip Enable, Write Enable, and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 6 and “5.7. AC Timing Characteristics" for details of the timings requirements.

2.2 Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. (Refer to “1.5. Addressing”). Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation(write/erase) the Write Protect pin must be high. See Figure 7 and “5.7. AC Timing Characteristics” for details of the timings requirements.

2.3 Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 8 and “5.7. AC Timing Characteristics" for details of the timings requirements.

2.4 Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 9 to Figure 10 and “5.7. AC Timing Characteristics" for details of the timings requirements.

2.5 Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby

In Standby, the device is deselected, outputs are disabled, and power consumption is reduced.

3. Device Operation

3.1 Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2176 bytes (x8) or 1088 (x16) of data within the selected page are transferred to the data registers in less than 30us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 45nsec cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.

Check Figure 12 to Figure 14 as references.

3.2 Page Program

A page program cycle consists of a serial data loading period in which up to 2176 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded.

The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 17 to Figure 19 detail the sequence.

The device is programmed basically by page, but it also allows multiple partial page programming of a word or consecutive bytes up to 2176 (x8) or 1088 (x16) in a single page program cycle. The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. For example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

3.3 Page Reprogram

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. See Figure 33 for details.

On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm “10h”. See Figure 34 for details.

During page-re-program, address limitation applies as described in Figure 20 note 1 and 2 for copy-back function.

Similarly, the multi-plane page re-program allows to re-program two pages in parallel, one per each plane. The first page must be in the first plane while the second page must be in the second plane; the multi-plane page re-program operation is performed after a previously failed multi-plane page program operation. As for single page re-program case, multi-plane page re-program can be issued without any data manipulation (see Figure 35 for details) or with data manipulation (see Figure 36 for details). During multi-plane page-re-program, address limitation applies as described in Figure 28 notes 1 and 2 for multi-plane copy-back function.

3.4 Multi-plane Program

Device supports multi-plane program: it is possible to program 2 pages in parallel, one per each plane.

A multi-plane program cycle consists of a double serial data loading period in which up to 4352bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. Address for this page must be in the 1st plane(A18=0 for x8 devices, A17=0 for x16 devices). The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (tDBSY).

Once it has become ready again, either the traditional "81h" or the ONFI 1.0 "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be in the 2nd plane (A18=1 for x8 devices, A17=1 for x16 devices).Program Confirm command (10h) makes parallel programming of both pages to start. Figure 24 and Figure 25 describe the sequences.

User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program: read status register command is also available during Dummy Busy time (tDBSY). In case of fail in any of 1st and 2nd page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "read status enhanced" command must be issued Refer to section 3.10 for further info.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

3.5 Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A18 to A28 are valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. See Figure 22 for details.

3.6 Multi-plane Block Erase

Multi-plane erase, allows parallel erase of two blocks in parallel, one per each memory plane. Two different command sequences are allowed in these case, traditional and ONFI 1.0.

In traditional case, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start. In this case, multi-plane erase does not need any Dummy Busy Time between 1st and 2nd block insertion. See Figure 26 for details.

As an alternative, the ONFI 1.0 multi-plane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multi-plane confirm). Between the two block-related sequences, a short busy time tIEBSY will occur. See Section 5.8 and Figure 27 for details.

Address limitation required for multi-plane program applies also to multi-plane erase. Also operation progress can be checked like in the multi-plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced.

As for multi-plane page program, the address of the first second page must be within the first plane (A18=0 for x8 devices, A17=0 for x16 devices) and second plane (A18 = 1 for devices, A17=1 for x16 devices), respectively.

3.7 Copy Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block.

The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2176 bytes(x8 Device) or 1088 words(x16 Device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or copy-back command (85h) with the address cycles of destination page may be written.

The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 20"Copy-back Program with Random Data Input". When there is a program-failure at copy-back operation, error is reported by pass/fail status. But, if copy-back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, four bit error correction is recommended for the use of copy-back operation. Figure 20shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random

Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy-back, while it must be set to Vcc. When performing the program. During copy-back operation, address limitation applies as described in Figure 20 notes 1 and 2.

3.8 Multi-plane Copy Back Program

As for page program, device supports multi-plane copy-back program with exactly same sequence and limitations. Multi-plane copy-back program must be preceded by 2 single page read for copy-back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).

Multi-plane copy-back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.

Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) represented in Figure 28, and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h) represented in Figure 29 and Figure 30.

During multi-plane copy-back operation, address limitation applies as described in Figure 28 notes 1 and 2.

3.9 Special Read for Copy Back

The device features the "special read for copy-back".
If copy-back read (described in sections 3.7 and 3.8) is triggered with confirm command "36h" instead "35h", copy-back read from target page(s) will be executed with an increased internal (Vpass) voltage. This special feature is used in order to try to recover incorrigible ECC read errors due to over-program or read disturb: it shall be used ONLY if ECC read errors have occurred in the source page using "standard read" or "standard read for copy-back" sequences.. Excluding the copy-back read confirm command, all other features described in sections 3.7 and 3.8 for standard copy-back remain valid (including the figures referred to in those sections).

3.10 Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to “Table 7. Status Register Coding" for specific Status Register definitions, and Figure 11Afor specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

3.11 Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation on a specific plane in case of multi-plane operations.

Figure 11B defines the Read Status Enhanced behavior and timings. The plane address must be specified in the command sequence in order to retrieve the status of the plane of interest.

Refer to Table 7for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.

Status register is dynamic in other words, user is not required to toggle RE# / CE# to update it.

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program	Coding
0	Pass / Fail	Pass / Fail	N/A	N/A	Pass / Fail (N)	N page Pass : '0' Fail : '1'
1	N/A	N/A	N/A	N/A	Pass / Fail (N-1)	N -1 page Pass : '0' Fail : '1'
2	N/A	N/A	N/A	N/A	N/A	-
3	N/A	N/A	N/A	N/A	N/A	-
4	N/A	N/A	N/A	N/A	N/A	-
5	Ready / Busy	Ready / Busy	Ready / Busy	P/E/R Controller Bit	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	N/A	Write Protect	Protected : '0' Not Protected : '1'

Table 7. Status Register Coding

Notes:

1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2. I/O1: This bit is only valid for Cache Program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache Program sequence. When Cache Program is not supported, this bit is not used.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4. I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the last operation is complete.

3.12 Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to table 7 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for tRST after the Reset command is written. Refer to Figure 23 for further details.

3.13 Cache Read (available only within a block)

The Cache Read Sequential and Cache Read Random functions permit a page to be read from the page register while another page is simultaneously read from the Flash array. A Page Read command, as defined in table 4, shall be issued prior to the initial Cache Read Sequential or Cache Read Random command in a Cache Read sequence. A Cache Read Sequential or Cache Read Random command shall be issued prior to a Cache Read End (3Fh) command being issued.

The Cache Read (Sequential or Random) function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Cache Read (Sequential or Random) function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache Read (Sequential or Random) function. Issuing an additional Cache Read (Sequential or Random) function copies the data most recently read from the array into the page register.

When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a Cache Read Sequential (31h) command after the last page of the block is read. Figure 15 defines the Cache Read behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. During Cache Read operation the only acceptable commands are Read Status, Random Data Output and Reset.

3.14 Cache Program (available only within a block)

Cache Program is used to improve the program throughput by programming data using the cache register(Figure 21). The Cache Program operation can only be used only within one block. The cache register allows new data to be input while the previous data that was transferred to the page buffer is programmed into the memory array. After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence (80h-15h).

The Busy time following the first sequence 80h-15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model. In case of any subsequent sequence 80h-15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCBSYW).

Read Status commands (70h) may be issued to check the status of the different registers, and the pass/ fail status of the Cache Program operations. More in detail: a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data. b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete. c) the Cache Program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in Cache Program operation. The latter can be polled upon I/O<6> status bit changing to "1" . d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation. See “table7. Status Register Coding".

3.15 Multi-plane Cache Program

The device supports Multi-plane Cache Program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache.

The device supports both the traditional and ONFI 1.0 command sets.

The command sequence can be summarized as follows:

a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A18=0 for x8 devices, A17=0 for x16 devices). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.

b) The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

c) Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A18=1 for x8 devices, A17=1 for x16 devices). The data of 2nd page other than those to be programmed do not need to be loaded.

d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence.

The sequence 80h-...-11h...-...81h...-...15h (or the corresponding ONFI 80h-...-11h...-...80h...-...15h) can be iterated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.

The sequence to end Multi-plane Cache Program is 80h-...-11h...-...81h...-...10h (or 80h-...-11h...-...80h...-...10h for the ONFI 1.0 case).Figure 31and Figure 32show the command sequence for the Multi-plane Cache Program operation for the two protocols. Multi-plane Cache Program is available only within two paired blocks belonging to the two planes..

User can check operation status by R/B# pin or read status register commands (70h or 78h)If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes. More in detail:

a) I/O<6> indicates when both cache registers are ready to accept new data.

b) I/O<5> indicates when the cell programming of the current data registers is complete

c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1".

d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".

If the system monitor the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

3.16 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Figure 16 shows the command sequence.

The 5-byte Read ID configuration are supported: The device operating mode (5-byte) is selected through cam setting.

3.16.1 Legacy Read ID

Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 16 shows the operation sequence, while Table 8 to Table 12 explain the byte meaning. Complete read id code table is as follows.

Parameter	Symbol
Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
4th	Page size, Block size, Spare Size, Organization, Serial Acces time
5th	ECC, Multi-plane information

Table 8. "Legacy" Read ID bytes meaning

3.16.2 Read ID Data Table (5 cycle)

Voltage (Vcc)	Bus With	ManuFacture Code	Device Code	3rd	4rh	5th
1.8V	X8	ADh	ACh	90	15	56
1.8V	X16	ADh	BCh	90	55	56

Table 9. Read ID Data Table

3rd Byte of Device Identifier Description

3rd cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleaved Program Between Multiple die	Not Supported Supported		0 1						
Cache Program	Not Supported Supported	0 1							

Table 10. Legacy Read ID 3rd byte description

4th Byte of Device Identifier Description

4th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Block Size (Without Spare Area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Redundant Area Size (byte/512byte)	16						1		
Number of IO	X8 X16		0 1						
Serial Access Time(min)	45ns 25ns Reserved Reserved	0 1 0 1				0 0 1 1			

Table 11. Legacy Read ID 4th byte description

5th Byte of Device Identifier Description

5th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1bit/512Bytes 2bit/512Bytes 4bit/512Bytes 8bit/512Bytes							0 0 1 1	0 1 0 1
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size (W/O redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved		0							

Table 12. Legacy Read ID 5th byte description

3.17 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI" where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 37 shows the operation sequence

3.18 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. Figure 38 defines the Read Parameter Page behavior.

This data structure enables the host processor to automatically recognize the Nand Flash configuration of a device. The whole data structure is repeated at least three times.

The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.

The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

3.19 Parameter Page Data Structure Definition

For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.

Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.

For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

Byte	O/M	Description	
		Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page copy-back 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	X8: 1Ch X16: 1Dh
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports copy-back 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache command 0 1 = supports Page Cache Program command	3Bh, 00h
10-31		Reserved (0)	00h
		Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)	0x53h, 0x4Bh, 0x20h, 48h, 59h, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	X8: 48h, 32h, 37h, 53h, 32h, 47h, 38h, 46h, 32h, 44h, 4Bh, 41h, 2Dh, 42h, 4Dh, 20h, 20h, 20h, 20h, 20h X16: 48h, 32h, 37h, 53h, 32h, 47h, 36h, 46h, 32h, 44h, 4Bh, 41h, 2Dh, 42h, 4Dh, 20h, 20h, 20h, 20h, 20h

Byte	O/M	Description	
		Revision information and features block	
64	M	JEDEC manufacturer ID	ADh
65-66	O	Date code	00h
67-79		Reserved (0)	00h
		Memory organization block	
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	40h, 00h
86-89	M	Number of data bytes per partial page	00h, 00h, 00h, 00h
90-91	M	Number of spare bytes per partial page	00h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	00h, 08h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	28h, 00h
105-106	M	Block endurance	05h, 04h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	05h, 04h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	04h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	04h
115-127		Reserved (0)	00h

	Electrical parameters block		
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	03h, 00h
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	03h, 00h
133-134	M	t_{PROG} Maximum page program time (µs)	BCh, 02h
135-136	M	t_{BERS} Maximum block erase time (µs)	10h, 27h
137-138	M	t_R Maximum page read time (µs)	1Eh, 00h
139-140	M	tCCS Minimum change column setup time (ns)	3Ch, 00h
141-163		Reserved (0)	00h
	Vendor block		
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255	M	Integrity CRC	X8: 1Fh, AAh X16: D0h, 05h
	Redundant Parameter Pages		
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Table 13. Parameter Page Description

Note:
1. O" Stands for Optional, "M" for Mandatory.

4. Signal Descriptions

4.1 Data Protection and Power On/Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.1 V (1.8 V Device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 42. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Figure 40). Its value can be determined by the following guidance.

4.3 Write Protect Handling

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100nsec. Switching WP# low during this time is equivalent to issuing a Reset command (FFh)

The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for tRST (similarly to Figure 23). At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the WP# value. Refer to Table 7 for more information on device status.

Erase and program operations are enabled or disabled by setting WP# to high or low respectively prior to issuing the setup commands (80h or 60h).

The level of WP# shall be set tWW nsec prior to raising the WE# pin for the set up command, as explained in Figure 41~44.

5. Device Parameters

5.1 Valid Blocks

	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	4016		4096	Blocks

Table 14. Valid Blocks Number

Note:
1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment..

5.2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
		Min	
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	℃
	Ambient Operating Temperature (Mobile Operating Temperature)	-30 to 85	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	℃
V_{IO}	Input or Output Voltage	-0.6 to 4.6	V
V_{CC}	Supply Voltage	-0.6 to 4.6	V

Table 15. Absolute Maximum Ratings

Notes:
1. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability

5.3 DC and Operating Characteristics

Parameter		Symbol	Test Conditions	1.7 V ~ 1.95 V			Units
				Min	Typ	Max	
Power on reset current		I_{CC0}	FFh command input after power on	-	-	50 per device	mA
Operating Current	Read	I_{CC1}	t_{RC}= t_{RC}(min), CE#=V_{IL}, I_{OUT}=0 mA	-	10	20	mA
	Program	I_{CC2}	Normal	-	-	20	mA
			Cache	-	-	30	mA
	Erase	I_{CC3}		-	10	20	mA
Stand-by Current (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{CC5}	CE#=V_{CC}-0.2, WP#=0V/V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to $V_{CC(MAX)}$	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to $V_{CC(MAX)}$	-	-	±10	uA
Input High Voltage		V_{IH}	-	Vccx0.8	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xVcc	V
Output High Voltage Level		V_{OH}	I_{OH}=-100 µA	Vcc-0.1	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=100 µA	-	-	0.1	V
Output Low Current (R/B#)		I_{OL} (R/B#)	V_{OL}=0.1V	3	4	-	mA

Table 18. DC and Operation Characteristics

5.4 AC Test Conditions

Parameter	Value
	1.7V ≤ Vcc ≤ 1.95V
Input Pulse Levels	0 V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} / 2
Output Load (2.7V-3.6V)	1 TTL GATE and CL=30pF

Table 19. AC Test Conditions

5.5 Pin Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	-	10	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V	-	10	pF

5.6 Program / Read / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program	t_{PROG}	-	300	700	us
Read Cache busy time	t_{CBSYR}		5	tR	us
Cache Program short busy time	t_{CBSYW}	-	5	tPROG	us
Cache Program busy time (ONFI)	t_{PCBSY}	-	5	tPROG	us
Multi-plane Erase busy time	t_{IEBSY}	-	500	1000	ns
Multi-plane Program busy time (traditional)	t_{DBSY}	-	500	1000	ns
Multi-plane Program busy time (ONFI)	t_{IPBSY}	-	500	1000	ns
Number of partial Program Cycles in the same page	NOP	-	-	4	cycles
Block Erase Time	t_{BERS}	-	3.5	10	ms

Table 20. Program / Erase Characteristics

Notes:
Typical value is measured at Vcc=1.8 V, TA=25℃(1.8V Device). . Not 100% tested.

5.7 AC Timing Characteristics

Parameter	Symbol	3.3V		1.8V		Unit
		Min	Max	Min	Max	
CLE setup time	t_{CLS}	12	-	25	-	ns
CLE Hold time	t_{CLH}	5	-	10	-	ns
CE# setup time	t_{CS}	20	-	35	-	ns
CE# hold time	t_{CH}	5	-	10	-	ns
WE# pulse width	t_{WP}	12	-	25	-	ns
ALE setup time	t_{ALS}	12	-	25	-	ns
ALE hold time	t_{ALH}	5	-	10	-	ns
Data setup time	t_{DS}	12	-	20	-	ns
Data hold time	t_{DH}	5	-	10	-	ns
Write cycle time	t_{WC}	25	-	45	-	ns
WE# high hold time	t_{WH}	10	-	15	-	ns
Address to data loading time	t_{ADL}	70	-	100	-	ns
Data transfer from cell to register	t_{R}	-	30	-	30	us
ALE to RE# delay	t_{AR}	10	-	10	-	ns
CLE to RE# delay	t_{CLR}	10	-	10	-	ns
Ready to RE# low	t_{RR}	20	-	20	-	ns
RE# pulse width	t_{RP}	12	-	25	-	ns
WE# high to busy	t_{WB}	-	100	-	100	ns
Read cycle time	t_{RC}	25	-	45	-	ns
RE# access time	t_{REA}	-	20	-	30	ns
RE# high to output high Z	t_{RHZ}	-	100	-	100	ns
CE# high to output high Z	t_{CHZ}		30		50	ns
CE# high to ALE or CLE Don't care	t_{CSD}	10	-	10	-	ns
RE# high to output hold	t_{RHOH}	15	-	15	-	ns
RE# low to output hold	t_{RLOH}	5	-	-	-	ns
RE# or CE# high to output hold	t_{COH}	15	-	15	-	ns
RE# high hold time	t_{REH}	10	-	15	-	ns
Output Hi-Z to RE# Low	t_{IR}	0	-	0	-	ns
RE# high to WE# low	t_{RHW}	100	-	100	-	ns
WE# high to RE# low	t_{WHR}	60	-	60	-	ns
CE# low to RE# low	t_{CR}	10	-	10		ns
Device resetting time (Read/Program/Erase)	t_{RST}	-	5/10/500	-	5/10/500	us
Write protect time	t_{WW}	100	-	100	-	ns

Table 21. AC Timing Characteristics

6. Timing Diagrams

6.1 Command Latch Cycle Timing

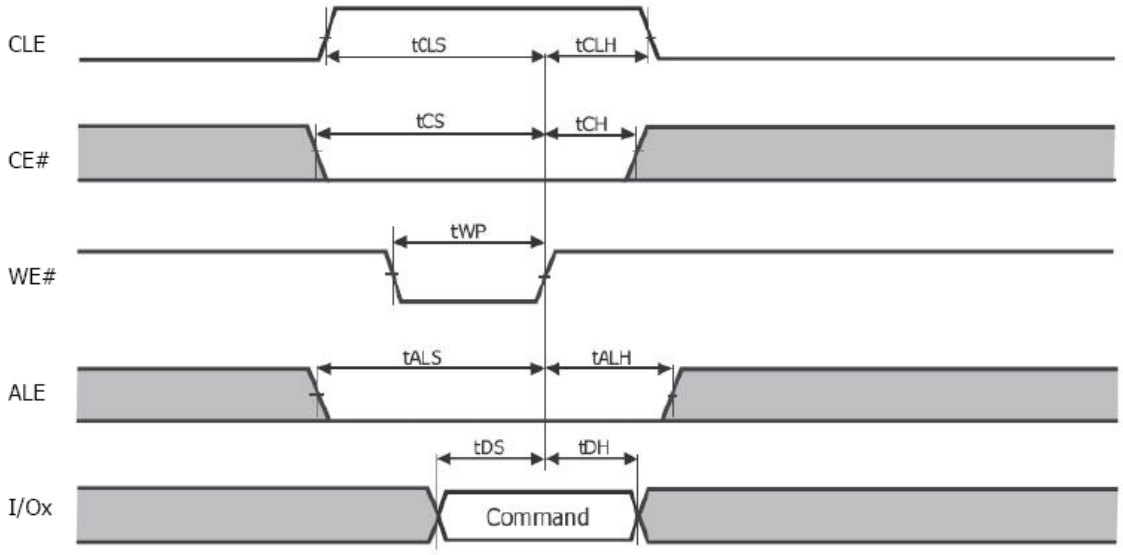


Figure 6. Command Latch Timings

6.2 Address Latch Cycle

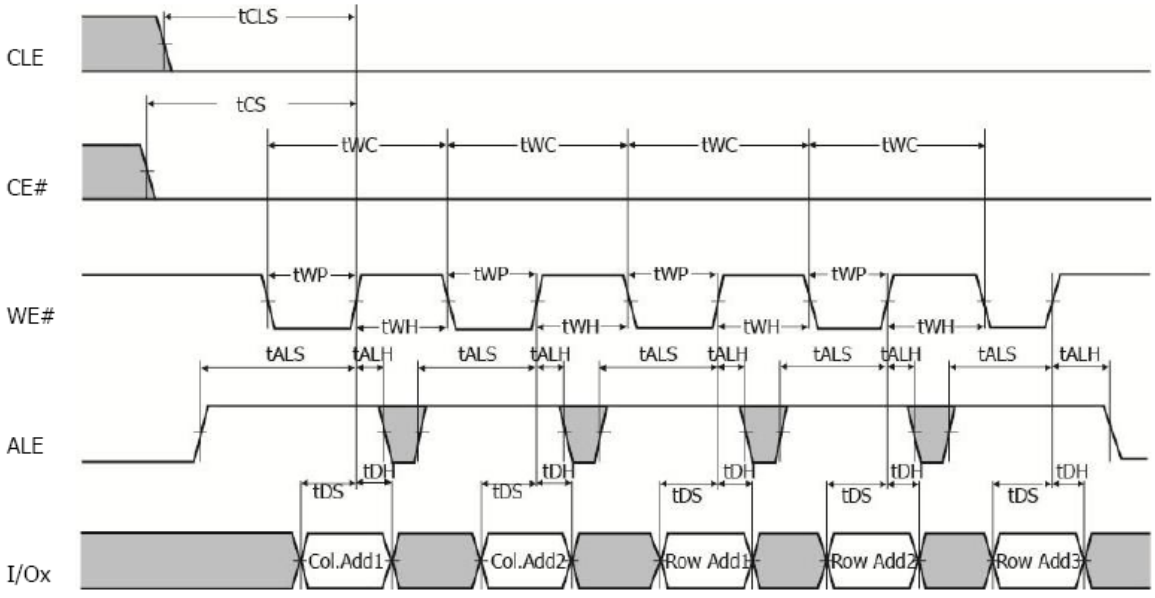


Figure 7. Address Latch Timings

6.3 Data Input Cycle Timing

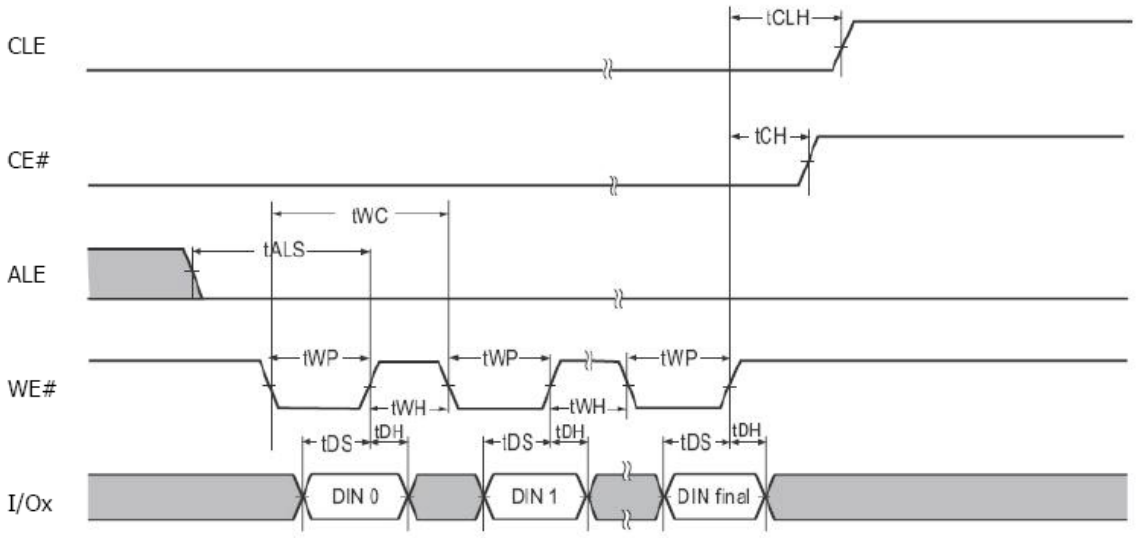


Figure 8. Data Input Cycle Timings

Notes:
Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

6.4 Data Output Cycle Timing (CLE=L, WE#=H, ALE=L, WP#=H)

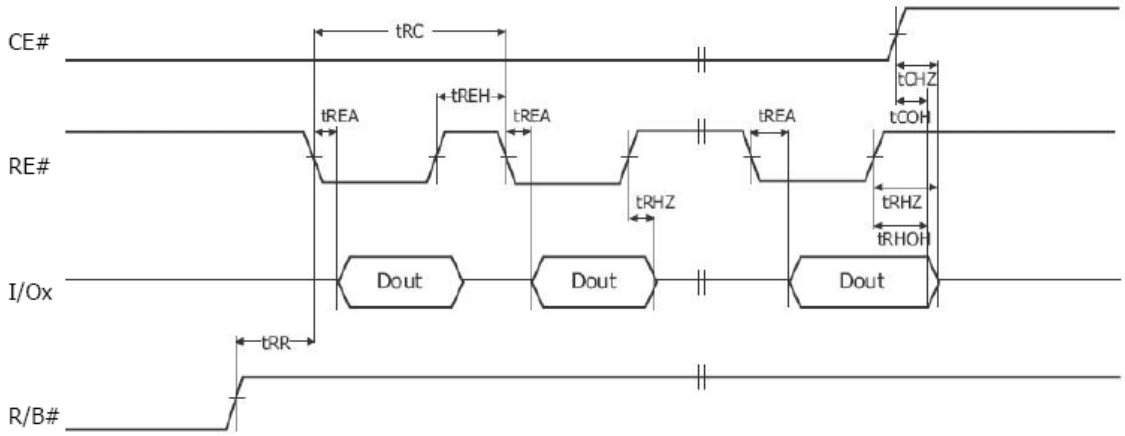


Figure 9. Data Output Cycle Timings

Notes:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRHOHis valid when frequency is lower than 33 MHz.

6.5 Data Output Cycle Timing (EDO Type, CLE=L, WE#=H, ALE=L)

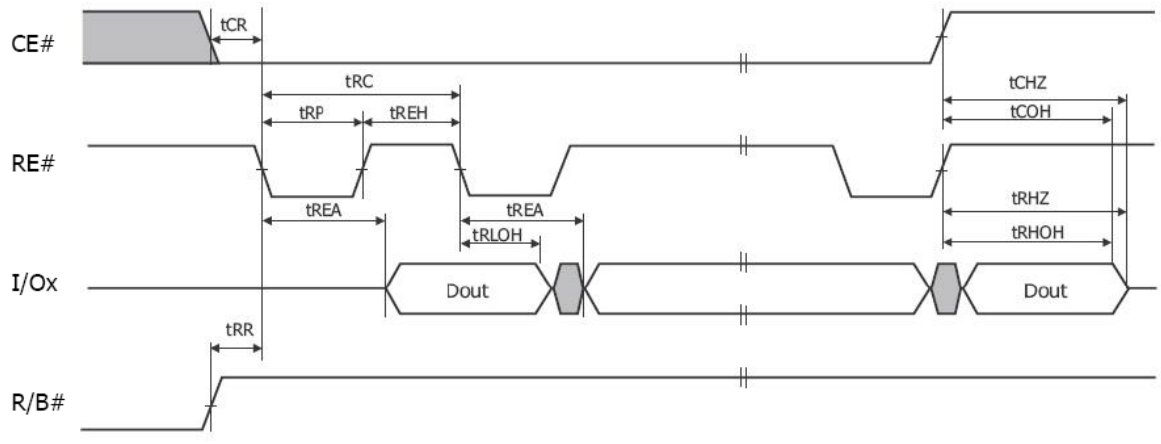


Figure 10. Data Output Cycle Timings (EDO)

Notes:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRLOHis valid when frequency is higher than 33 MHz.tRHOHstarts to be valid when frequency is lower than 33 MHz.

6.6 Read Status Cycle Timing

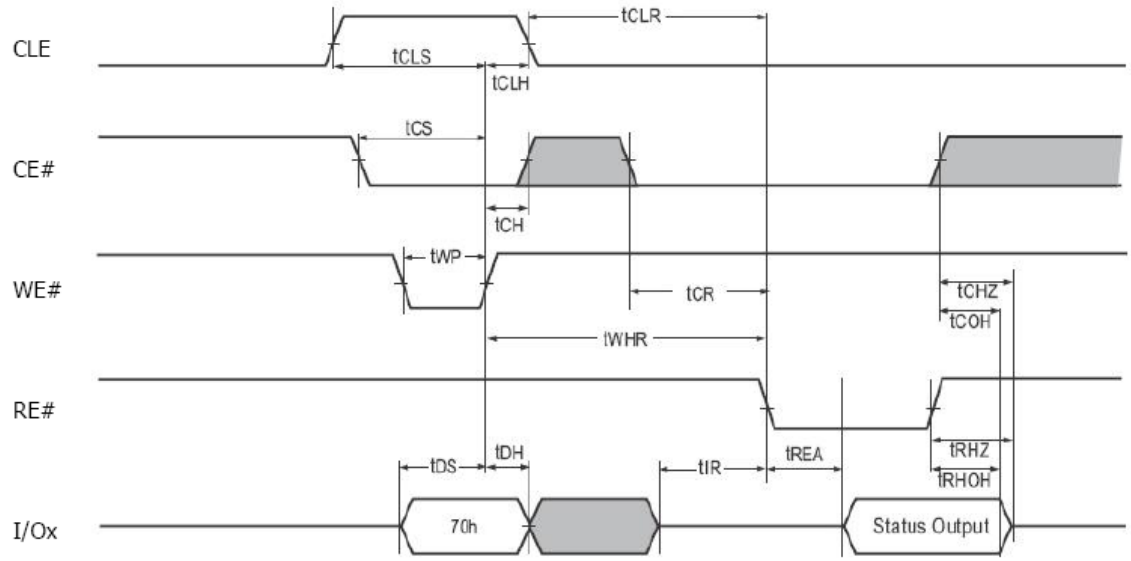


Figure 11A. Read Status Timings

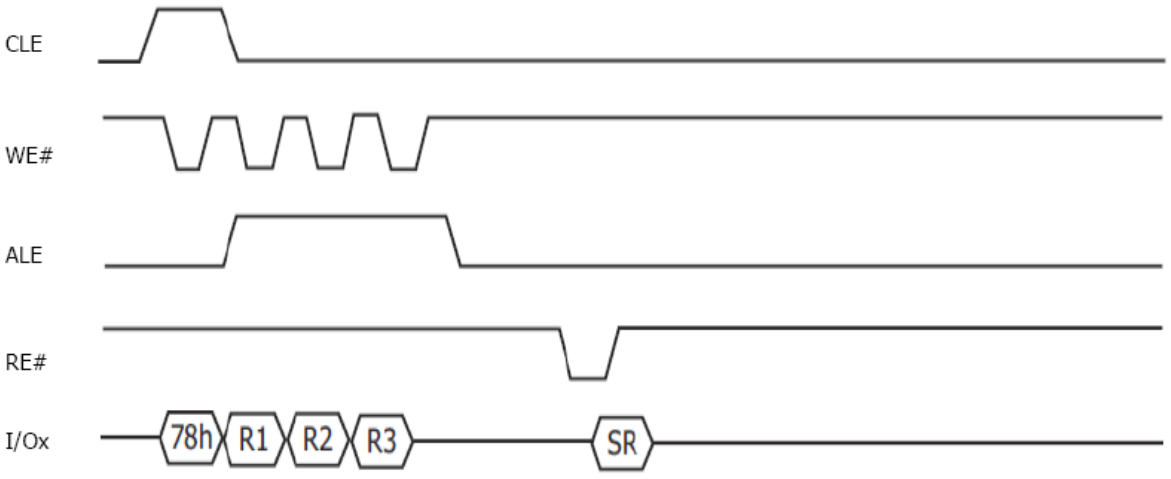


Figure 11B. Read Status Enhanced Cycle

6.7 Page Read Operation Timing (Intercepted by CE#)

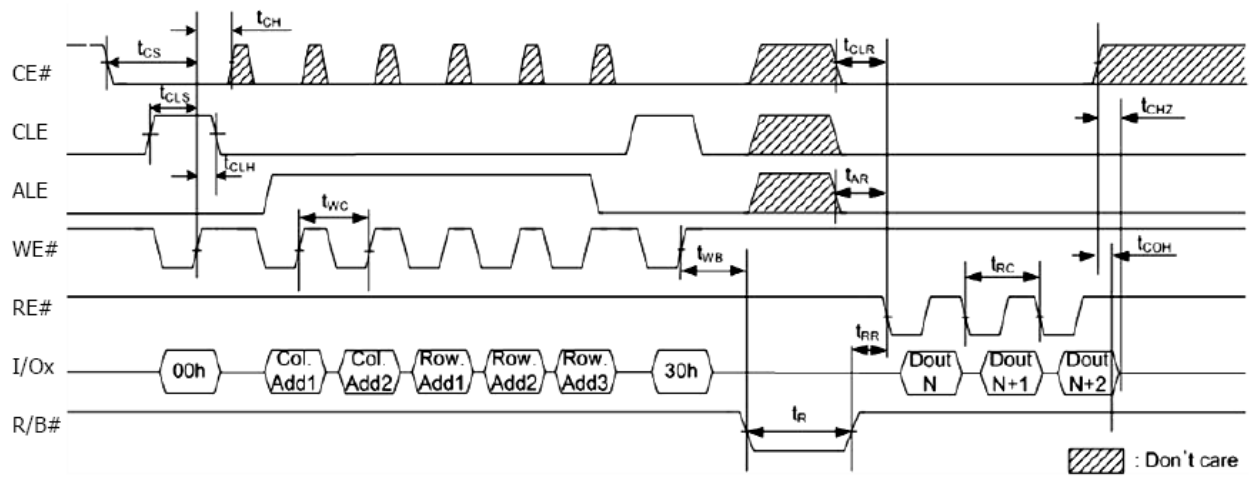


Figure 12. Page Read Operation Timings (Intercepted by CE#)

6.8 Page Read Operation Timing with CE don't care

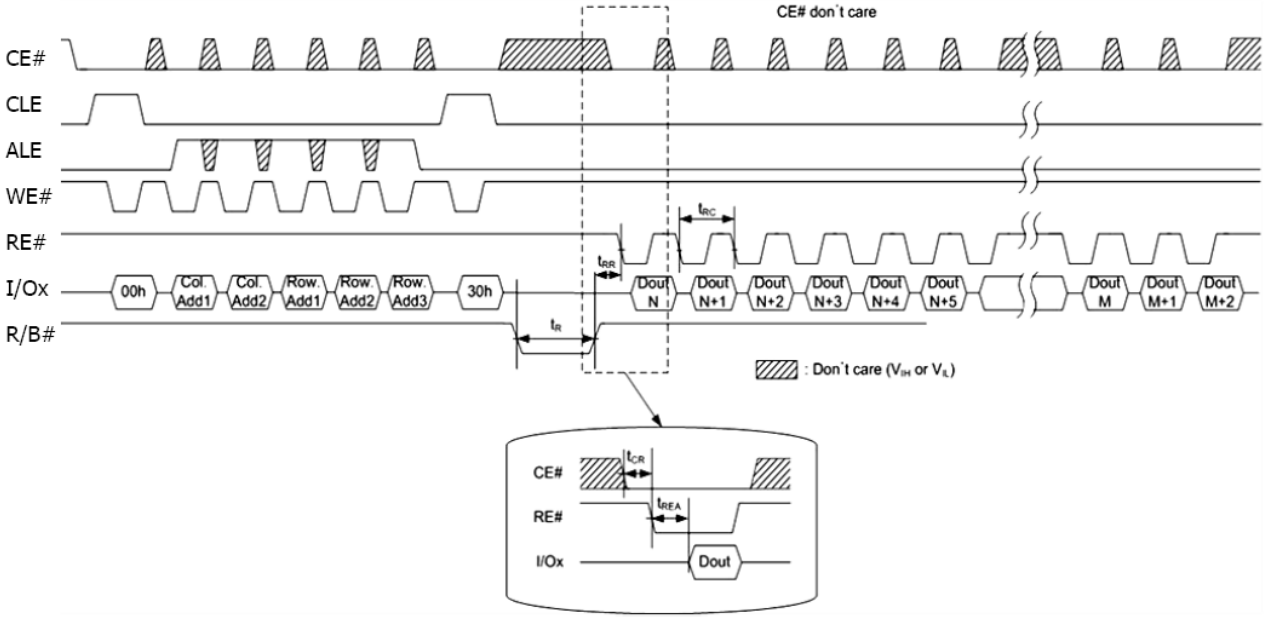


Figure 13. Page Read Operation Timings with CE# don't care

6.9 Random Data Output Timings

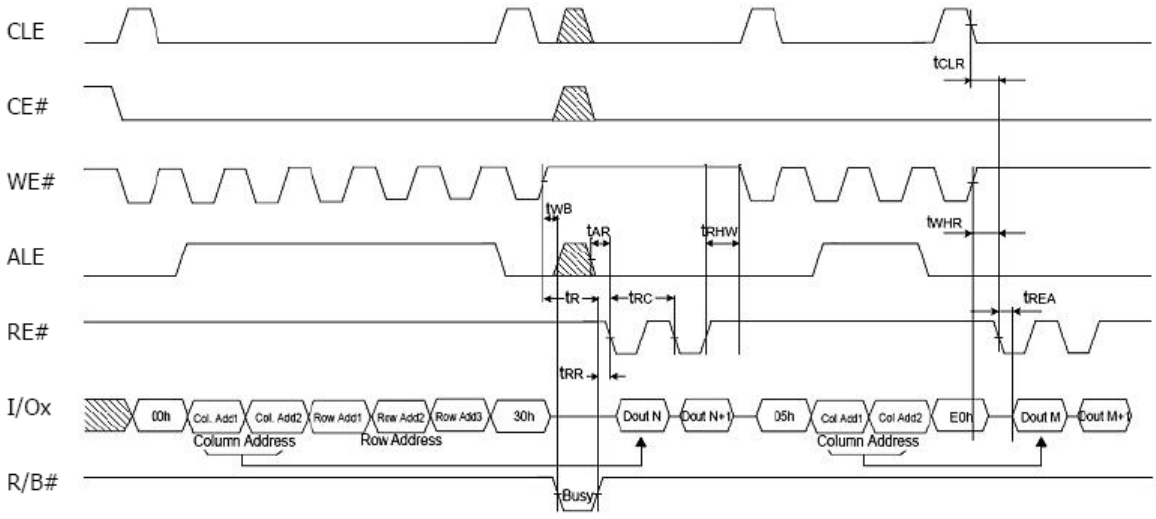


Figure 14. Random Data Output Timings

6.10 Cache Read Operation Timing

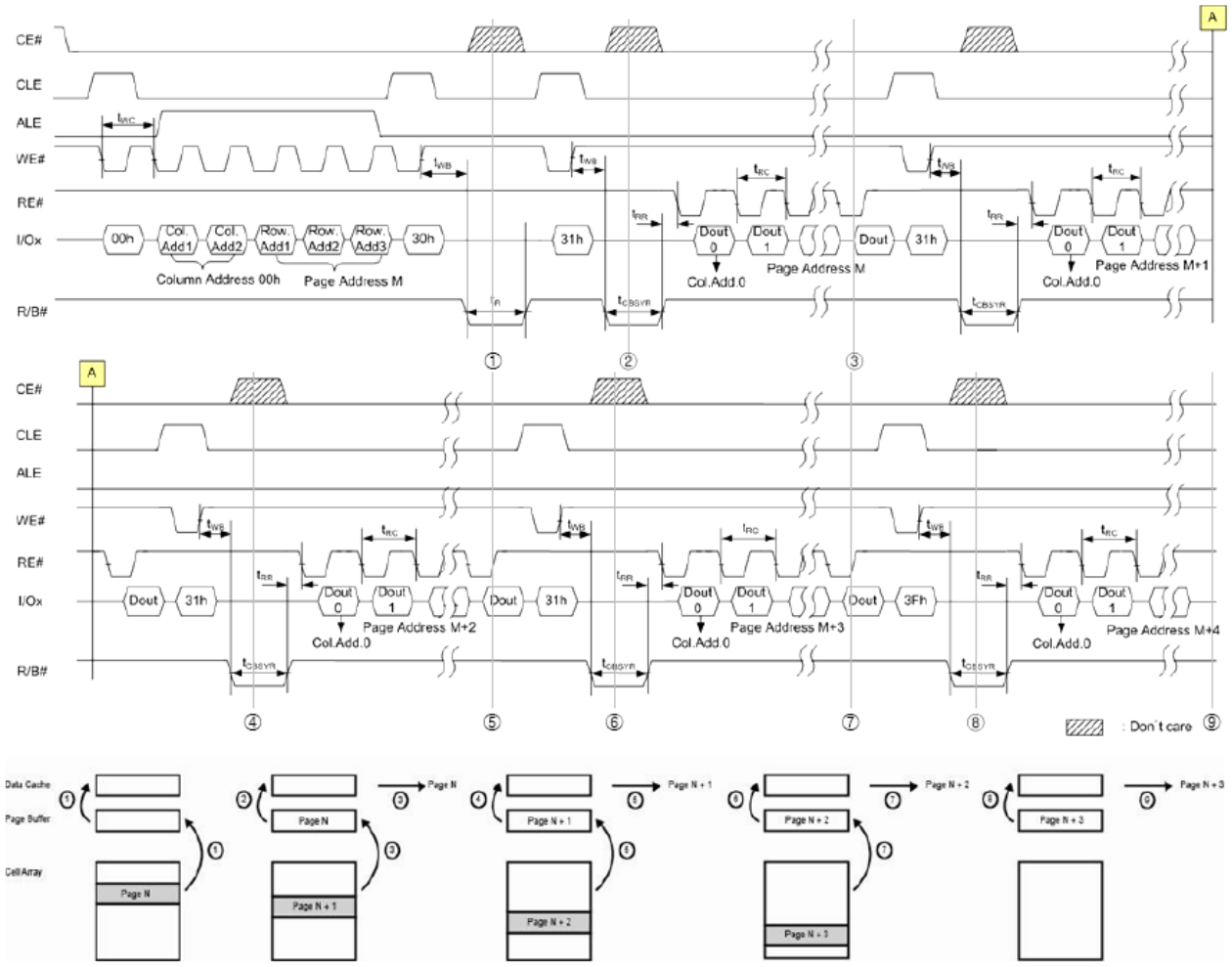


Figure 15. Cache Read Operation Timings

6.11 Read ID Operation Timing

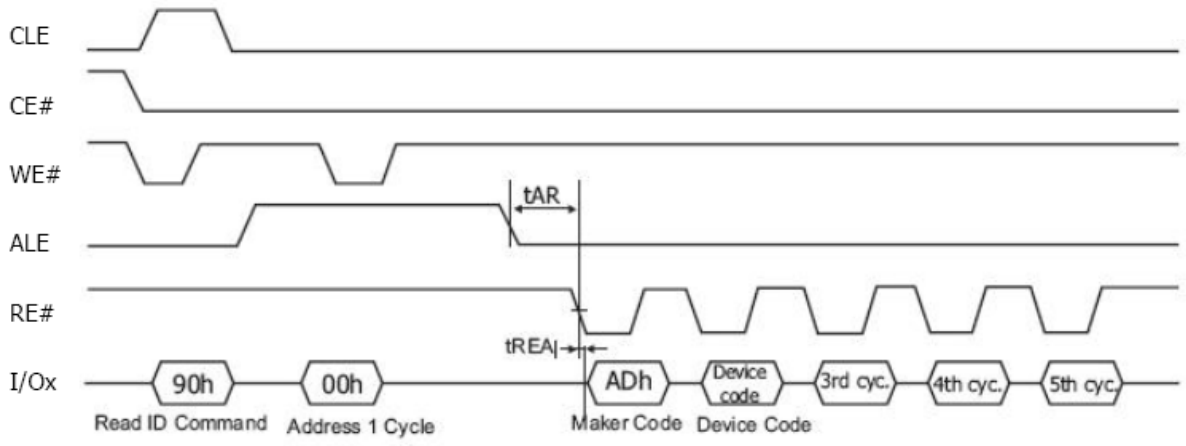


Figure 16. Read ID Operation Timings

6.12 Page Program Operation Timing

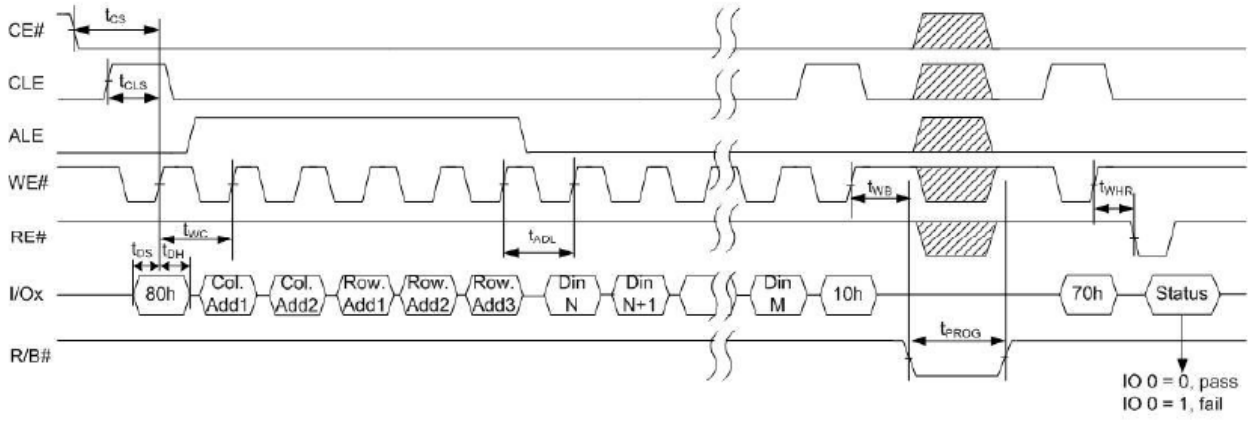


Figure 17. Page Program Operation Timings : Don't care

Notes:
tADLis the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

6.13 Page Program Operation Timing with CE# Don't Care

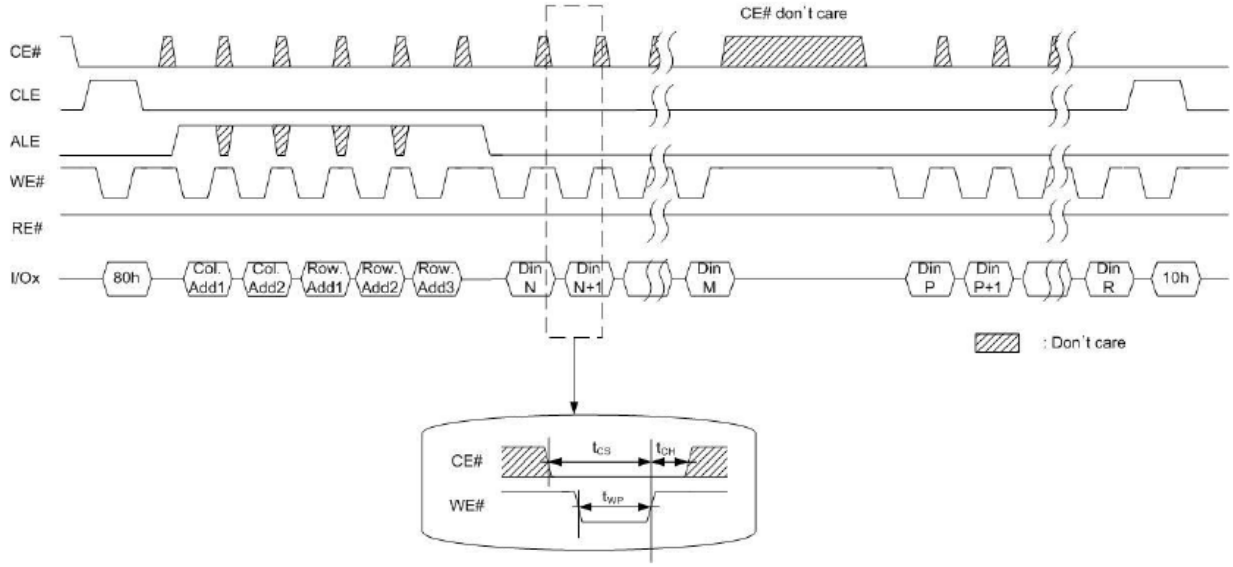


Figure 18. Page Program Operation Timings with CE# don't care

Notes:
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

6.14 Random Data Input Timing

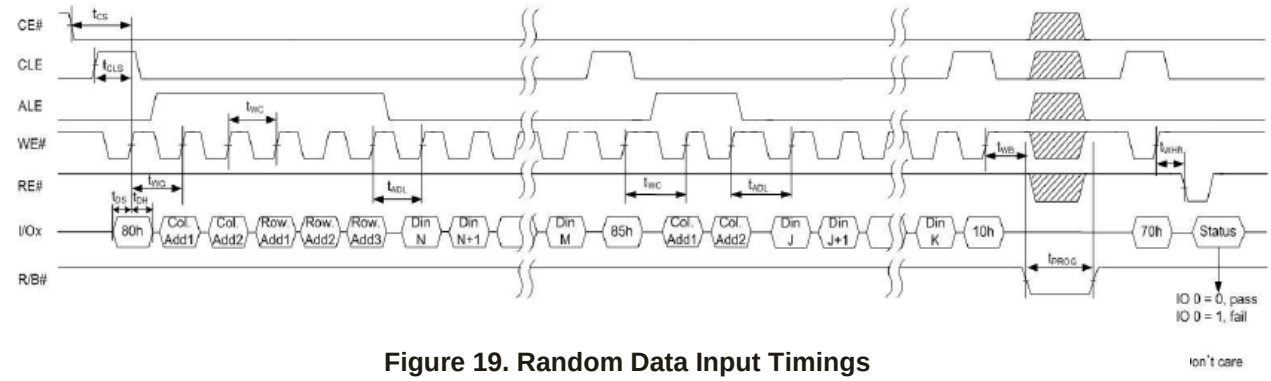


Figure 19. Random Data Input Timings

Notes:
1. tADLis the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
2. Random data input can be performed in a page.

6.15 Copy Back Program Operation with Random Data Input

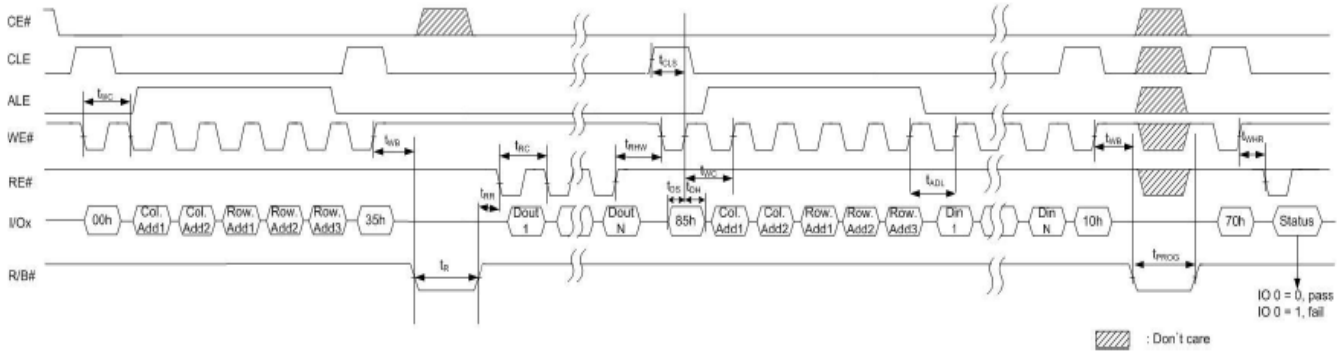


Figure 20. Copy Back Program Operation Timing with Random Data Input

Notes:

1. Copy-Back Program operation is allowed only within the same memory plane.
2. On the same plane, It"s prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. tADLis the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

6.16 Cache Program Operation Timing

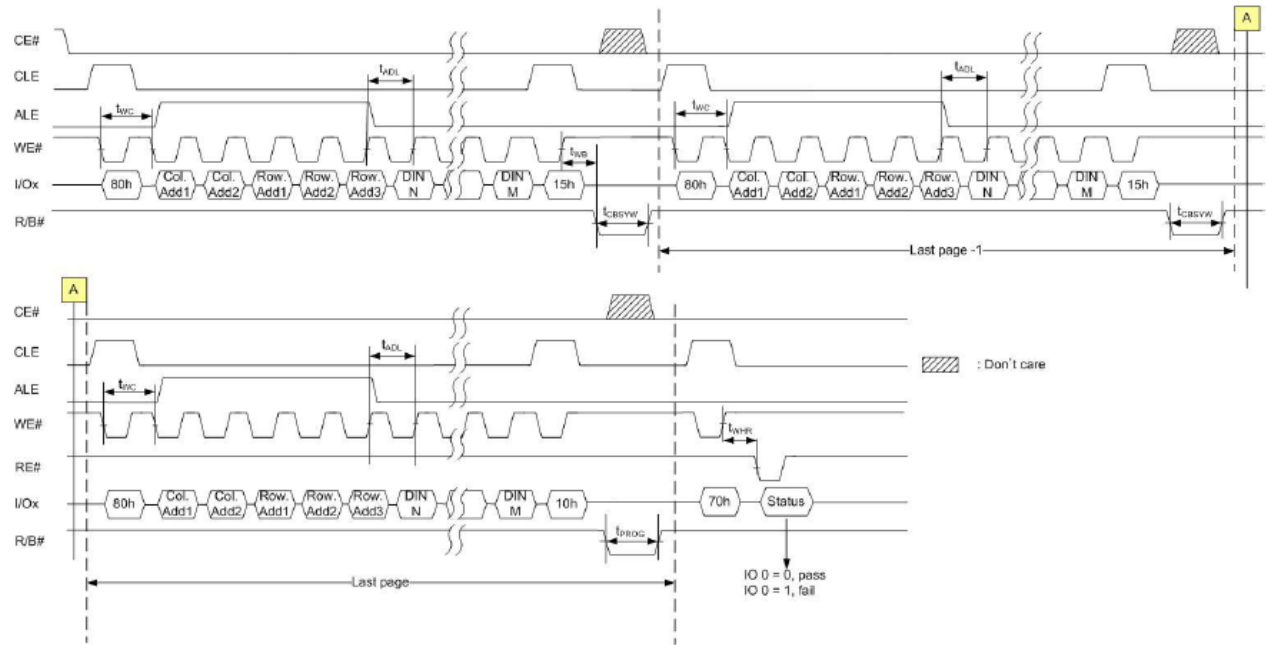


Figure 21. Cache Program Operation Timings

Notes:

tPROG= Program time for the last page + Program time for the (last -1)th page -(command input cycle time + address input cycle time + Last page data loading time)

6.17 Block Erase Operation Timing

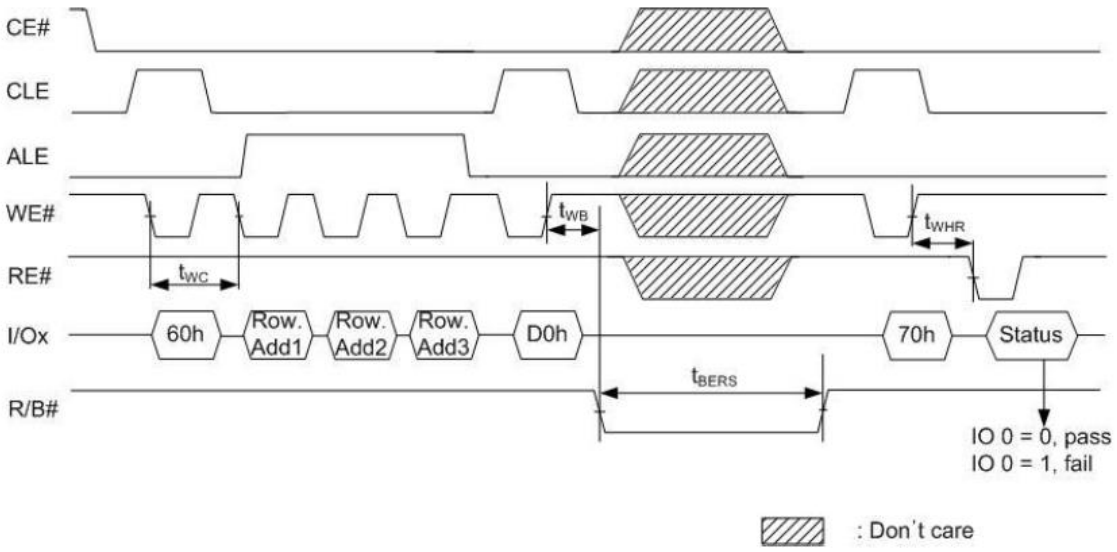


Figure 22. Block Erase Operation Timings

6.18 Reset Timing

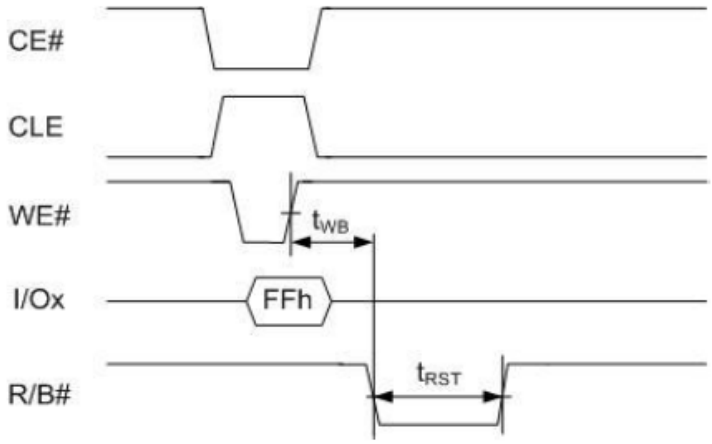


Figure 23. Reset Timings

6.19 Multi-plane Program

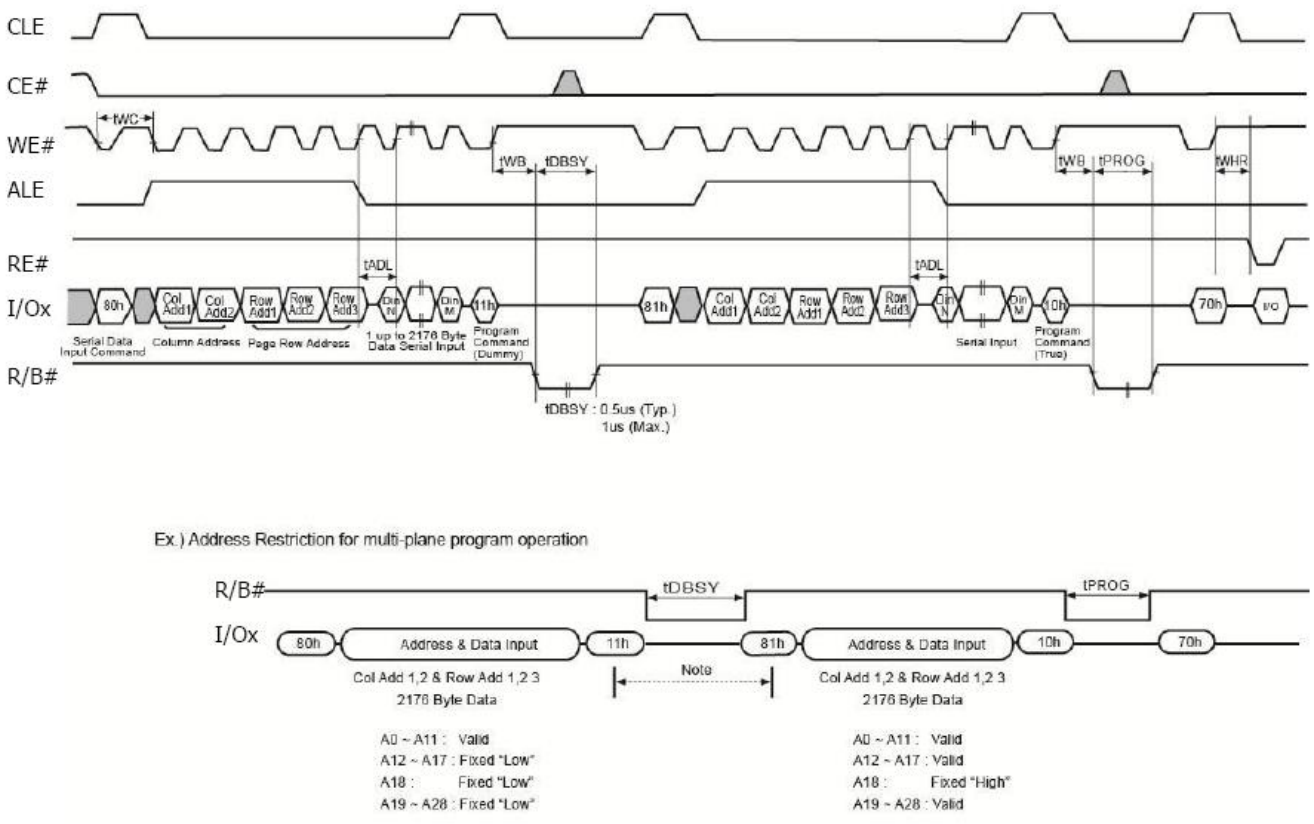


Figure 24. Multi-plane Page Program (traditional protocol)

Notes:
1. The figure refers to x8 case. Please refer to Section 1.4 for address remapping rules for the x16 case
2. Any command between 11h and 81h is prohibited except 70h, 78h and FFh

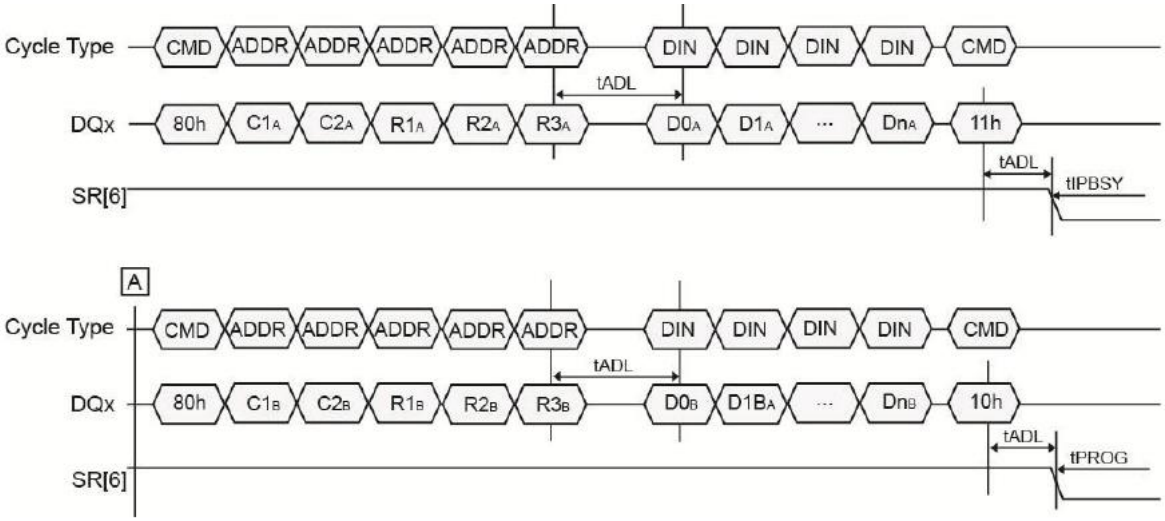
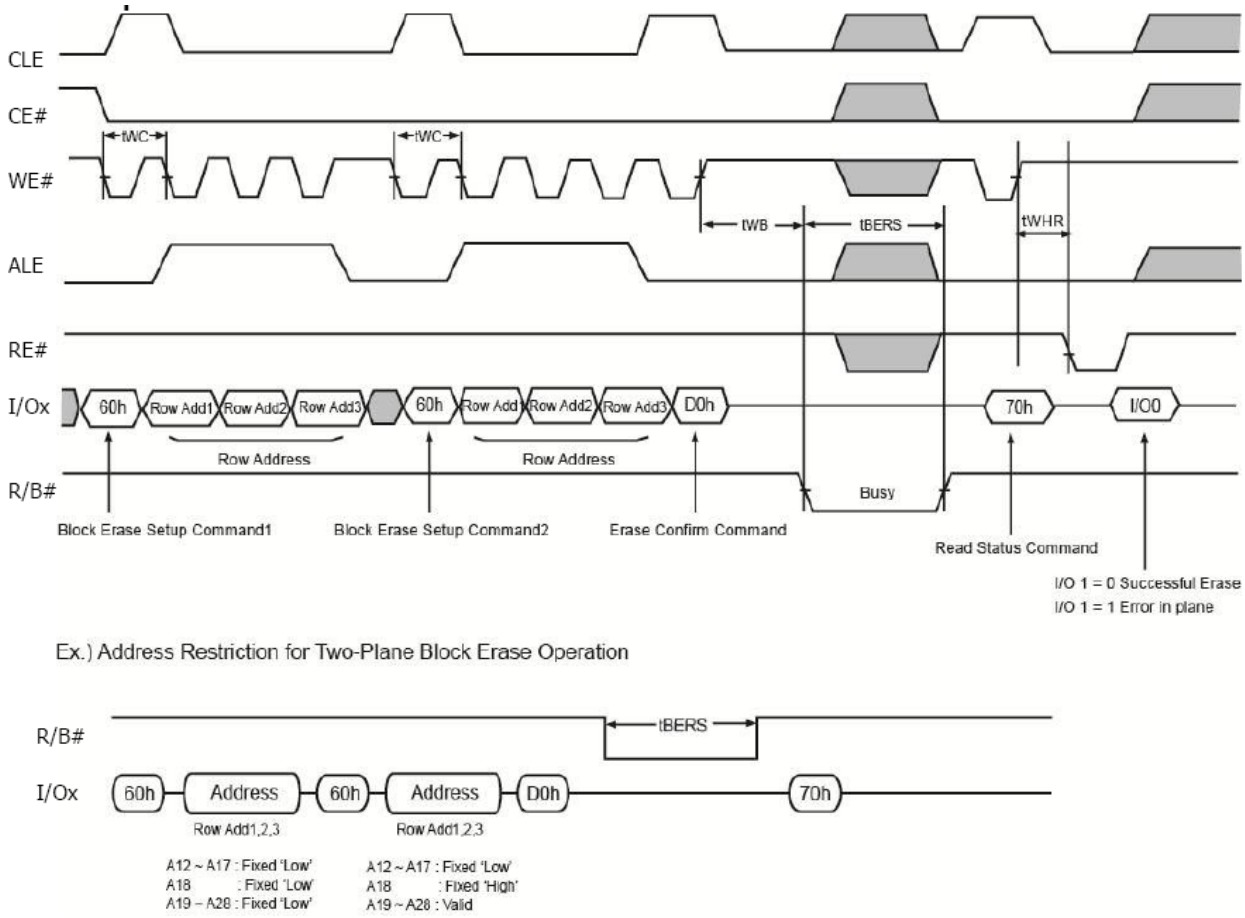


Figure 25. Multi-plane Page Program (ONFI 1.0 protocol)

Notes:
C1A-C2A Column address for page A. C1A is the least significant byte.
R1A-R3A Row address for page A. R1A is the least significant byte.
D0A-DnA Data to program for page A.
C1B-C2B Column address for page B. C1B is the least significant byte.
R1B-R3B Row address for page B. R1B is the least significant byte.
D0B-DnB Data to program for page B.
Same restrictions on address of pages A and B, and allowed commands as Figure 24 apply

6.20 Multi-plane Block Erase



Ex.) Address Restriction for Two-Plane Block Erase Operation

Figure 26. Multi-plane Block Erase (traditional protocol)

Notes:
The figure refers to x8 case. Please refer to Section 1.7 for address remapping rules for the x16 case

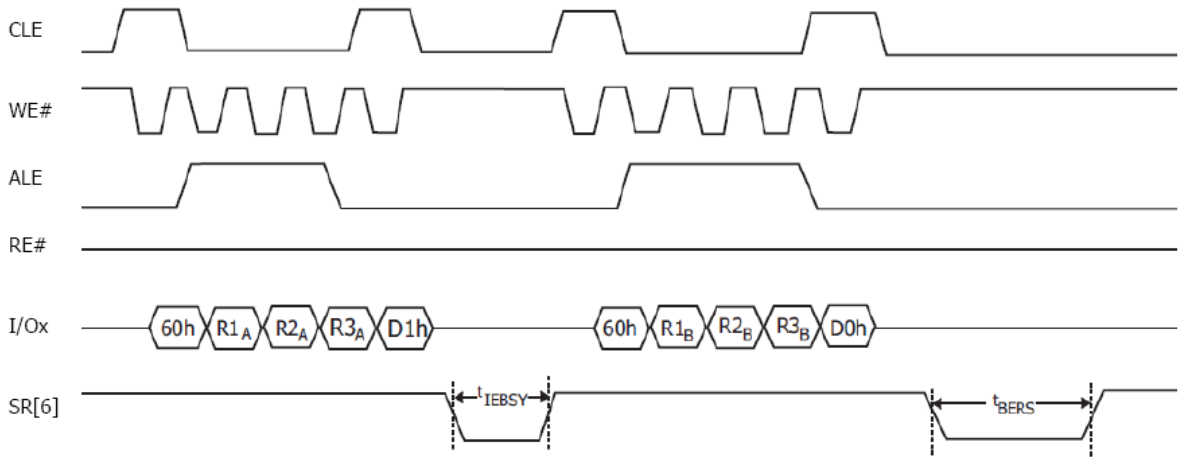


Figure 27. Multi-plane Block Erase (ONFI 1.0 protocol)

Notes:
R1A-R3A Row address for block on plane 0. R1A is the least significant byte.
R1B-R3B Row address for block on plane 1. R1B is the least significant byte.
Same restrictions on address of blocks on plane 0(A) and 1(B) and allowed commands as Figure 30 apply

6.21 Multi-plane Copy Back Program

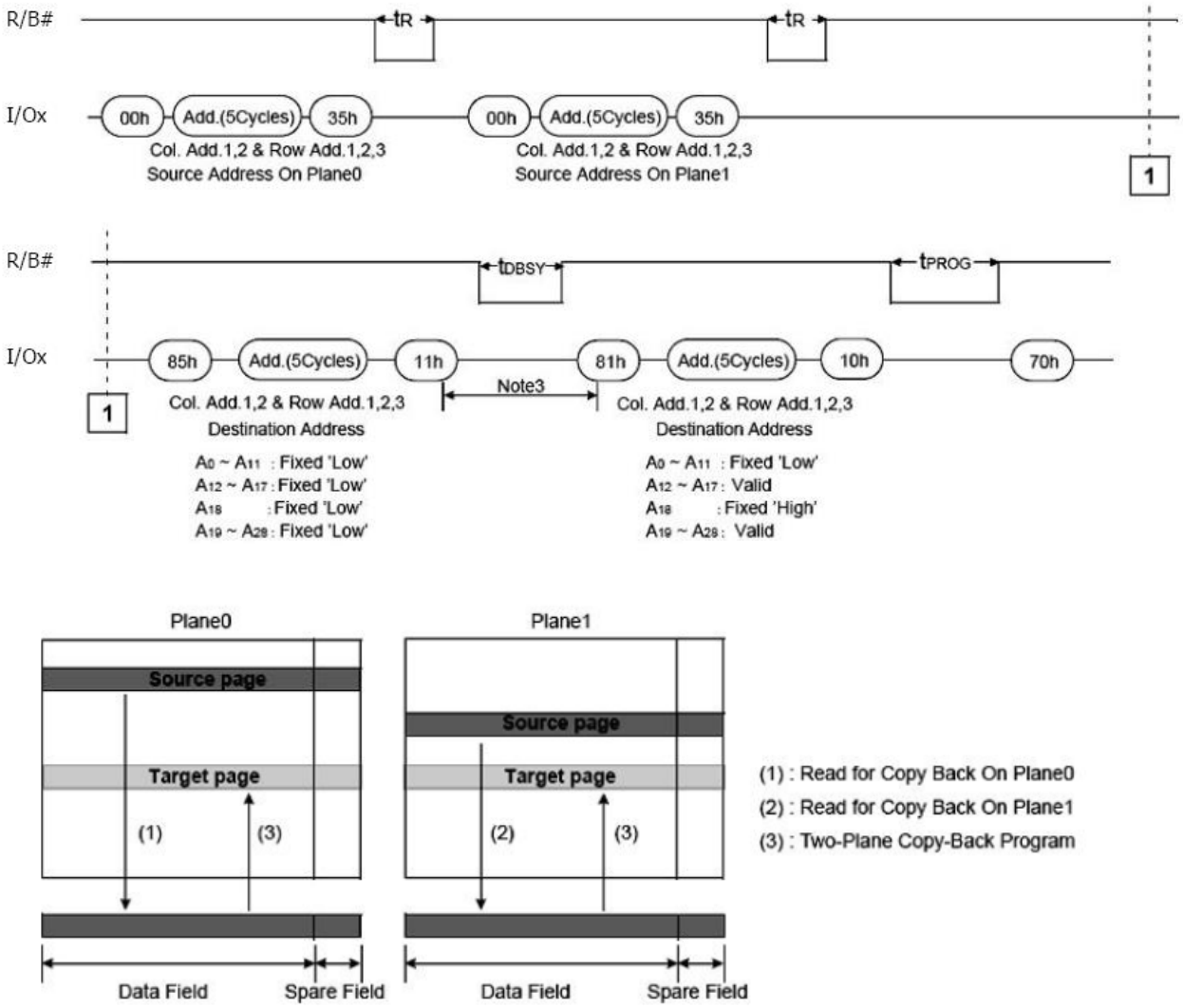


Figure 28. Multi-plane Copy Back Program (traditional protocol)

Notes:

1. Copy-back program operation is allowed only within the same memory plane
2. On the same plane it is prohibited to operate copy-back program from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. Any command between 11h and 81 h is prohibited except 70h and FFh.
4. The figure refers to x8 case. Please refer to Section 1.7 for address remapping rules for the x16 case.

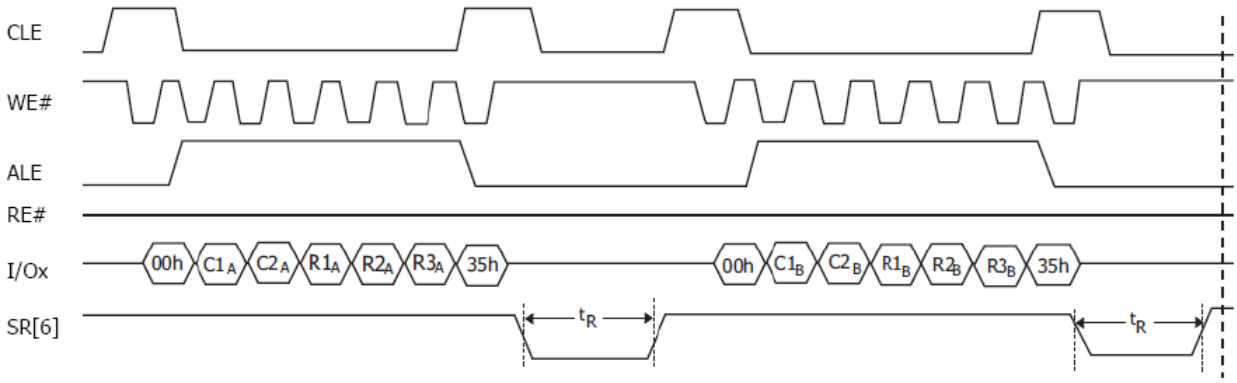


Figure 29. Multi-plane Copy Back Read (ONFI 1.0 protocol)

Notes:
C1A-C2A Column address for page A. C1A is the least significant byte.
R1A-R3A Row address for page A. R1A is the least significant byte.
C1B-C2B Column address for page B. C1B is the least significant byte.
R1B-R3B Row address for page B. R1B is the least significant byte.

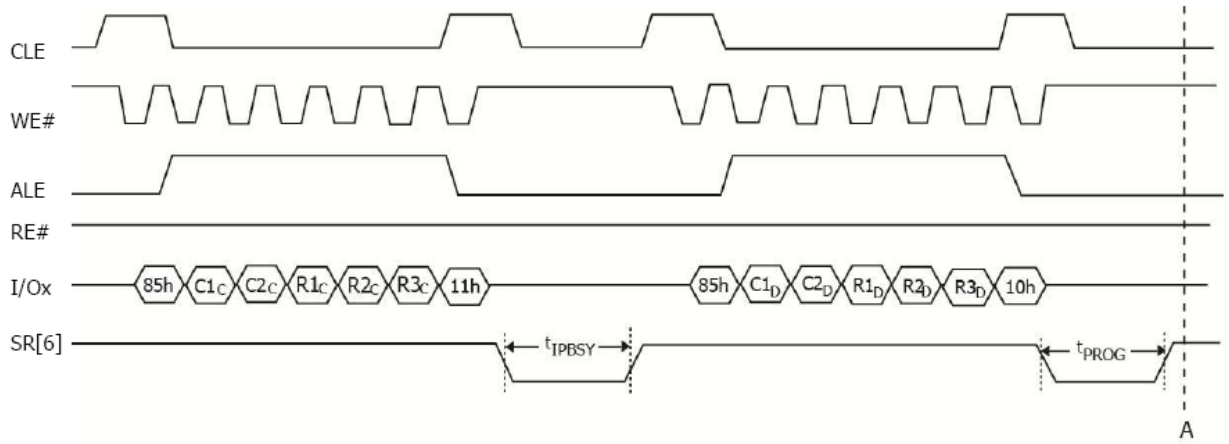


Figure 30. Multi-plane Copy Back Program (ONFI 1.0 protocol)

Notes:
C1C-C2C Column address for page C. C1A is the least significant byte.
R1C-R3C Row address for page C. R1A is the least significant byte.
D0C-DnC Data to program for page C.
C1D-C2D Column address for page D. C1B is the least significant byte.
R1D-R3D Row address for page D. R1B is the least significant byte.
D0D-DnD Data to program for page D.
Same restrictions on address of pages C and D, and allowed commands as Figure 28 apply

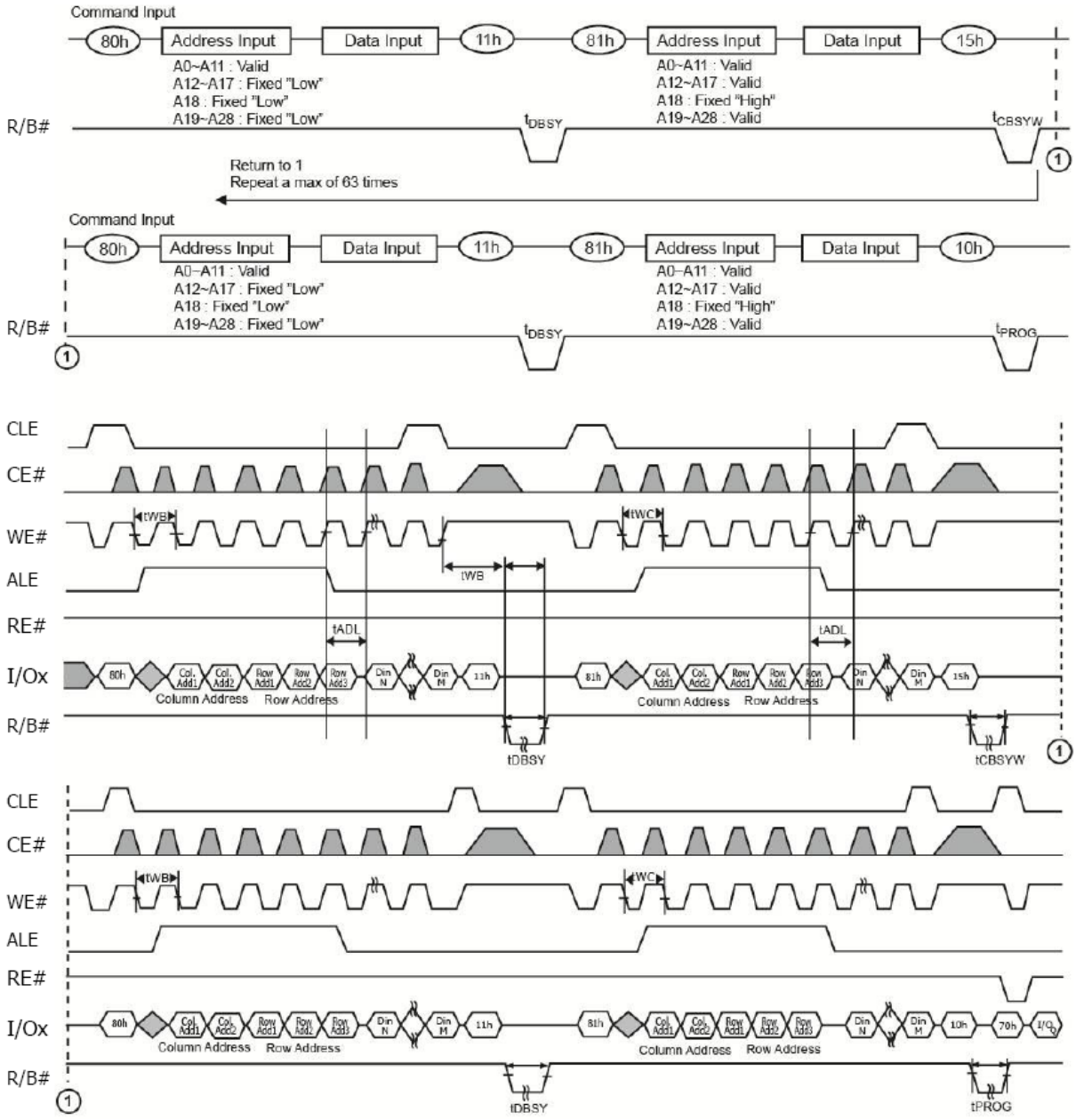


Figure 31. Multi-plane Cache Program (traditional protocol)

Notes:

1. The figure refers to x8 case. Please refer to Section 1.7 for address remapping rules for the x16 case.
2. Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

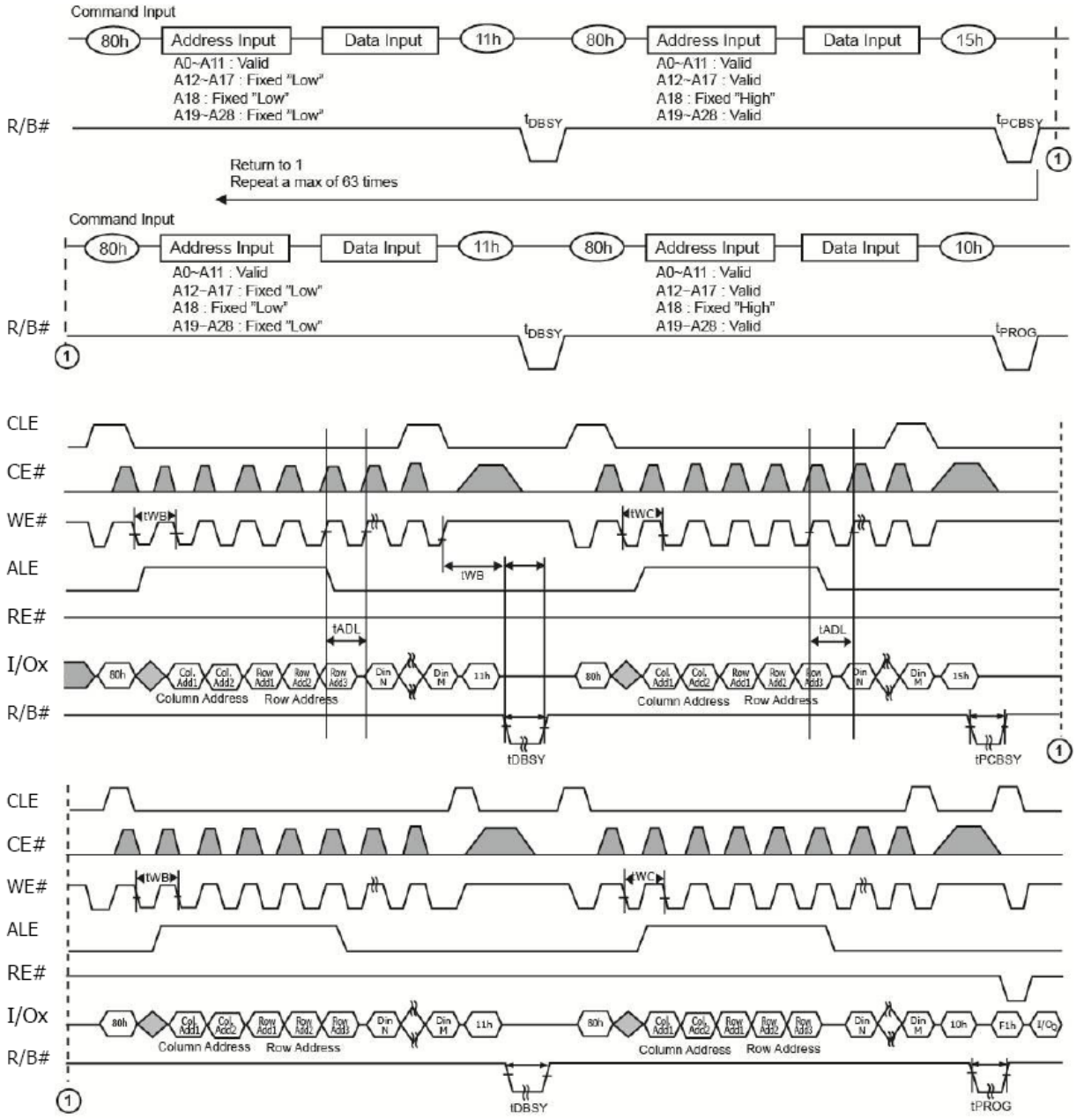


Figure 32. Multi-plane Cache Program (ONFI 1.0 protocol)

Notes:

1. The figure refers to x8 case. Please refer to Section 1.7 for address remapping rules for the x16 case.
2. Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

6.22 Page Reprogram

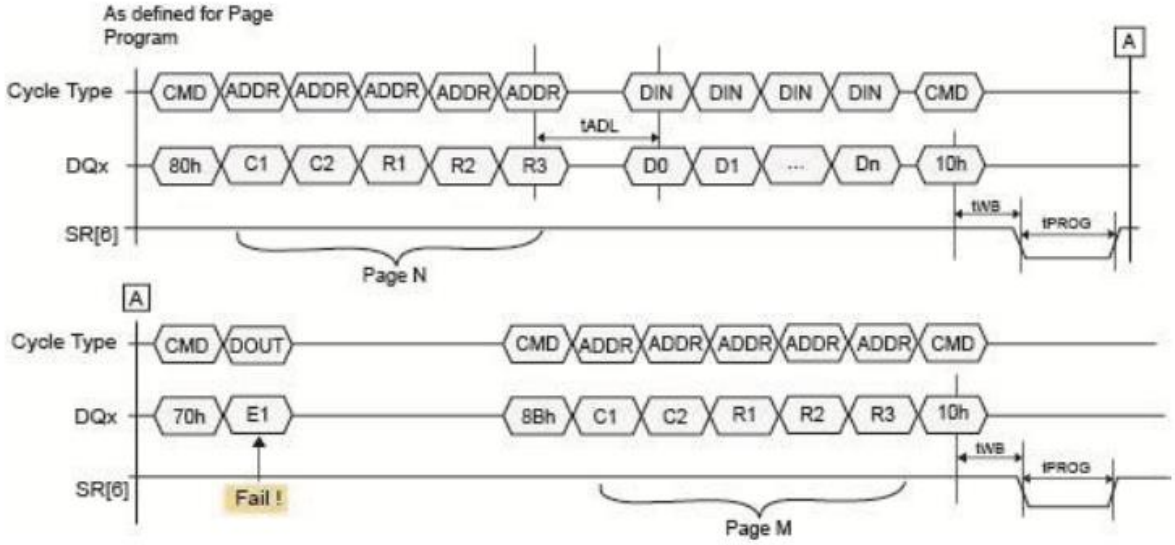


Figure 33. Page Reprogram

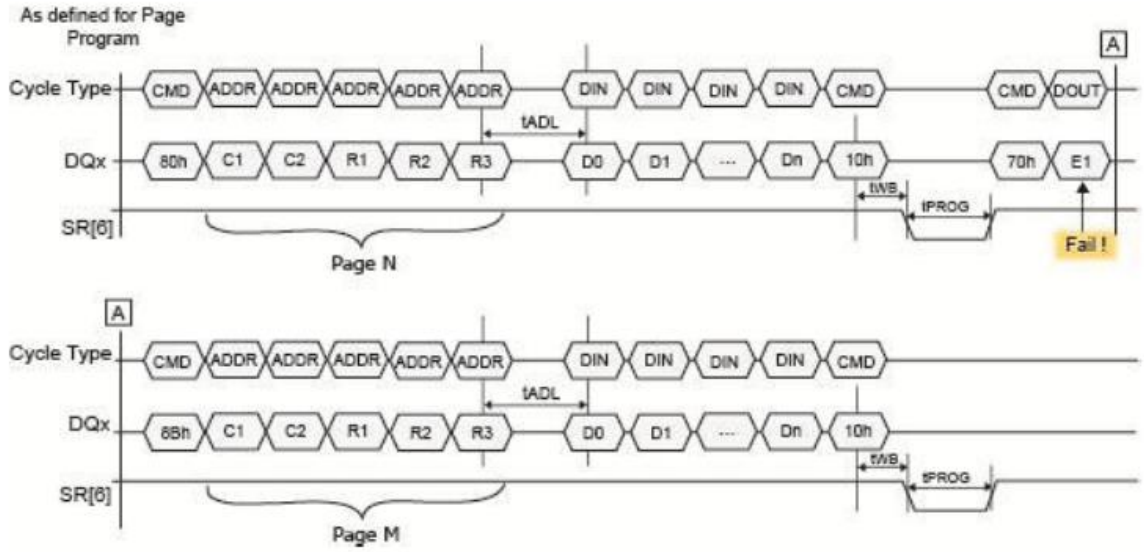


Figure 34. Page Reprogram with data manipulation

6.23 Multi-plane Page Reprogram

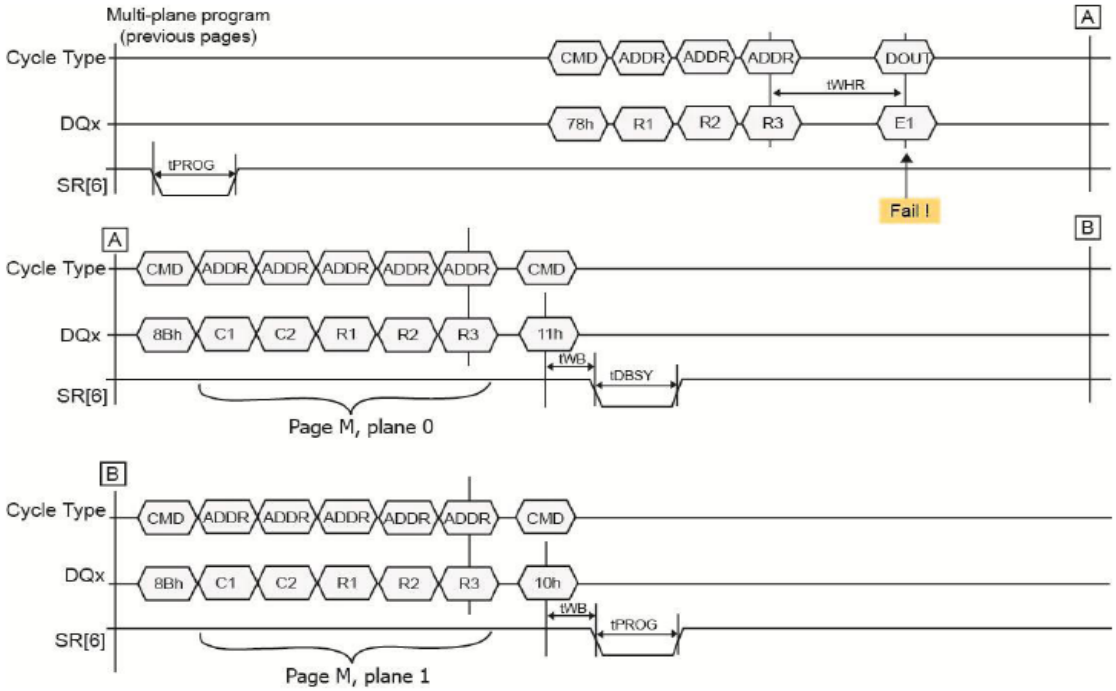


Figure 35. Multi-plane Page Reprogram

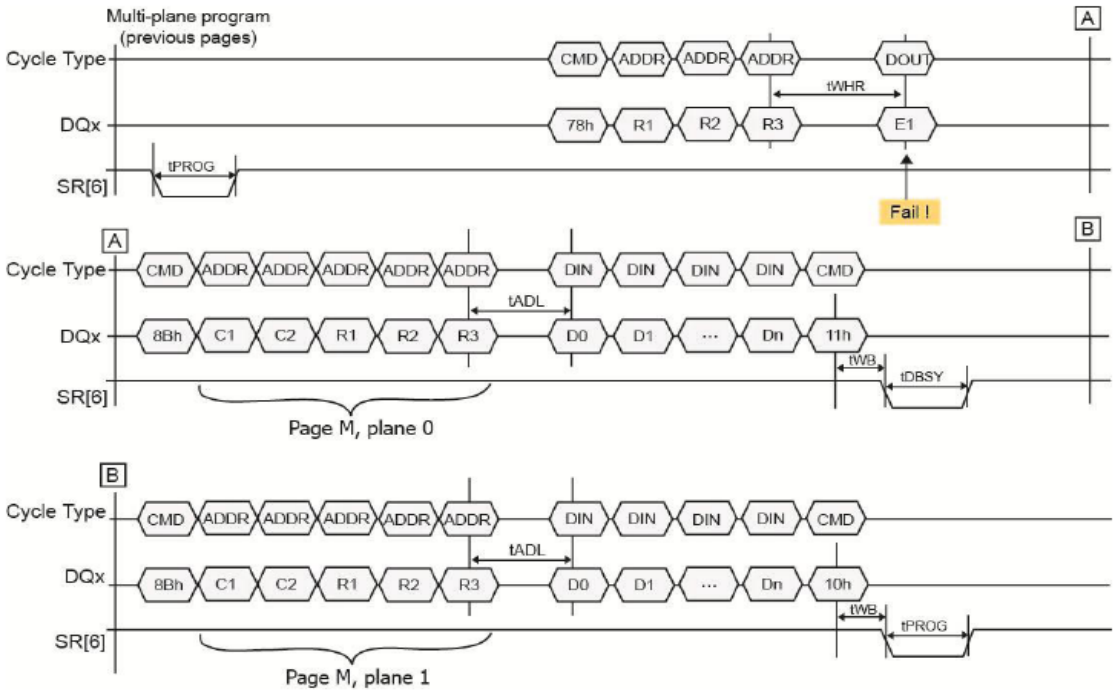


Figure 36. Multi-plane Page Reprogram with data manipulation

6.24 Read ONFI Signature

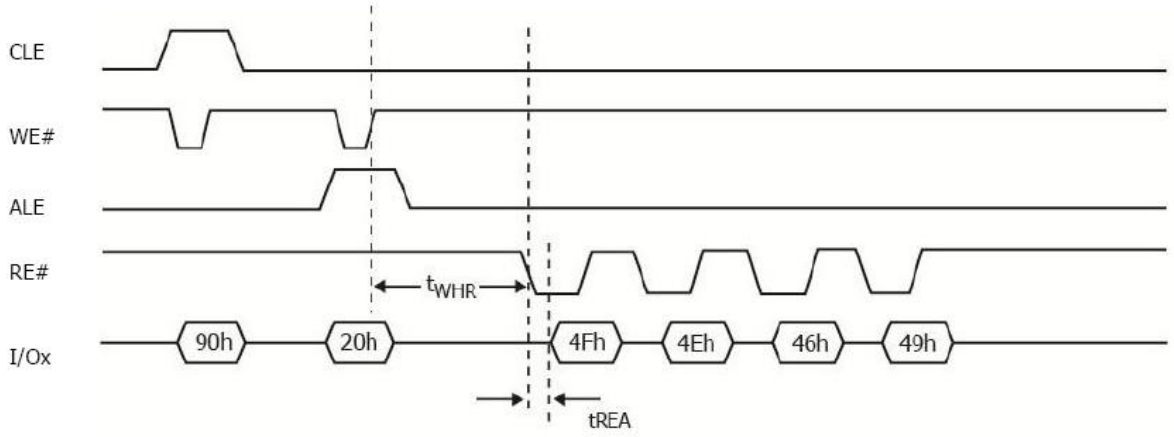


Figure 37. ONFI signature timing

6.25 Read Parameter Page

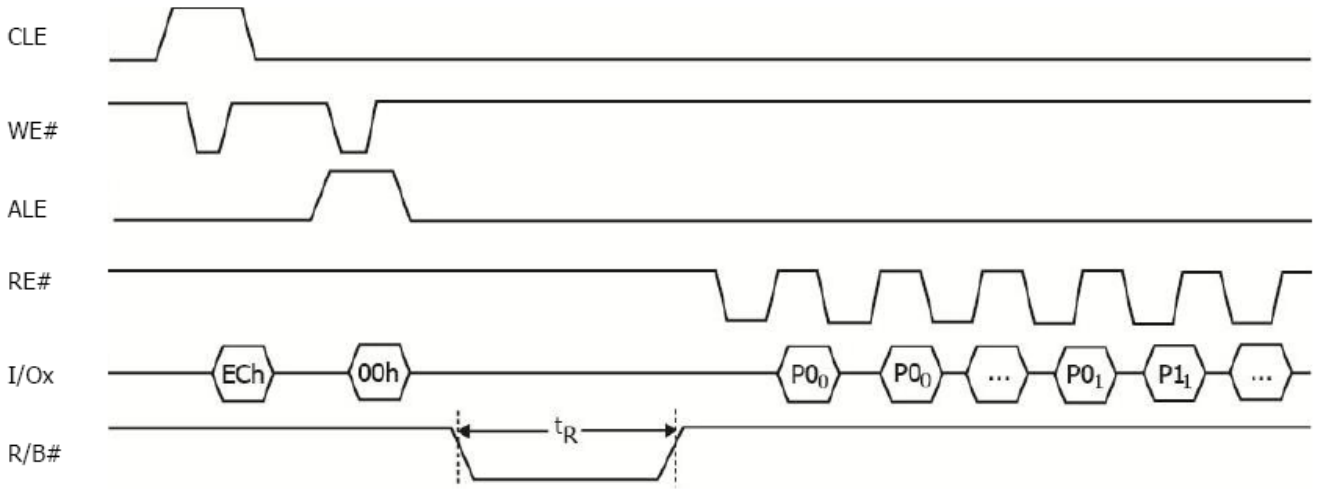


Figure 38. Read Parameter Page timing

6.26 Data Protection & Power on/off Sequence

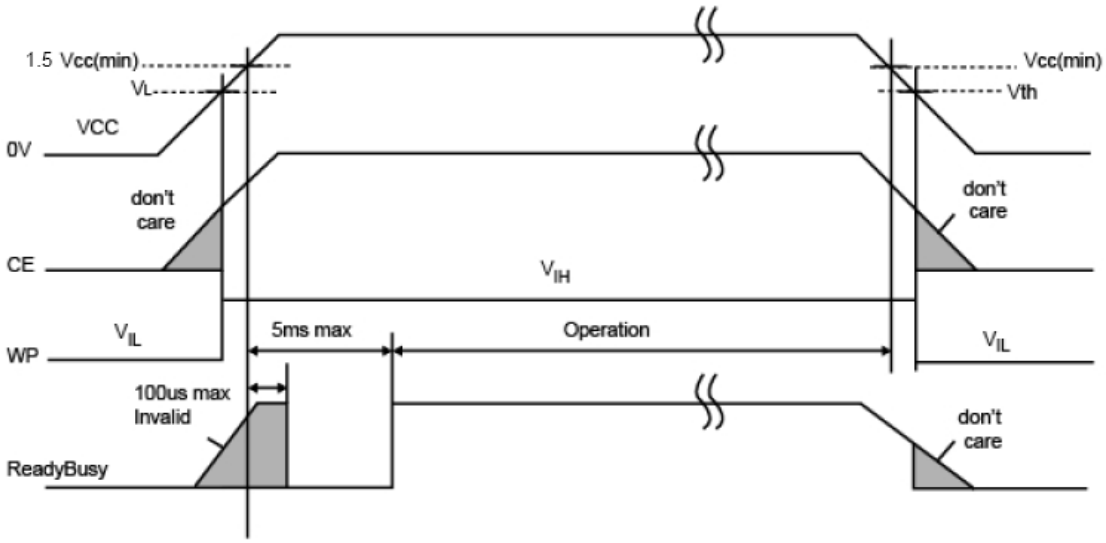
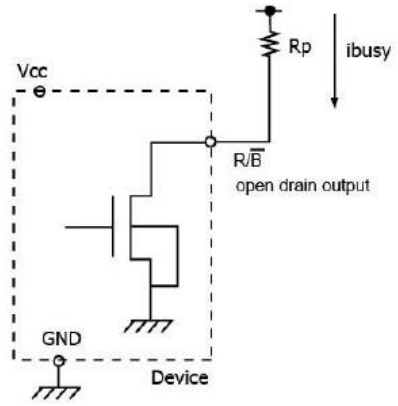
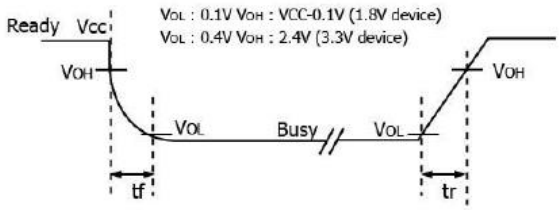


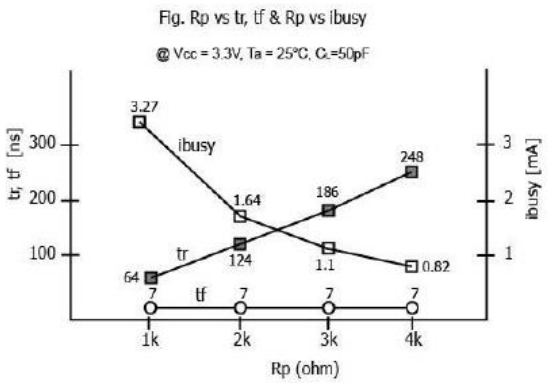
Figure 39. Data Protection and Power on/off

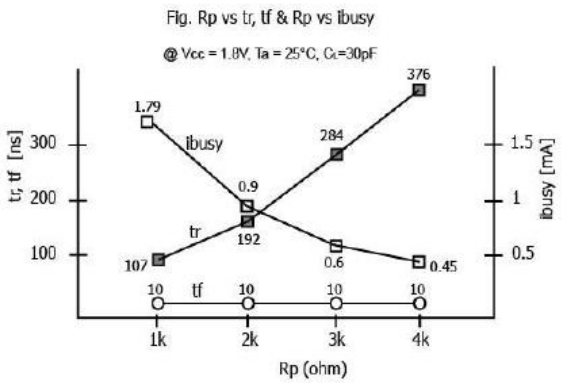
6.27 Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Figure 40). Its value can be determined by the following guidance.









Rp value guidence

$$Rp\ (\text{min } 3.3V \text{ device}) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

$$Rp\ (\text{min } 1.8V \text{ device}) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 40. Ready/Busy Pin Electrical Specifications

6.28 Write Protect Operation

The Erase and Program Operations are automatically reset when WP# goes Low (tWW= 100ns, min). The operations are enabled and disabled as follows.

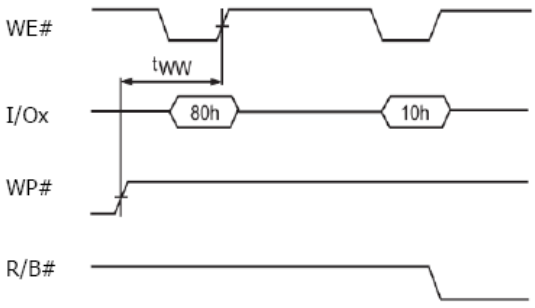


Figure 41. Enable Programming

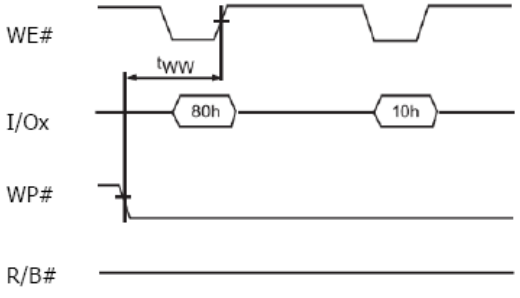


Figure 42. Disable Programming

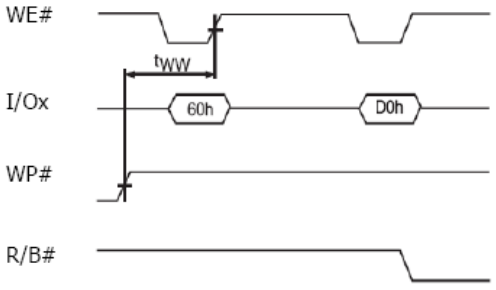


Figure 43. Enable Erase

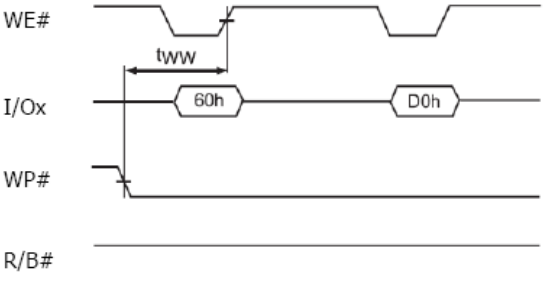


Figure 44. Disable Erase

7. Application Notes and Comments

7.1 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the First and Second page does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 45. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

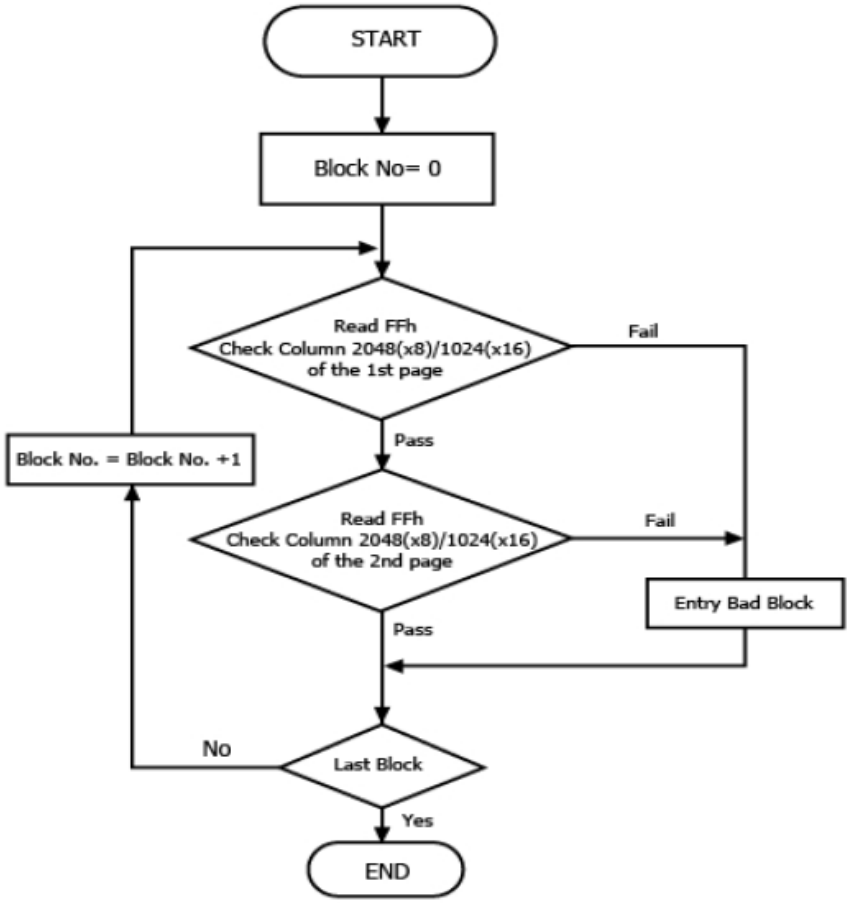


Figure 45 : Bad block management flow chart

Notes:

1. Do not try to erase the detected bad blocks, because the bad bock information will be lost.
2. Do not perform program and erase operation in invalid block, it is impossible to guarantee the Input data and to ensure that the function is normal.

7.2 Bad Block Replacement

This device may have the invalid blocks when shipped from factory. An invalid block is one that contains one or more bad bits. Over the lifetime of the device additional Bad Blocks may develop. In this case, the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block. Bad block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table 23 and Figure 46 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommanded Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC

Table 23. Block failure

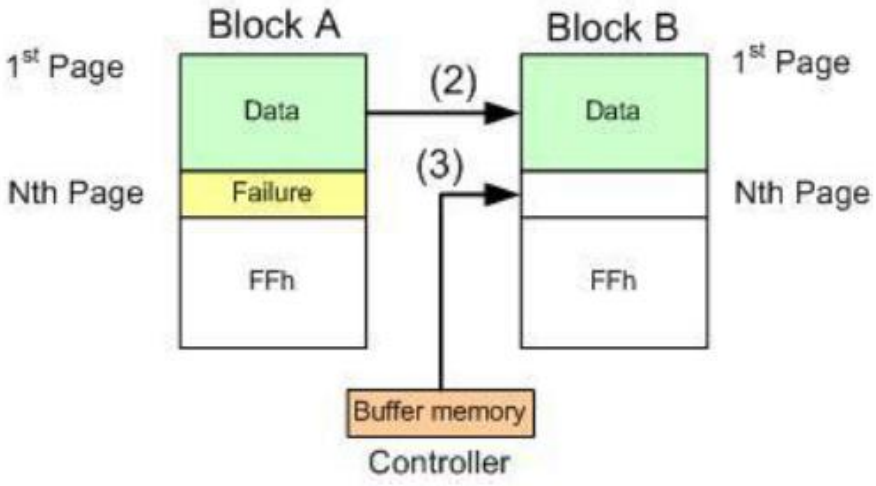


Figure 46. Block replacement

Notes:
1. An error occurs on nth page of the Block A during Program or Erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth page of block A which is in controller buffer memory is copied into nth page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A..

2Gb Low Power DDR2 SDRAM

Revision 0.2

Mar. 2015

Document Title

2Gb(128MX16, 64MX32) Low Power DDR2 SDRAM

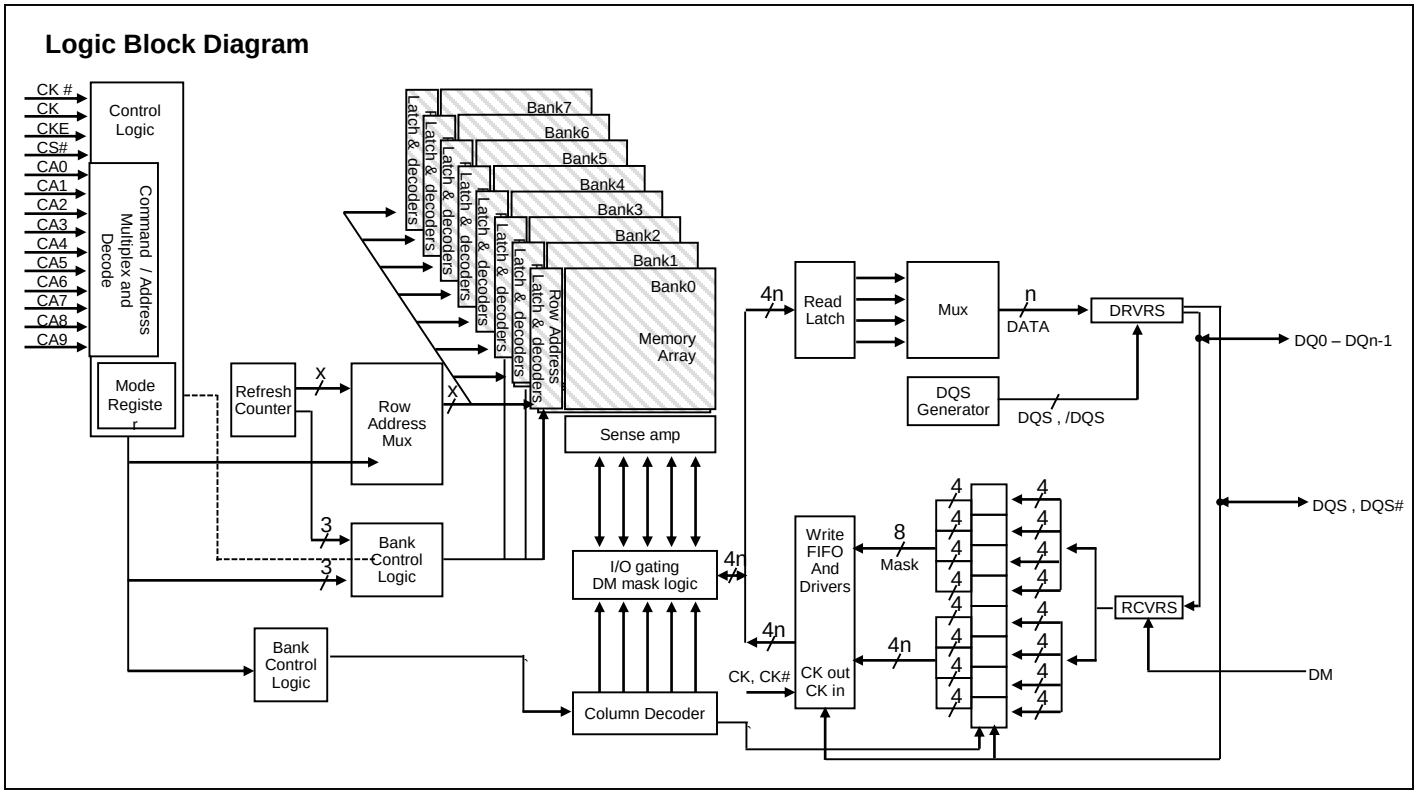
Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Sep. 29th, 2014	Preliminary
0.1	Revised IDD Specification.	Nov. 4th, 2014	Preliminary
0.2	Revised IDD Specification.	Mar. 24th, 2015	Preliminary

DDR2 Sync DRAM Features

- **Functionality**
  - VDD2 = 1.14–1.30V
  - VDDCA/VDDQ = 1.14–1.30V
  - VDD1 = 1.70–1.95V
  - Interface : HSUL_12
  - Data width : x16 / x32
  - Clock frequency range : max 533MHz
  - Four-bit pre-fetch DDR architecture
  - Eight internal banks for concurrent operation
  - Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
  - Bidirectional/differential data strobe per byte of data(DQS/DQS#).
  - DM masks write date at the both rising and falling edge of the data strobe
  - Programmable READ and WRITE latencies (RL/WL)
  - Programmable burst lengths: 4, 8, or 16
  - Auto refresh and self refresh supported
  - All bank auto refresh and per bank auto refresh supported
  - Clock stop capability
- **Configuration**
  - 128 Meg X 16 (16 Meg X 16 X 8 Banks).
  - 64 Meg X 32 (8 Meg X 32 X 8 Banks).
- **Low Power Features**
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - PASR (Partial Array Self Refresh) power-saving mode.
  - DPD (Deep Power Down) Mode.
  - DS (Driver Strength) Control.
- **Timing – Cycle time**
  - 1.875ns @ RL = 8
  - 2.5ns @ RL = 6
  - 3.0ns @ RL = 5
- **Operating Temperature Ranges**
  - Commercial (0℃ to +70℃).
  - Extended (-25℃ to +85℃).
  - Industrial (-40℃ to +85℃).
- **Package**
  - 121-Ball FBGA(8.0mm x 8.0mm x 0.86mm)
  - 134-Ball FBGA(10.0mm x 11.5mm x 1.0mm)

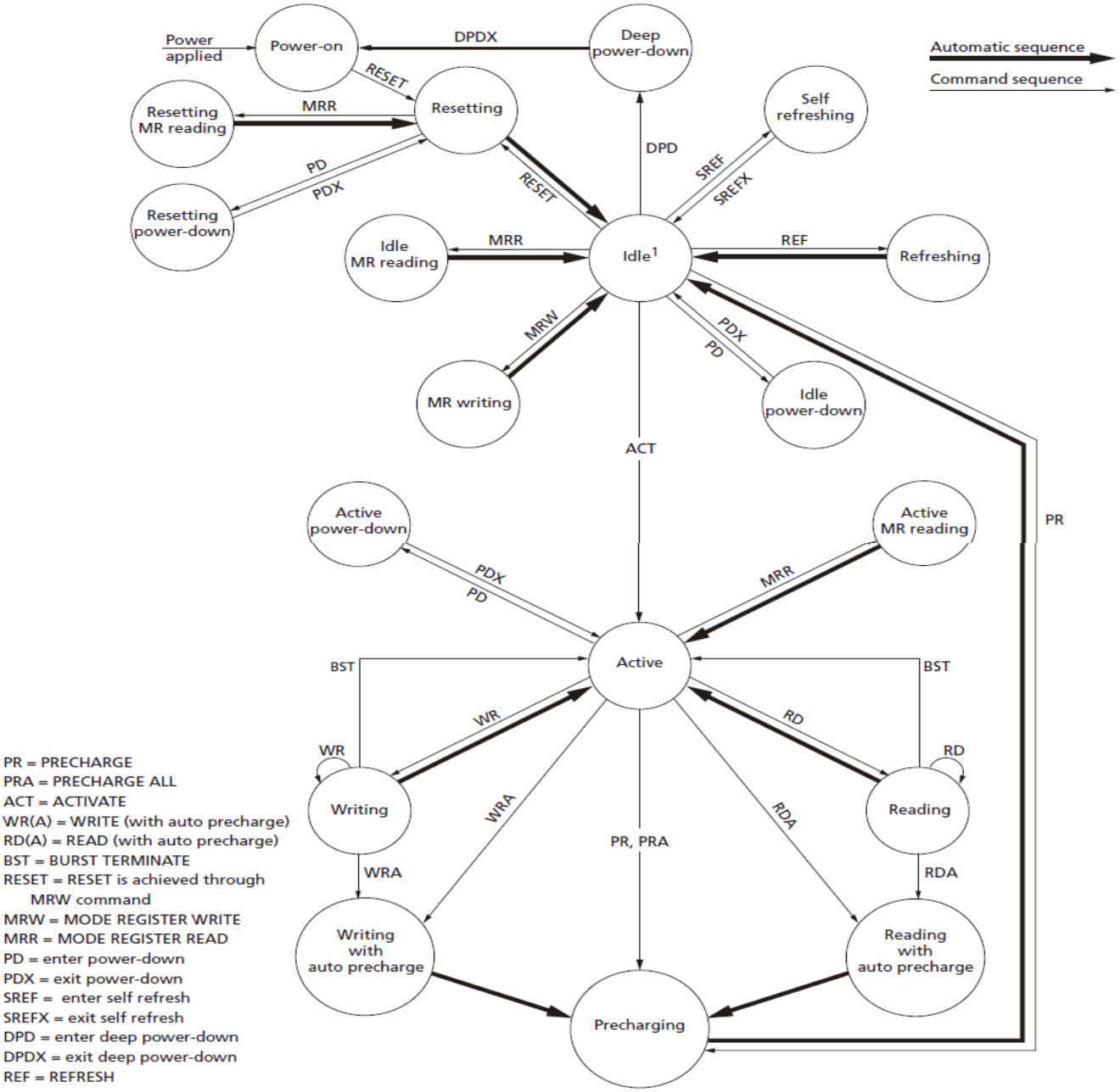
Logic Block Diagram



General Description

The 2Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 2,147,483,648 bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x16's 268,435,456-bit banks is organized as 16,384 rows by 1024 columns by 16 bits. Each of the x32's 268,435,456-bit banks is organized as 16,384 rows by 512 columns by 32 bits.

Simplified Bus Interface State Diagram



Note: 1. All banks are precharged in the idle state.

Address Table

Parameter	128Mb X 16	64Mb X 32
Configuration	16Mb x 8banks x 16	8Mb x 8banks x 32
Bank Address	BA0 ~ BA2	BA0 ~ BA2
Row Address	R0 ~ R13	R0 ~ R13
Column Address	C0 ~ C9	C0 ~ C8

Note : 1. The least-significant column address CA0 is not transmitted on the CA bus, and is implied to be zero.

Pin Description(X16)

Symbol	Type	Description
CK, CK#	Input	**Clock :** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE	Input	**Clock enable :** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS#	Input	**Chip select :** CS# is considered part of the command code and is sampled at the rising edge of CK.
DM0–DM1	Input	**Input data mask :** DM is an input mask signal for WRITE data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[1:0] is DM for each of the two data bytes, respectively.
DQ0 – DQ15	Input	**Data input/output :** Bidirectional data bus.
DQS0 – DQS1 DQS0# – DQS1#	I/O	**Data strobe :** The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[1:0]/DQS[1:0]# is DQS for each of the two data bytes, respectively.
CA0 – CA9	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
VDDQ	Supply	**DQ Power** : Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	**DQ Ground** : Provide isolated ground to DQs for improved noise immunity.
VDDCA	Supply	**Command/address power supply :** Command/address power supply.
VSSCA	Supply	**Command/address ground :** Isolated on the die for improved noise immunity**.**
VDD1	Supply	**Core power :** Supply 1.
VDD2	Supply	**Core power :** Supply 2.
VSS	Supply	**Common ground**
VREFCA, VREFDQ	Supply	**Reference voltage :** VREFCA is reference for command/address input buffers, VREFDQ is reference for DQ input buffers.
ZQ	Reference	**External impedance (240 ohm) :** This signal is used to calibrate the device output impedance for S4 devices. For S2 devices, ZQ should be tied to VDDCA.
DNU	–	**Do not use :** Must be grounded or left floating.
NC	–	**No connect :** Not internally connected.
(NC)	–	**No connect :** Balls indicated as (NC) are no connects, however, they could be connected together internally.

Address Table

Parameter	128Mb X 16	64Mb X 32
Configuration	16Mb x 8banks x 16	8Mb x 8banks x 32
Bank Address	BA0 ~ BA2	BA0 ~ BA2
Row Address	R0 ~ R13	R0 ~ R13
Column Address	C0 ~ C9	C0 ~ C8

Note : 1. The least-significant column address CA0 is not transmitted on the CA bus, and is implied to be zero.

Pin Description(X32)

Symbol	Type	Description
CK, CK#	Input	**Clock :** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE	Input	**Clock enable :** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS#	Input	**Chip select :** CS# is considered part of the command code and is sampled at the rising edge of CK.
DM0–DM3	Input	**Input data mask :** DM is an input mask signal for WRITE data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ0 – DQ31	Input	**Data input/output :** Bidirectional data bus.
DQS0 – DQS3 DQS0# – DQS3#	I/O	**Data strobe :** The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively.
CA0 – CA8	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
VDDQ	Supply	**DQ Power** : Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	**DQ Ground** : Provide isolated ground to DQs for improved noise immunity.
VDDCA	Supply	**Command/address power supply :** Command/address power supply.
VSSCA	Supply	**Command/address ground :** Isolated on the die for improved noise immunity**.**
VDD1	Supply	**Core power :** Supply 1.
VDD2	Supply	**Core power :** Supply 2.
VSS	Supply	**Common ground**
VREFCA, VREFDQ	Supply	**Reference voltage :** VREFCA is reference for command/address input buffers, VREFDQ is reference for DQ input buffers.
ZQ	Reference	**External impedance (240 ohm) :** This signal is used to calibrate the device output impedance for S4 devices. For S2 devices, ZQ should be tied to VDDCA.
DNU	–	**Do not use :** Must be grounded or left floating.
NC	–	**No connect :** Not internally connected.
(NC)	–	**No connect :** Balls indicated as (NC) are no connects, however, they could be connected together internally.

Functional Description

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 8-bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system.

The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a 4*n* pre-fetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or WRITE access for the LPDDR2-S4 effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed.

The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Power-Up

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory (see Figure1). Power-up and initialization by means other than those specified will result in undefined operation.

1. Voltage Ramp

While applying power (after Ta), CKE must be held LOW (≤0.2 ×V_{DDCA}), and all other inputs must be between V_{ILMIN} and V_{IHMAX}. The device outputs remain at High-Z while CKE is held LOW. On or before the completion of the voltage ramp (Tb), CKE must be held LOW. DQ, DM, DQS, and DQS# voltage levels must be Between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch up.

The following conditions apply for voltage ramp :

- Ta is the point when any power supply first reaches 300mV.
- Noted conditions apply betweenTa and power-down (controlled or uncontrolled).
- Tb is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration tINIT0 (Tb -Ta) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any ofVSS,VSSQ, andVSSCA pins must not exceed 100mV.

Voltage Ramp Completion.

After Ta is reached :

- VDD1 must be greater than VDD2 - 200mV
- VDD1 and VDD2 must be greater than VDDCA—200mV
- VDD1 and VDD2 must be greater than VDDQ—200mV
- V_{REF} must always be less than all other supply voltages

Beginning at Tb, CKE must remain LOW for at least tINIT1=100ns, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 = 5 × tCK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (and to subsequent falling and rising edges). If any MRRs are issued, the clock period must be within the range defined for tCKb(18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3=200µs (Td).

2. RESET Command

After tINIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands.

3.MRRs and Device Auto Initialization (DAI) Polling

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down (page 53)).

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of tINIT5, or until the DAI bit is set, before proceeding. Because the memory output buffers are not properly configured by Te, some AC parameters must use relaxed timing specifications before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding.

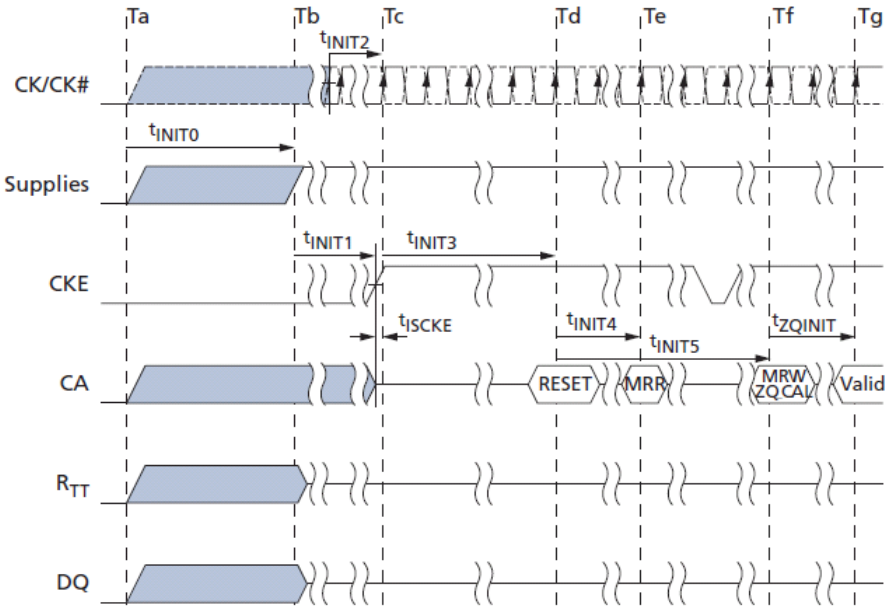
4.ZQ Calibration

After tINIT5 (Tf), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10).
This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands.
The device is ready for normal operation after tZQINIT.

5.Normal Operation

After (Tg), MRW commands must be used to properly configure the memory (output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration. After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop with CKE HIGH (page 62).

Figure 1 : Voltage Ramp and Initialization Sequence



Note : 1. High-Z on the CA bus indicates valid NOP.

Table1 : Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Maximum voltage ramp time
tINIT1	100	-	ns	Minimum CKE LOW time after completion of voltage ramp
tINIT2	5	-	tCK	Minimum stable clock before first CKE HIGH
tINIT3	200	-	µs	Minimum idle time after first CKE assertion
tINIT4	1	-	µs	Minimum idle time after RESET command
tINIT5	-	10	µs	Maximum duration of device auto initialization
tZQINIT	1	-	µs	ZQ initial calibration (S4 devices only)
tCKb	18	-	ns	Clock cycle time during boot

Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Power-Off

While powering off, CKE must be held LOW (≤0.2 ×VDDCA); all other inputs must be between V_{ILMIN} and V_{IHMAX}.
The device outputs remain at High-Z while CKE is held LOW. DQ, DM, DQS, and DQS# voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table. Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Required Power Supply Conditions Between Tx and Tz:

- VDD1 must be greater than VDD2 - 200mV.
- VDD1 must be greater than VDDCA - 200mV.
- VDD1 must be greater than VDDQ - 200mV.
- VREF must always be less than all other supply voltages.

The voltage difference between VSS,VSSQ, and VSSCA must not exceed 100mV.
For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off.
  The time between Tx and Tz must not exceed tPOFF. During this period, the relative voltage between power supplies is uncontrolled. VDD1 andVDD2 must decrease with a slope lower than 0.5V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table2 : Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	tPOFF	-	2	Sec

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignments and Definitions

The MRR command is used to read from a register.The MRW command is used to write to a register. An “R” in the access column of the mode register assignment table indicates read-only; a “W” indicates write-only; “R/W” indicates read or WRITE capable or enabled.

Table3 : Mode Register Assignments

MR #	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	RFU			RZQI		DNVI	DI	DAI	go to MR0
1	01h	Device feature 1	W	*nWR (for AP)*			WC	BT	BL			go to MR1
2	02h	Device feature 2	W	RFU					RL and WL			go to MR2
3	03h	I/O config-1	W	RFU					DS			go to MR3
4	04h	SDRAM refresh rate	R	TUF	RFU				Refresh rate			go to MR4
5	05h	Basic config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06h	Basic config-2	R	Revision ID1								go to MR6
7	07h	Basic config-3	R	Revision ID2								go to MR7
8	08h	Basic config-4	R	I/O width		Density				Type		go to MR8
9	09h	Test mode	W	Vendor-specific test mode								go to MR9
10	0Ah	I/O calibration	W	Calibration code								go to MR10
11-15	0Bh≈0Fh	Reserved	-	RFU								go to MR11
16	10h	PASR_Bank	W	Bank mask								go to MR16
17	11h	PASR_Seg	W	Segment mask								go to MR17
18-19	12h–13h	Reserved	-	RFU								go to MR18
20-31	14h–1Fh	Reserved for NVM										go to MR30
32	20h	DQ calibration pattern A	R	See Table 28								go to MR32
33-39	21h–27h	Do not use										go to MR33
40	28h	DQ calibration pattern B	R	See Table 28								go to MR40
41-47	29h–2Fh	Do not use										go to MR41
48-62	30h–3Eh	Reserved	-	RFU								go to MR48
63	3Fh	RESET	W	X								go to MR63
64-126	40h–7Eh	Reserved	-	RFU								go to MR64
127	7Fh	Do not use										go to MR127
128-190	80h–BEh	Reserved for vendor use		RVU								go to MR128
191	BFh	Do not use										go to MR191
192-254	C0h–FEh	Reserved for vendor use		RVU								go to MR192
255	FFh	Do not use										go to MR255

Notes : 1. RFU bits must be set to 0 during MRW.

2. RFU bits must be read as 0 during MRR.

3. For READs to a write-only or RFU register, DQS will be toggled and undefined data is returned.

4. RFU mode registers must not be written.

5. WRITEs to read-only registers must have no impact on the functionality of the device.

Table4 : MR0 Device information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read–only	OP0	0b : DAI complete 1b : DAI still in progress
DI (Device Information)	Read–only	OP1	0b : SDRAM 1b : NVM
DNVI (Data Not Valid Information)	Read–only	OP2	LPDDR2 SDRAM will not implement DNV functionality
RZQI(Built in Self Test for RZQ Information)	Read–only	OP[4:3]	00b : RZQ self test not executed 01b : ZQ-pin may connect to VDDCA or float 10b : ZQ-pin may short to GND 11b : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)

Notes : 1. If RZQI is supported, it will be set upon completion of the MRW ZQ initialization calibration.

2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] must be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 could indicate a ZQ-pin assembly error. It is recommended that the assembly error be corrected.

3. In the case of a possible assembly error(either OP[4:3]=01 or OP[4:3]=10, as defined above), the device will default to factory trim settings for RON and will ignore ZQ calibration commands. In either case, the system might not function as Intended.

4. If a ZQ self test returns a value of 11b, this indicates that the device has detected a resistor connection to the ZQ pin. Note that this result cannot be used to validate the ZQ resistor value, nor does it indicate that the ZQ resistor tolerance meets the specified limits (240 ohms ±1%).

Table5 : MR1 Device Feature 1 (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write - only	OP[2:0]	010b : BL4 (default) 011b : BL8 100b : BL16 All others : reserved
BT	Write - only	OP3	0b : Sequential (default) 1b : Interleaved
WC	Write – only	OP4	0b : Wrap (default) 1b : No wrap (allowed for SDRAM BL4 only)
nWR	Write – only	OP[7:5]	001b : nWR = 3 (default) 010b : nWR = 4 011b : nWR = 5 100b : nWR = 6 101b : nWR = 7 110b : nWR = 8 All others : reserved

Note : 1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR / tCK).

Table6 : Burst Sequence by Burst Length(BL), Burst Type(BT), and Wrap Control(WC)

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	46
4	Any	X	X	0b	0b	Wrap	0	1	2	3												
		X	X	1b	0b		2	3	0	1												
	Any	X	X	X	0b	No Wrap	*y*	*y*+1	*y*+2	*y*+3												
8	Seq	X	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	4	5	6	7	0	1								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	0	1	2	3	4	5								
	Int	X	0b	0b	0b		0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	0	1	6	7	4	5								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	4	5	2	3	0	1								
	Any	X	X	X	0b	No Wrap	illegal (not supported)															
16	Seq	0b	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	Int	X	X	X	0b		illegal (not supported)															
	Any	X	X	X	0b	No Wrap	illegal (not supported)															

Notes : 1. C0 input is not present on CA bus. It is implied zero.

2. For BL = 4, the burst address represents C[1:0].

3. For BL = 8, the burst address represents C[2:0].

4. For BL = 16, the burst address represents C[3:0].

5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary.

The variable *y* can start at any address with C0 equal to 0, but must not start at any address shown in the following table.

Table7 : No – Wrap Restrictions

Bus Width	2Gb
Not across full page boundary	
X 16	3FE, 3FF, 000, 001
X 32	1FE, 1FF, 000, 001
Not across full page boundary	
X 16	1FE, 1FF, 200, 201
X 32	None

Note : 1. No-wrap BL = 4 data orders shown are prohibited.

Table8 : MR2 Device Feature 2 (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				RL and WL			

RL and WL	Write - only	OP [3:0]	0001b : RL=3 / WL=1 (default)
			0010b : RL=4 / WL=2
			0011b : RL=5 / WL=2
			0100b : RL=6 / WL=3
			0101b : RL=7 / WL=4
			0110b : RL=8 / WL=4
			All others : reserved

Table9 : MR3 I/O Configuration 1 (MA [7:0] =03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

DS	Write - only	OP [3:0]	0000b : reserved
			0001b : 34.3 ohm typical
			0010b : 40 ohm typical
			0011b : 48 ohm typical
			0100b : 60 ohm typical
			0101b : reserved for 68.6 ohm typical
			0110b : 80 ohm typical
			0111b : 120 ohm typical
			All others : reserved

Table10 : MR4 Device Temperature (MA [7:0] =04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU				SDRAM Refresh Rate		

SDRAM Refresh rate	Read - only	OP [2:0]	000b : SDRAM Low temperature operating limit exceeded.
			001b : 4x tREF, 4x tREFIpb, 4x tREFW.
			010b : 2x tREF, 2x tREFIpb, 2x tREFW.
			011b : 1x tREF, 1x tREFIpb, 1x tREFW (<= 85℃).
			100b : Reserved.

SDRAM Refresh rate	Read - only	OP [2:0]	101b : 0.25x tREF, 0.25x tREFlpb, 0.25x tREFW, do not de-rate SDRAM AC timing .
			110b : 0.25x tREF, 0.25x tREFlpb, 0.25x tREFW, de-rate SDRAM AC timing .
			111b : SDRAM High temperature operating limit exceeded.
Temperature Update Flag (TUF)	Read - only	OP7	0b : OP [2:0] value has not changed since last read of MR4.
			1b : OP [2:0] value has changed since last read of MR4.
RL and WL	Write – only	OP [3:0]	0001b : RL=3 / WL=1 (default)
			0010b : RL=4 / WL=2
			0011b : RL=5 / WL=2
			0100b : RL=6 / WL=3
			0101b : RL=7 / WL=4
			0110b : RL=8 / WL=4
			All others : reserved

Notes:

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up
3. If OP2 equals '1', the device temperature is greater than 85℃
4. OP7 is set to'1' if OP2-OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP[2:0] = 000b or 111b.
6. LPDDR2 devices must be de-rated by adding 1.875ns to the following core timing parameters ; tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in AC timing table.
   Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
7. The recommended frequency for reading MR4 is provided in Temperature Sensor.

Table11 : MR5 Basic Configuration 1 (MA [7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							
LPDDR2 Manufacturer ID		Read-only		OP[7:0]		0000 0000b : Fidelix	
						All others : Reserved	

Table12 : MR6 Basic Configuration 2 (MA [7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							
Revision ID1		Read-only		OP[7:0]		0000 0000b : A-version	

Table13 : MR7 Basic Configuration 3 (MA [7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							
Revision ID2		Read-only		OP[7:0]		0000 0000b : A-version	

Table14 : MR8 Basic Configuration 4 (MA [7:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read – only	OP [1:0]	00b : S4 SDRAM
Density	Read – only	OP [5:2]	0100b : 1Gb
			0101b : 2Gb
			0110b : 4Gb
I/O width	Read – only	OP [7:6]	00b : x32
			01b : x16

Table15 : MR9 Test Mode (MA [7:0] = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor – specific Test Mode							

Table16 : MR10 Calibration (MA [7:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write - only	OP [7:0]	0xFF : Calibration command after initialization.
			0xAB : Long calibration
			0x56 : Short calibration
			0xC3 : ZQ Reset
			All others : Reserved

Notes : 1. Host processor must not write MR10 with reserved values.

2. The device ignores calibration commands when a reserved value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see MRW ZQ Calibration Commands (page 51)) or default calibration (through the ZQRESET command) is supported.
   If ZQ is connected to V_{DDCA}, the device operates with default calibration and ZQ calibration commands are ignored.
   In both cases, the ZQ connection must not change after power is supplied to the device.

Table17 : MR[11-15] Reserved (MA [7:0] = 0BH – 0FH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

Table18 : MR16 PASR Bank Mask (MA [7:0] = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask (4-bank or 8-bank)							

Bank [7:0] Mask	Write - only	OP [7:0]	0b : Refresh enable to the bank = unmasked (default)
			1b : Refresh blocked = masked

Table19 : MR17 PASR Segment Mask (MA [7:0] = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment	Write – only	OP [7:0]	0b : Refresh enable to the Segment = unmasked (default)
			1b : Refresh blocked = masked

Segment [7:0] Mask	OP	Segment Mask	R [13:11]
0	0	XXXXXXX1	000b
1	1	XXXXXX1X	001b
2	2	XXXXX1XX	010b
3	3	XXXX1XXX	011b
4	4	XXX1XXXX	100b
5	5	XX1XXXXX	101b
6	6	X1XXXXXX	110b
7	7	1XXXXXXX	111b

Table20 : Reserved Mode Register

Mode Register	MA	0	Restriction	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR[18:19]	MA[7:0]	12h-13h	RFU	Reserved							
MR[20:31]		14h-1Fh	NVM[1]								
MR[33:39]		21h-27h	DNU[1]								
MR[41:47]		29h-2Fh									
MR[48:62]		30h-3Eh	RFU								
MR[64:126]		40h-7Eh	RFU								
MR[127]		7Fh	DNU								
MR[128:190]		80h-BEh	RVU[1]								
MR[191]		BFh	DNU								
MR[192:254]		C0h-FEh	RVU								
MR[255]		FFh	DNU								

Note : 1. NVM = nonvolatile memory use only; DNU = Do not use; RVU = Reserved for vendor use.

Table21 : MR63 Reset (MA [7:0] = 3FH) – MRW Only

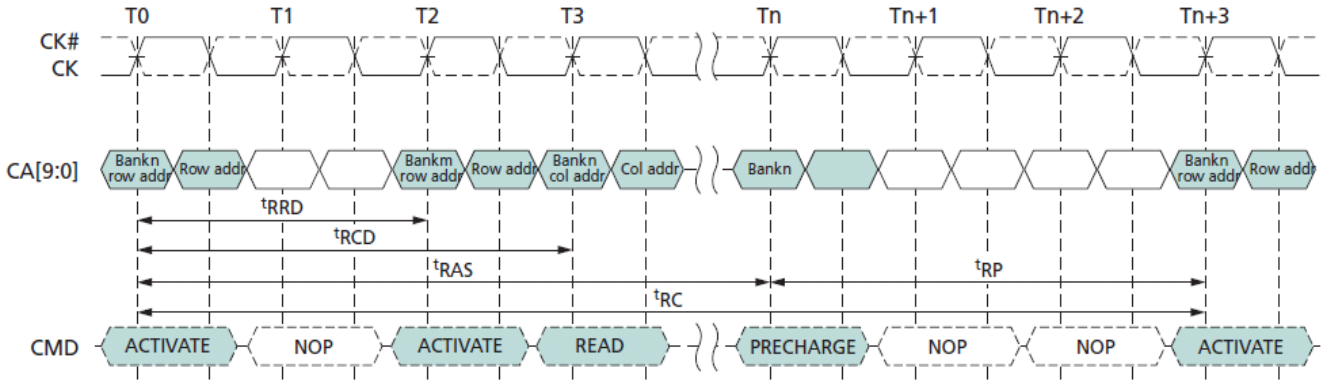
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note : For additional information on MRW RESET see MODE REGISTER WRITE Command (page 50).

ACTIVATE Command

The ACTIVATE command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock.
The bank addresses BA[2:0] are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at tRCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank.The bank active and precharge times are defined as tRAS and tRP, respectively.
The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

Figure 2: ACTIVATE Command



Notes : 1. tRCD = 3, tRP = 3, tRRD = 2.
2. A PRECHARGE ALL command uses tRPab timing, and a single-bank PRECHARGE command uses tRPpb timing. In this figure, tRP is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

8-Bank Device Operation

Two rules regarding 8-bank device operation must be observed.
One rule restricts the number of sequential ACTIVATE commands that can be issued; the second provides additional RAS precharge time for a PRECHARGE ALL command.

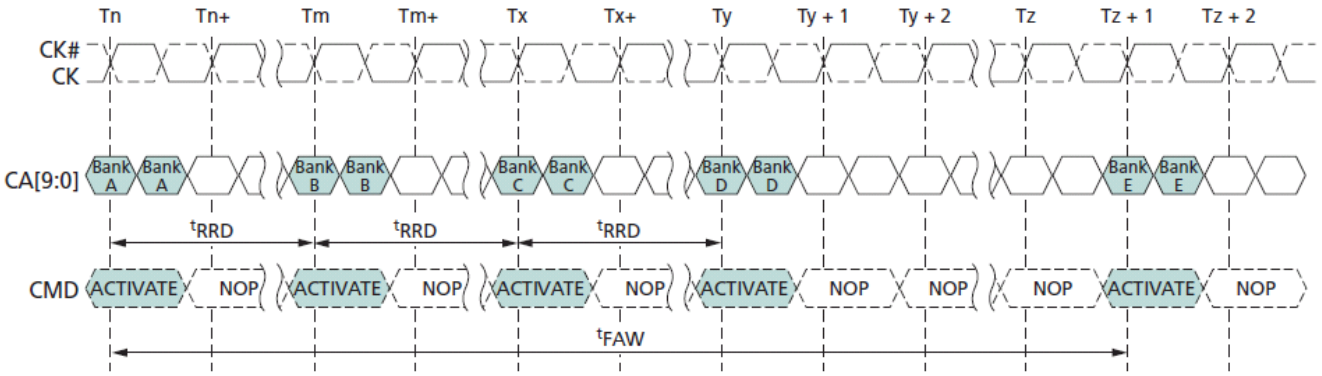
The 8-Bank Device Sequential Bank Activation Restriction :

No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. To convert to clocks, divide tFAW[ns] by tCK[ns], and round up to the next integer value.
For example, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock *n*, no more than three further ACTIVATE commands can be issued at or between clock *n* + 1 and *n* + 9. REFpb also counts as bank activation for purposes of tFAW.

The 8-Bank Device PRECHARGE ALL Provision:

tRP for a PRECHARGE ALL command must equal tRPab, which is greater than tRPpb.

Figure 3 : tFAW Timing (8-Bank Devices)



Note : 1. Exclusively for 8-bank devices.

Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles. A new burst access must not interrupt the previous 4-bit burst operation when BL = 4. When BL = 8 or BL = 16, READs can be interrupted by READs andWRITEs can be interrupted byWRITEs, provided that the interrupt occurs on a 4-bit boundary and that tCCD is met.

Burst READ Command

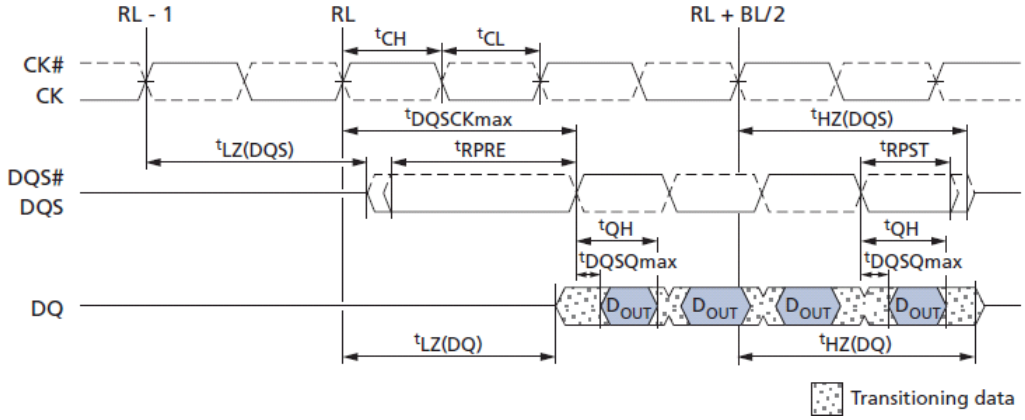
The burst READ command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the tDQSCK delay is measured.The first valid data is available RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock when the READ command is issued.

The data strobe output is driven LOW tRPRE before the first valid rising strobe edge.

The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers.

Pin input timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

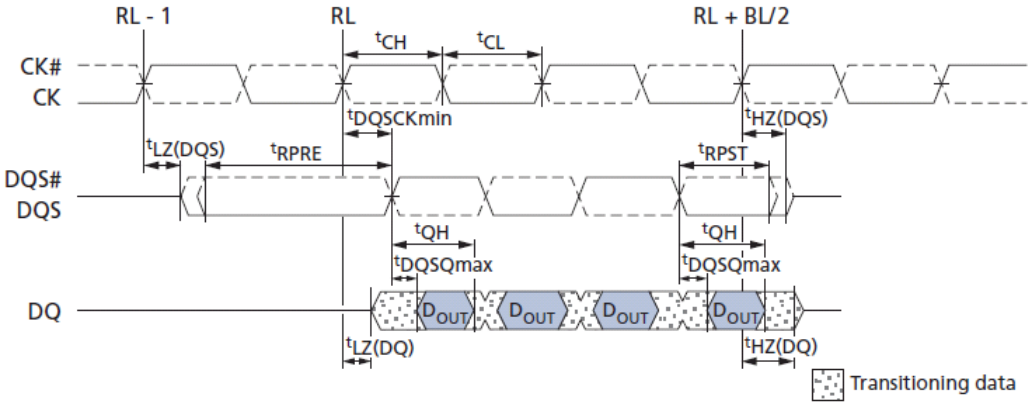
Figure 4 : READ Output Timing – tDQSCK (MAX)



Notes : 1. tDQSCK can span multiple clock periods.

2 An effective burst length of 4 is shown.

Figure 5 : READ Output Timing – tDQSCK (MIN)



Note : 1. An effective burst length of 4 is shown.

Figure 6 : Burst READ – RL = 5, BL = 4, tDQSCK > tCK

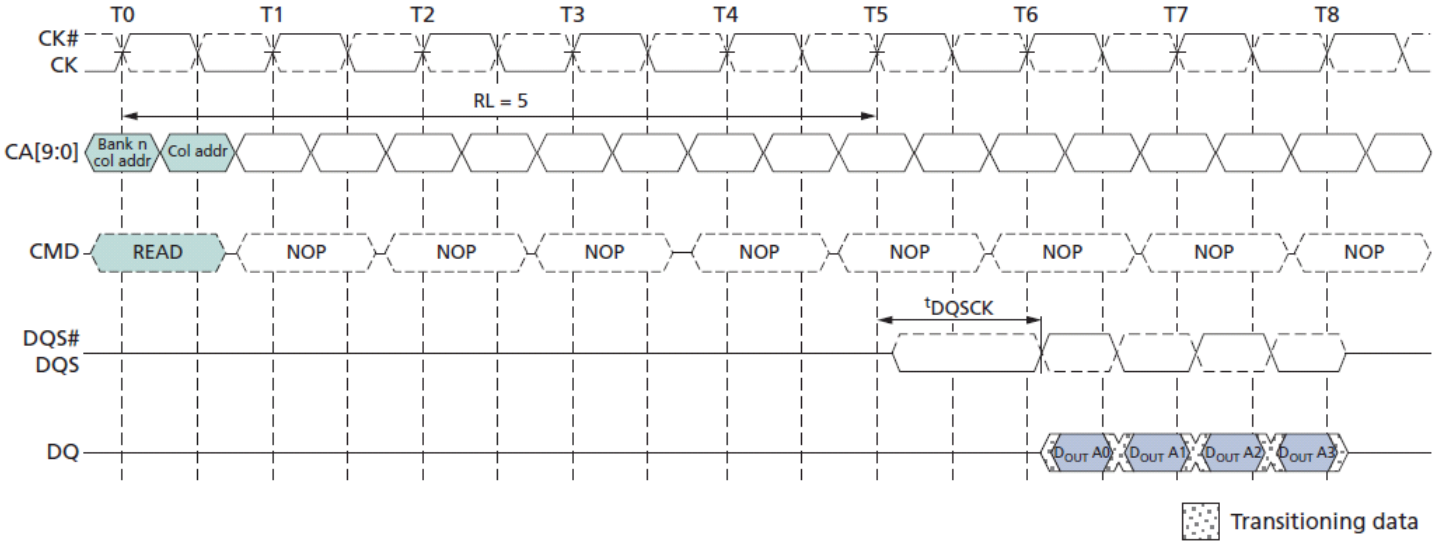


Figure 7 : Burst READ – RL = 3, BL = 8, tDQSCK < tCK

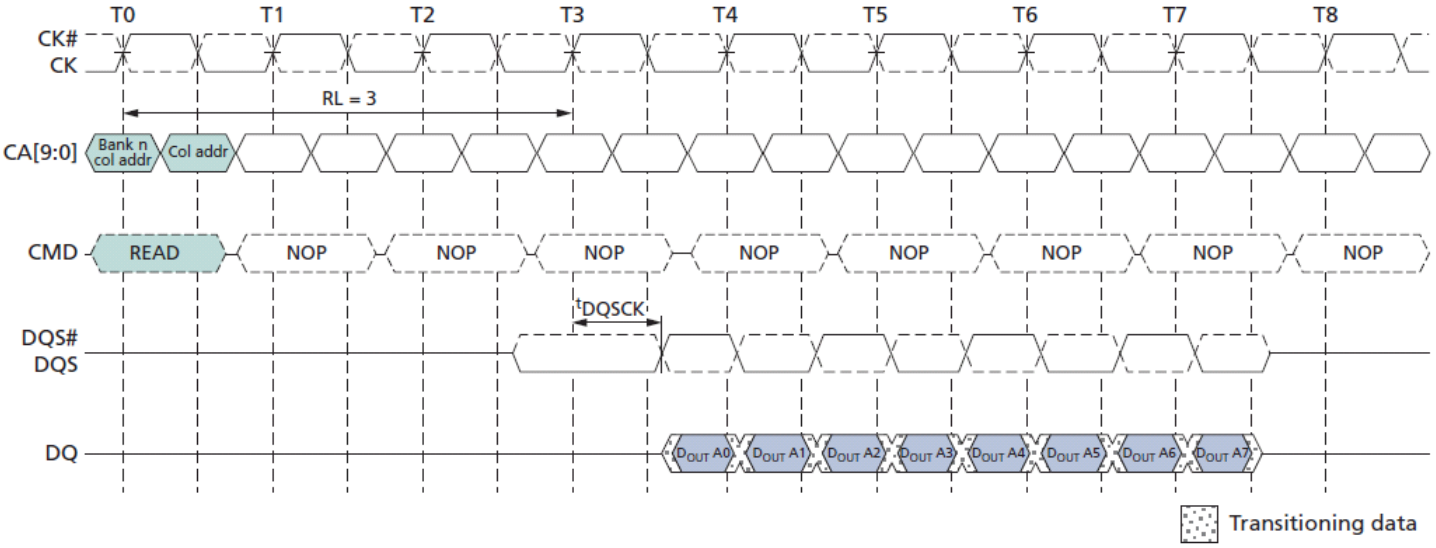
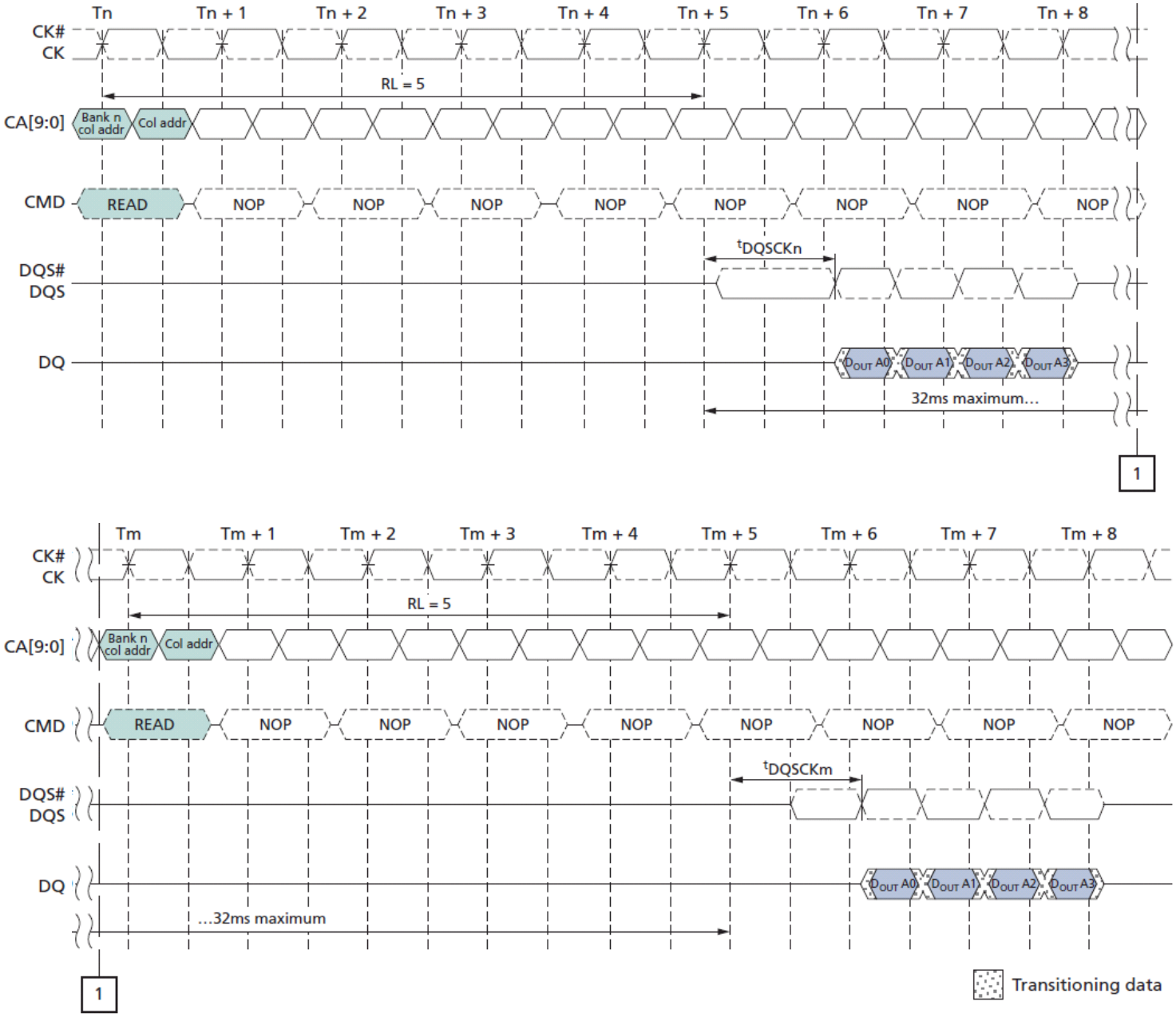


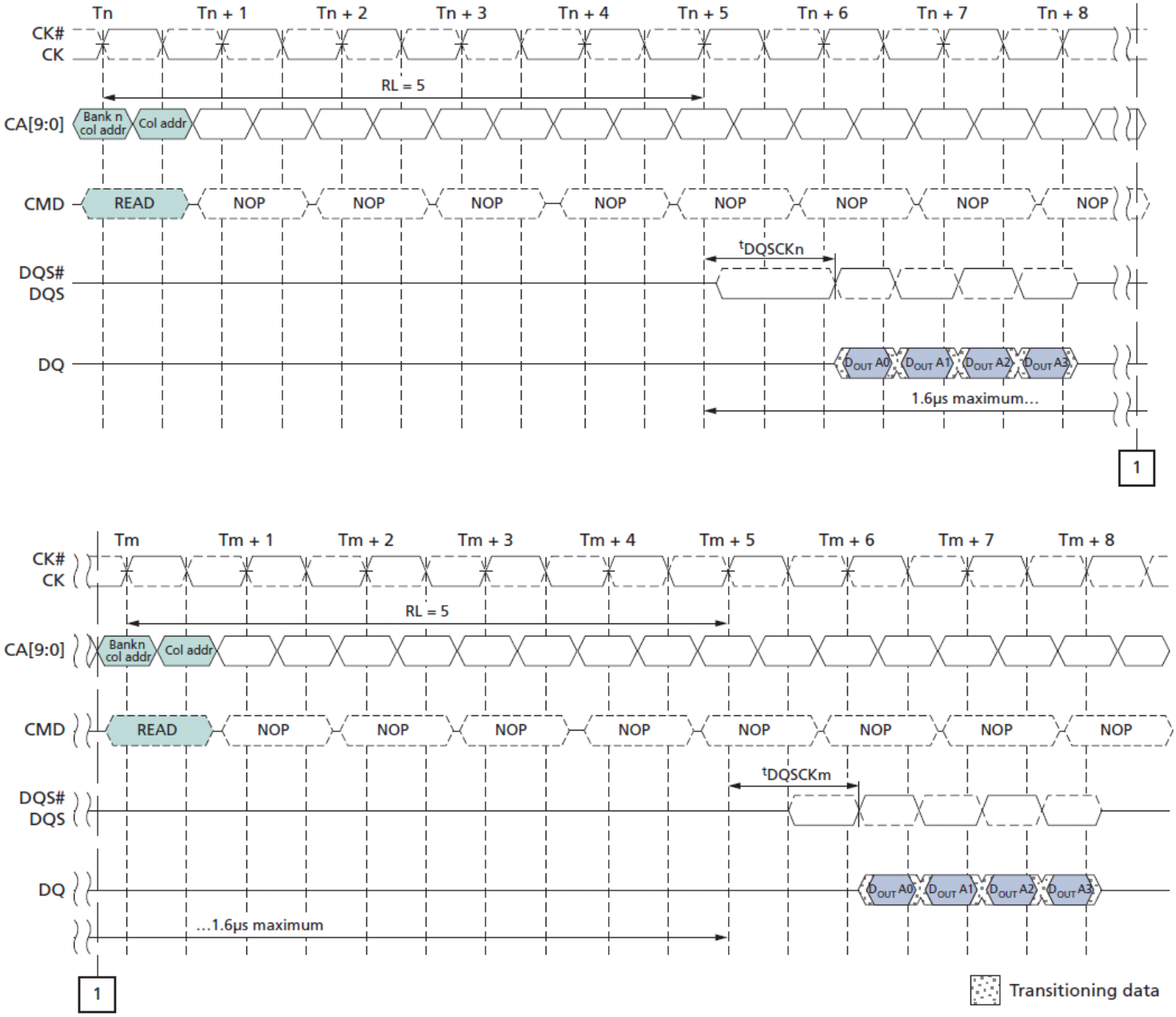
Figure 8 : tDQSCKDL Timing



Notes : 1. tDQSCKDL = (tDQSCK*n* - tDQSCK*m*).

2. tDQSCKDL (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair within any 32ms rolling window.

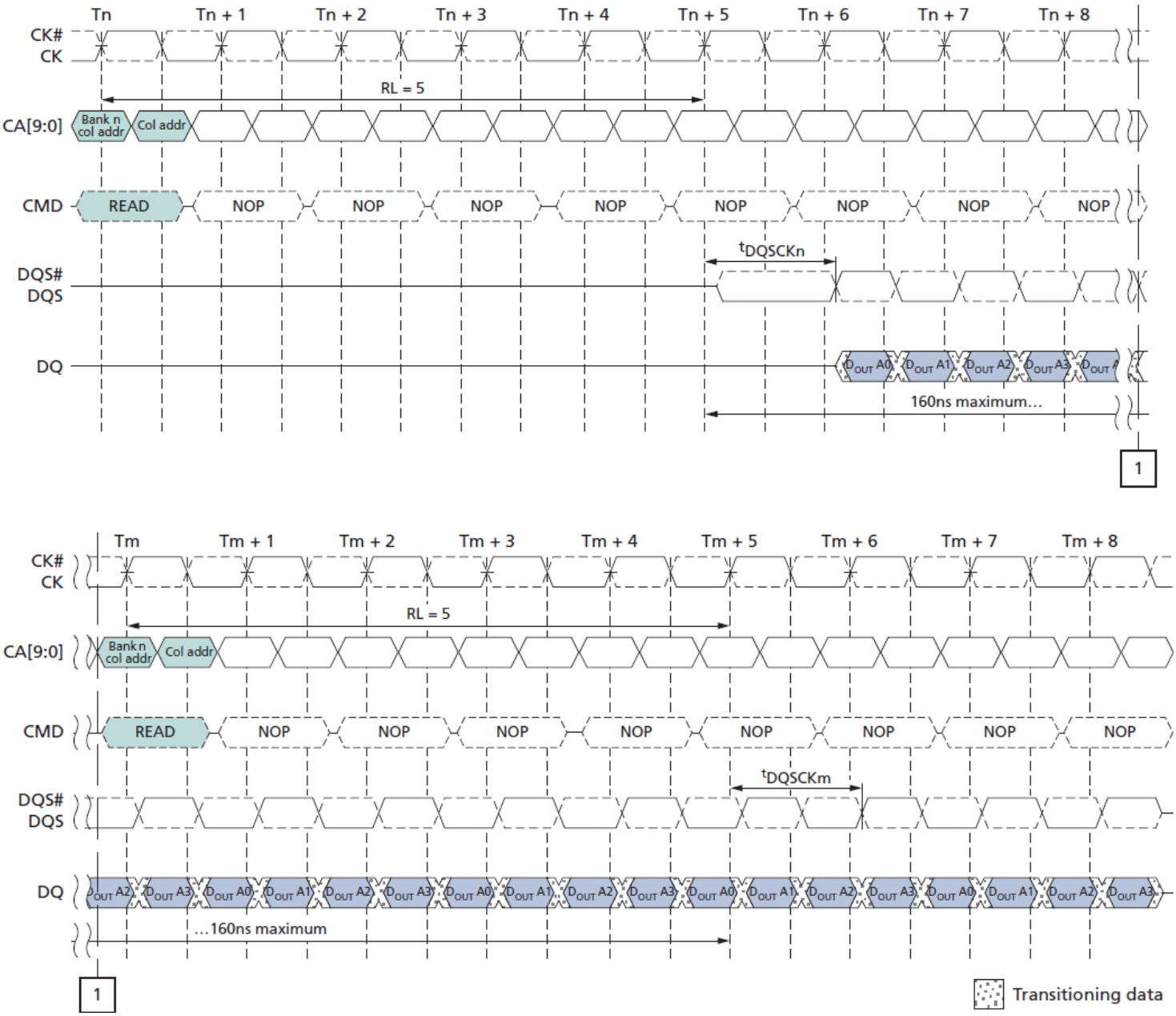
Figure 9 : tDQSCKDM Timing



Notes : 1. tDQSCKDM = (tDQSCK*n* - tDQSCK*m*).

2. tDQSCKDM (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair within any 1.6µs rolling window.

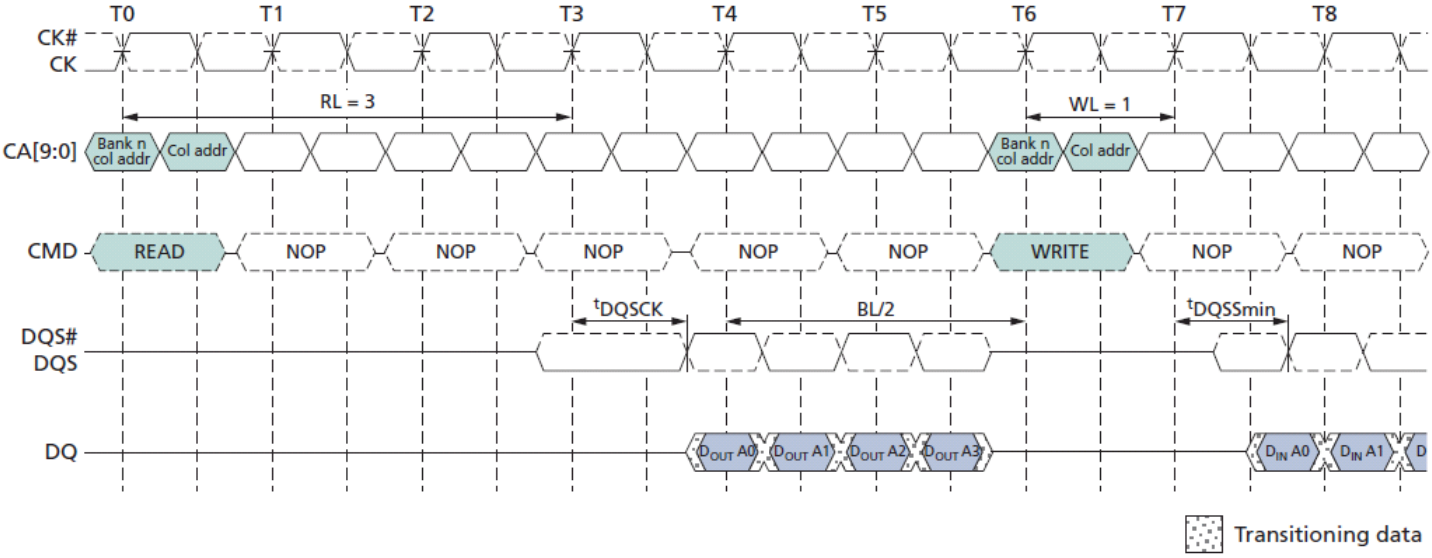
Figure 10 : tDQSCKDS Timing



Notes : 1. tDQSCKDS = (tDQSCK*n* - tDQSCK*m*).

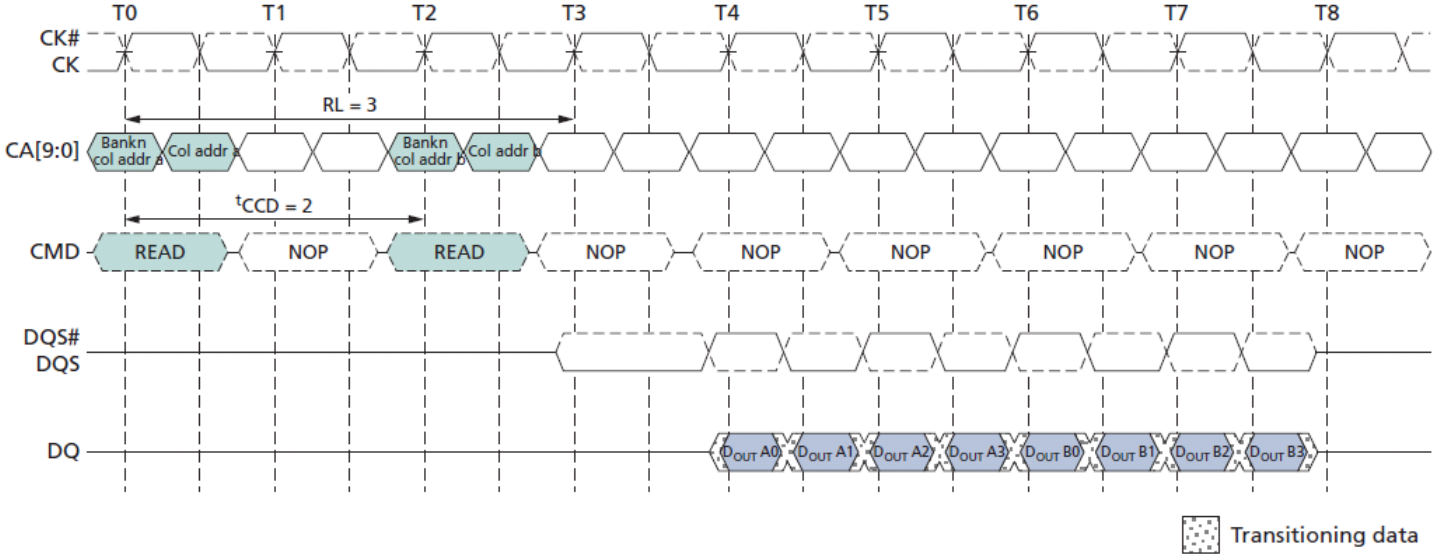
2. tDQSCKDS (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair for READs within a consecutive burst, within any 160ns rolling window.

Figure 11: Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4



The minimum time from the burst READ command to the burstWRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 -WL clock cycles. Note that if a READ burst is truncated with a burstTERMINATE (BST) command, the effective burst length of the truncated READ burst should be used for BL when calculating the minimum READ-to-WRITE delay.

Figure 12: Seamless Burst READ – RL = 3, BL = 4, CCD = 2



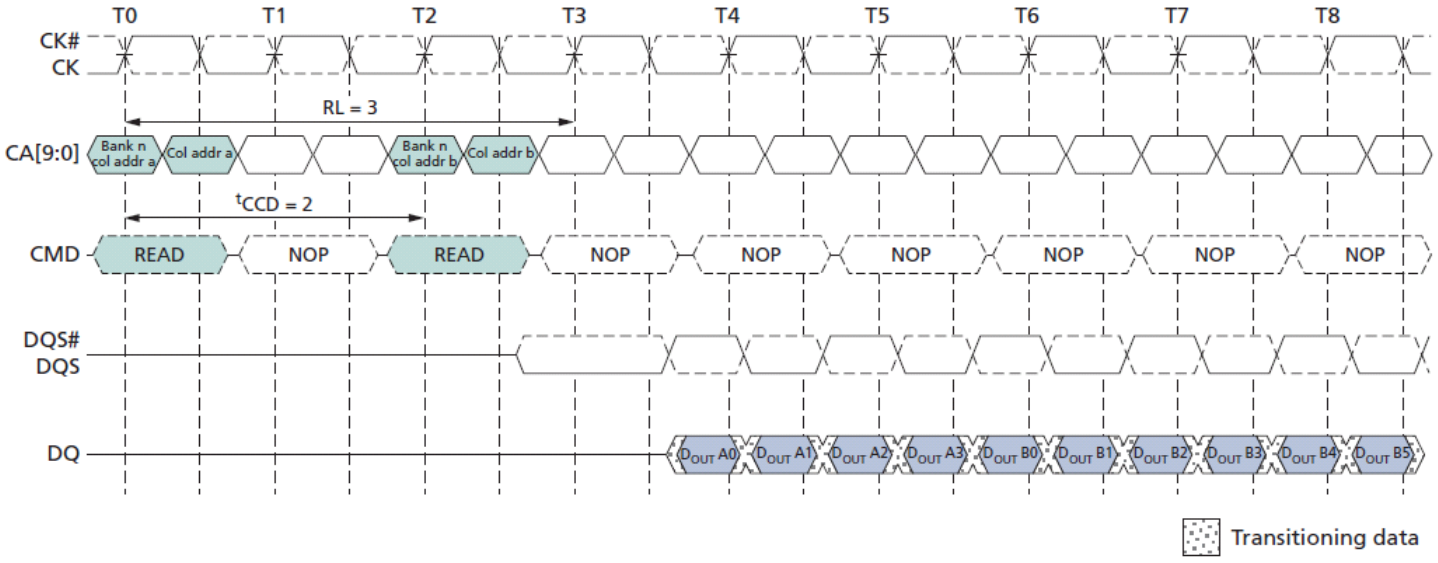
A seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL = 16 operation.
This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

READs Interrupted by a READ

A burst READ can be interrupted by another READ with a 4-bit burst boundary, provided that tCCD is met.

A burst READ can be interrupted by other READs on any subsequent clock, provided that tCCD is met.

Figure 13: READ Burst Interrupt Example – RL = 3, BL = 8, tCCD = 2



Note : 1. READs can only be interrupted by other READs or the BST command.

Burst WRITE Command

The burstWRITE command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock.

The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst.

Write latency (WL) is defined from the rising edge of the clock on which theWRITE command is issued to the rising edge of the clock from which the tDQSS delay is measured.The first valid data must be drivenWL × tCK + tDQSS from the rising edge of the clock from which the WRITE command is issued.The data strobe signal (DQS) must be driven LOW tWPRE prior to data input.

The burst cycle data bits must be applied to the DQ pins tDS prior to the associated edge of the DQS and held valid until tDH after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed.

After a burstWRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued.

Pin input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

Figure 14 : Data Input (WRITE) Timing

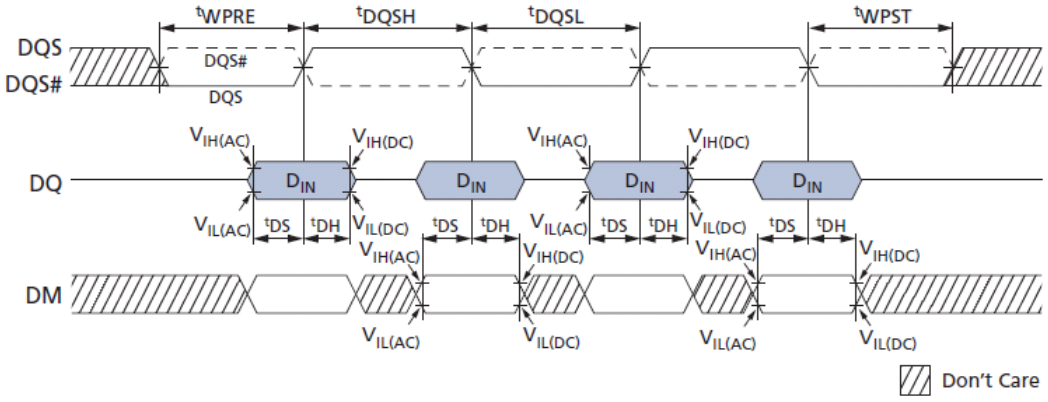


Figure 15 : Burst WRITE – WL = 1, BL = 4

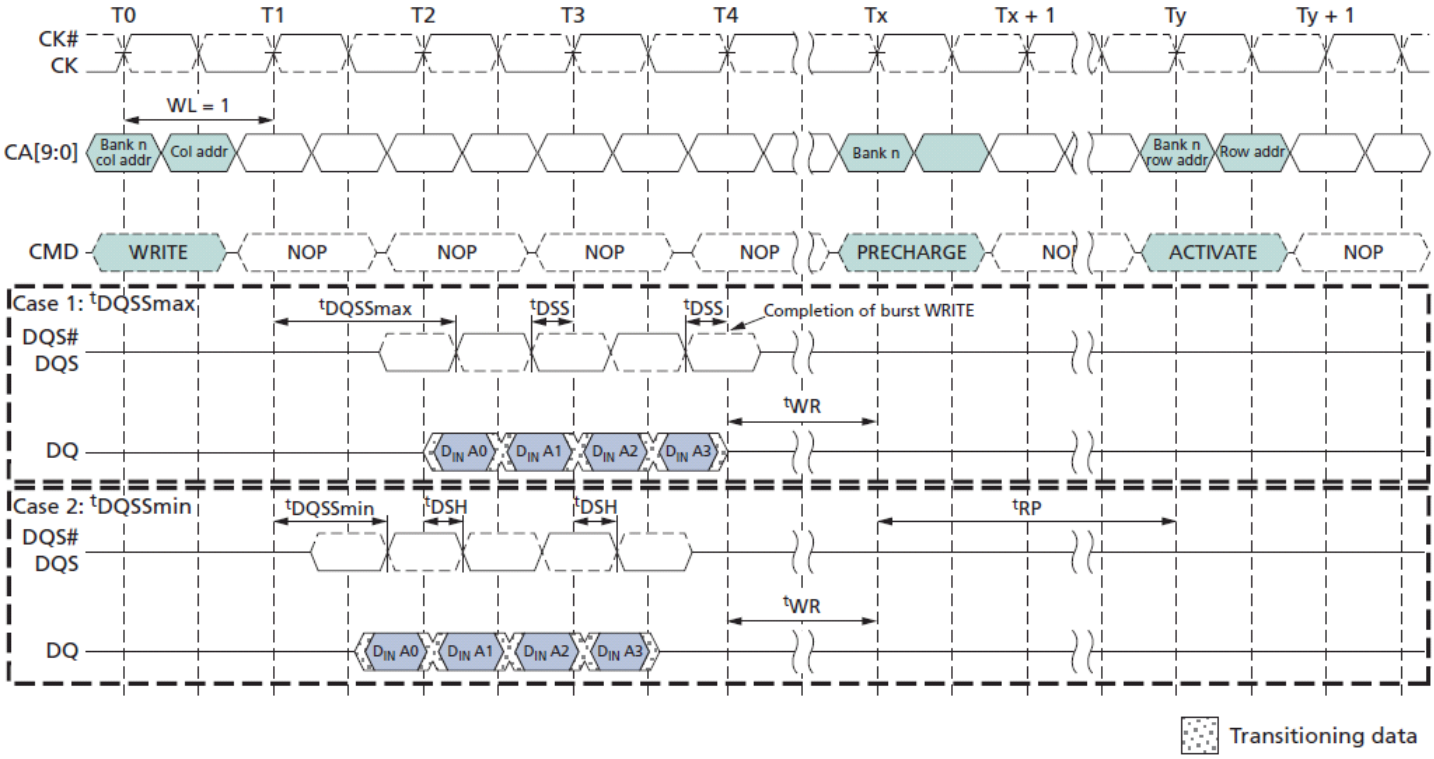
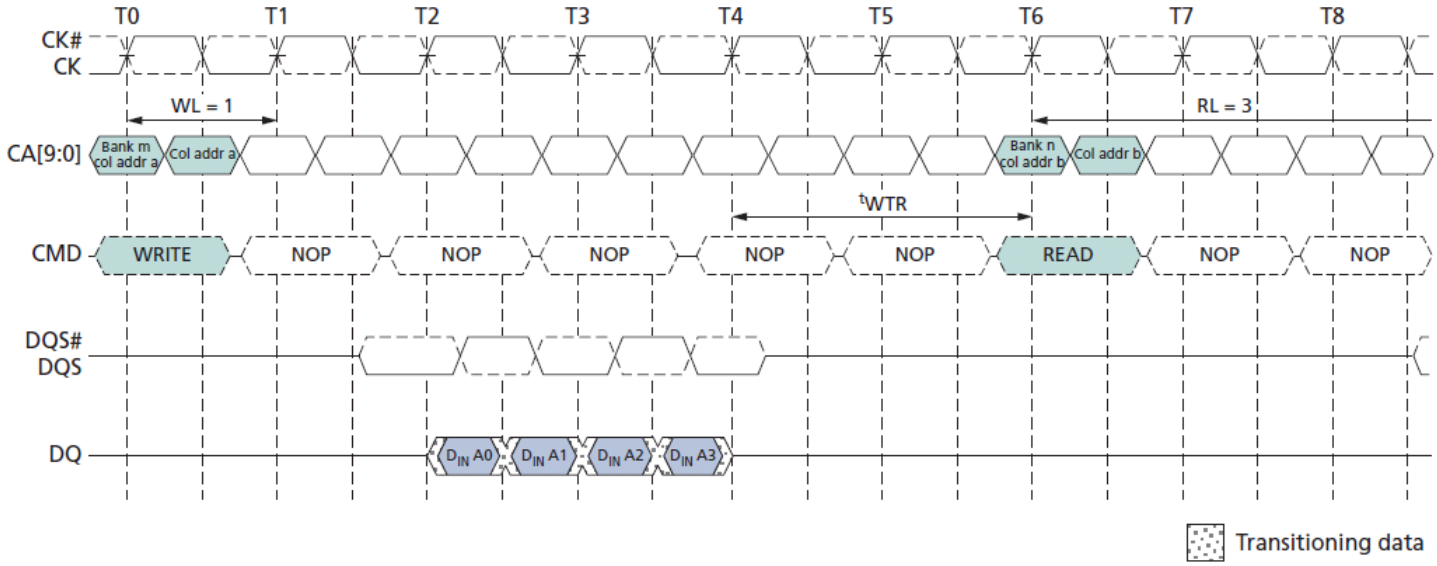


Figure 16: Burst WRITE Followed by Burst READ – RL = 3, WL = 1, BL = 4

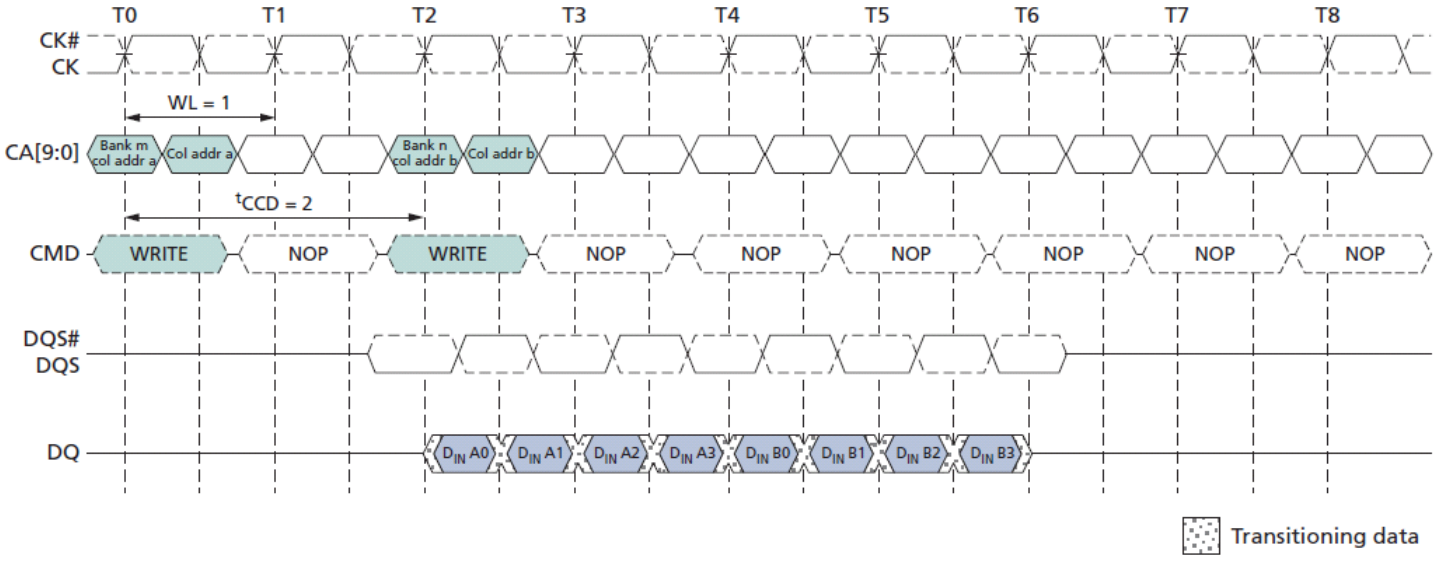


Notes : 1.The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(tWTR / tCK)].

2. tWTR starts at the rising edge of the clock after the last valid input data.

3. If a WRITE burst is truncated with a BST command, the effective burst length of the truncated WRITE burst should be used as BL to calculate the minimum WRITE-to-READ delay.

Figure 17 : Seamless Burst WRITE – WL = 1, BL = 4, tCCD = 2



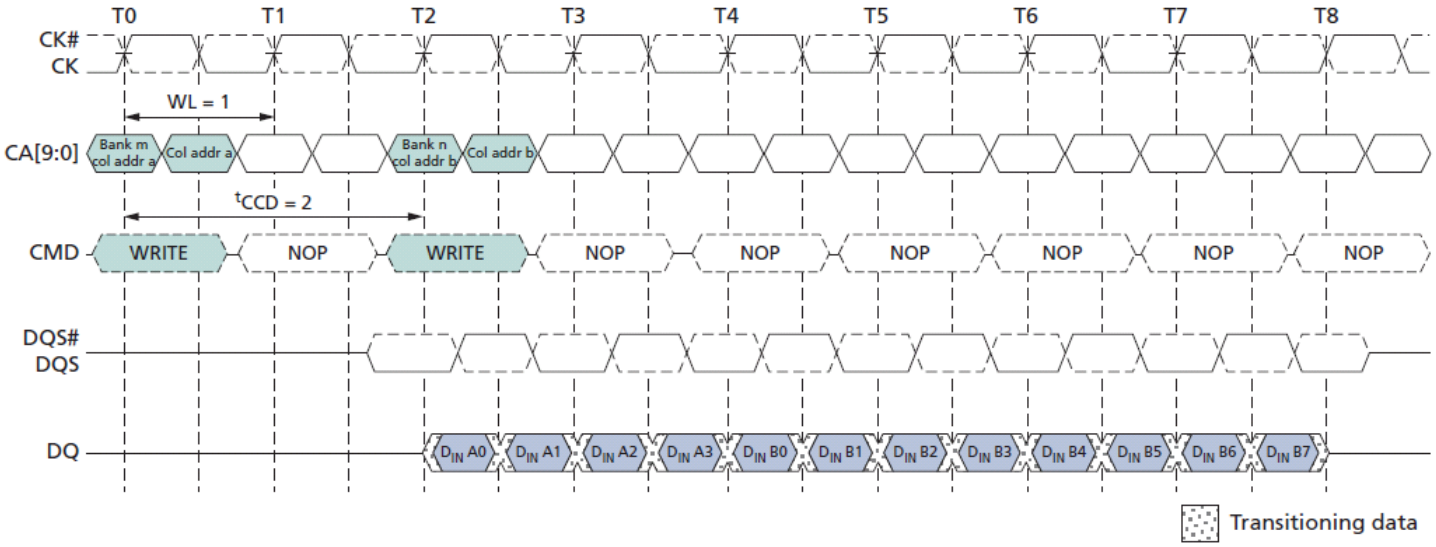
Note : 1. The seamless burst WRITE operation is supported by enabling a WRITE command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation.
This operation is supported for any activated bank.

WRITEs Interrupted by a WRITE

A burstWRITE can only be interrupted by anotherWRITE with a 4-bit burst boundary, provided that tCCD (MIN) is met.

AWRITE burst interrupt can occur on even clock cycles after the initial WRITE command, provided that tCCD (MIN) is met.

Figure 18: WRITE Burst Interrupt Timing – WL = 1, BL = 8, tCCD = 2



Notes : 1. WRITEs can only be interrupted by other WRITEs or the BST command.

2. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE.

BURST TERMINATE Command

The BURSTTERMINATE (BST) command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can only be issued to terminate an active READ or WRITE burst.

Therefore, a BST command can only be issued up to and including BL/2 - 1 clock cycles after a READ or WRITE command.

The effective burst length of a READ or WRITE command truncated by a BST command is as follows :

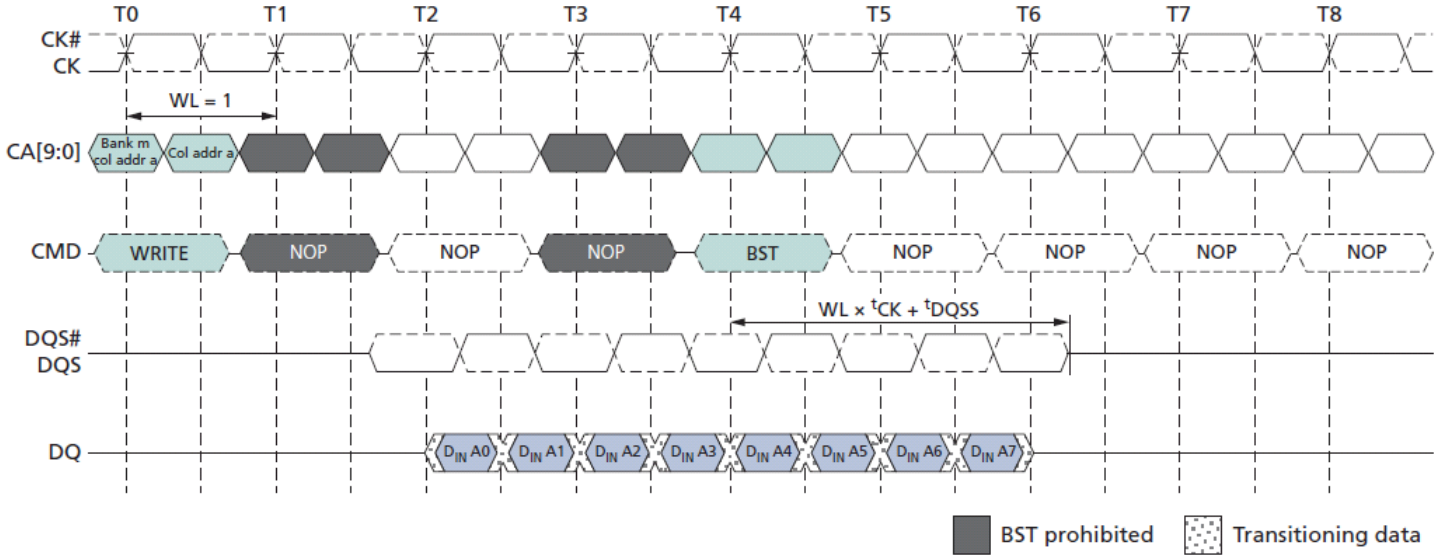
- Effective burst length = 2 × (number of clock cycles from the READ or WRITE command to the BST command).
- If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for BL when calculating the minimum READ-to-WRITE or WRITE-to-READ delay.
- The BST command only affects the most recent READ or WRITE command.

  The BST command truncates an ongoing READ burst RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock where the BST command is issued.

  The BST command truncates an on going WRITE burst WL X tCK + tDQSS after the rising edge of the clock where the BST command is issued.
- The 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command.

  The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of four.

Figure 19 : Burst WRITE Truncated by BST – WL = 1, BL = 16

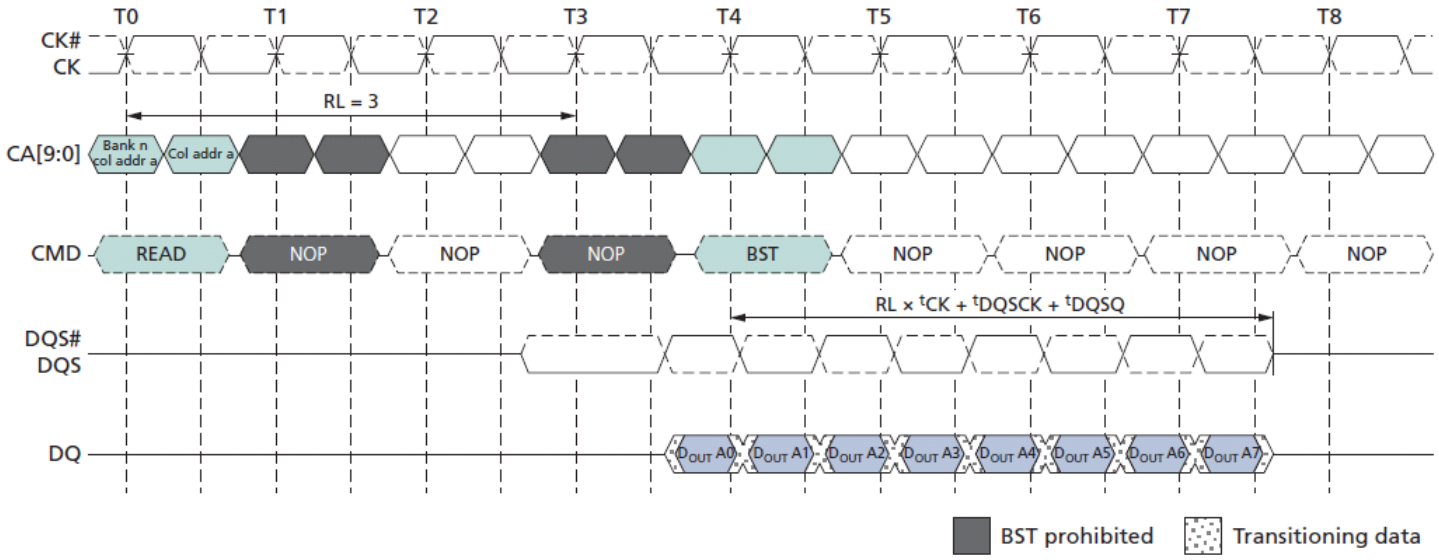


Notes : 1. The BST command truncates an ongoing WRITE burst WL × tCK + tDQSS after the rising edge of the clock where the BST command is issued.

2. BST can only be issued an even number of clock cycles after the WRITE command.

3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.

Figure 20: Burst READ Truncated by BST – RL = 3, BL = 16



Notes : 1. The BST command truncates an ongoing READ burst (RL × tCK + tDQSCK + tDQSQ) after the rising edge of the clock where the BST command is issued.

2. BST can only be issued an even number of clock cycles after the READ command.

3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.

Write Data Mask

On LPDDR2 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. ata mask timings match data bit timing, but are inputs only. Internal data mask loading is identical to data bit loading to ensure matched system timing.

Figure 21: Data Mask Timing

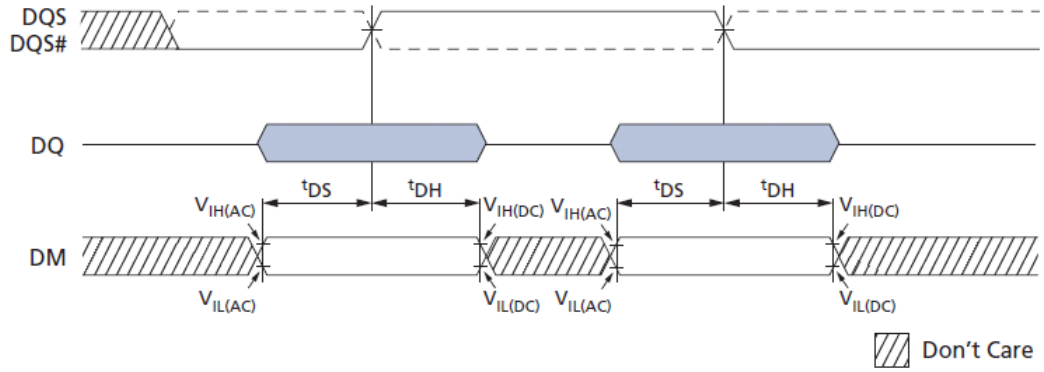
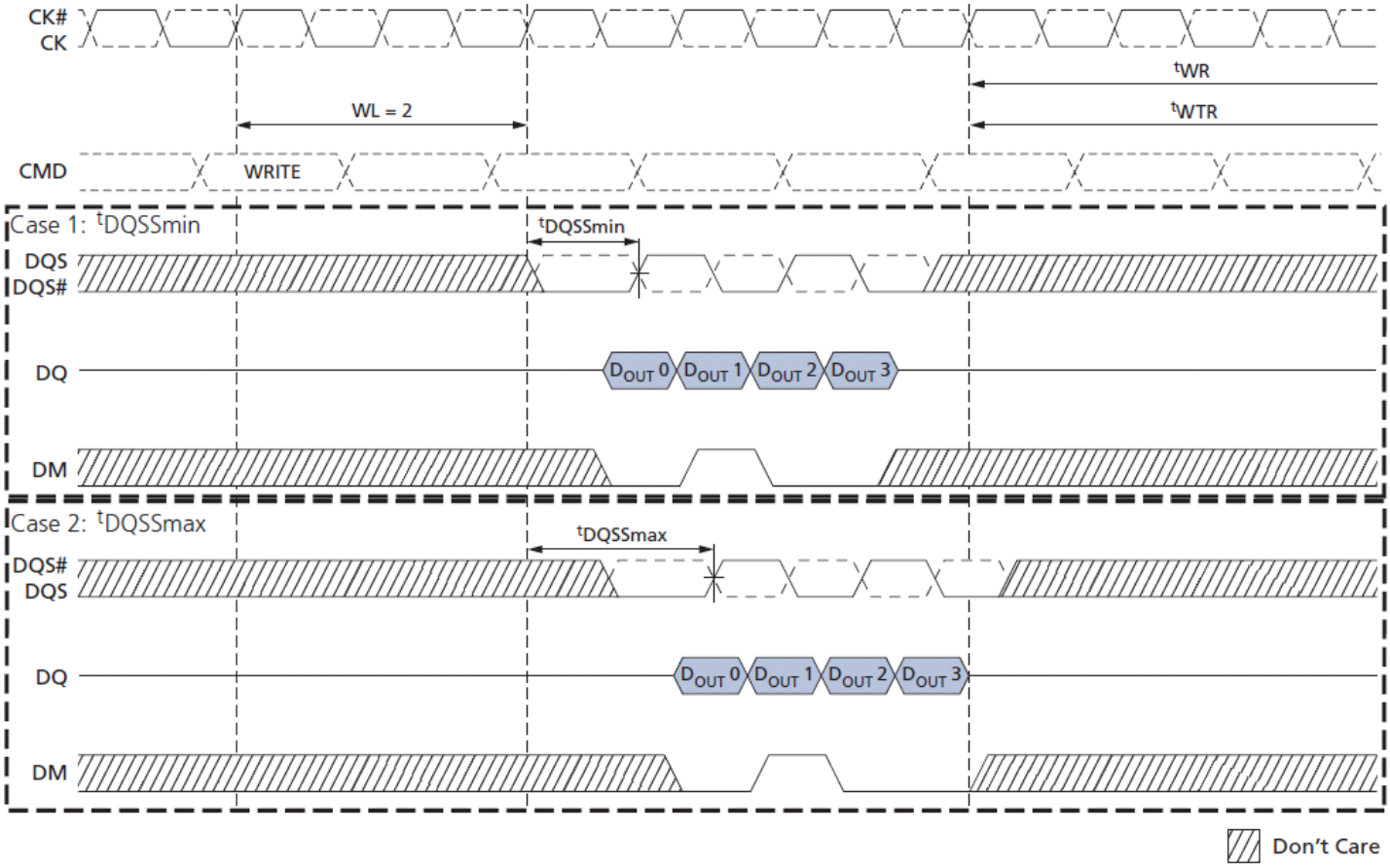


Figure 22: Write Data Mask – Second Data Bit Masked



Note : 1. For the data mask function, WL = 2, BL = 4 is shown; the second data bit is masked.

PRECHARGE Command

The PRECHARGE command is used to precharge or close a bank that has been activated.

The PRECHARGE command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag and bank address bits BA0 and BA1 are used to determine which bank(s) to precharge.

For 8-bank devices, the AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge.

The precharged bank(s) will be available for subsequent row access tRPab after an all bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

To ensure that 8-bank devices can meet the instantaneous current demand required to operate, the row precharge time (tRP) for an all bank PRECHARGE in 8-bank devices (tRPab) will be longer than the row precharge time for a single-bank PRECHARGE (tRPpb).

ACTIVATE to PRECHARGE timing is shown in ACTIVATE Command (page 17).

Table 22: Bank Selection for PRECHARGE by Address Bits

AB(CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 8-Bank Device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don't Care	Don't Care	Don't Care	All Banks

READ Burst Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command.

A new bank ACTIVATE command can be issued to the same bank after the row precharge time (tRP) has elapsed.

A PRECHARGE command cannot be issued until after tRAS is satisfied.

The minimum READ-to-PRECHARGE time (tRTP) must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ command. tRTP begins BL/2 - 2 clock cycles after the READ command.

If the burst is truncated by a BST command, the effective BL value is used to calculate when tRTP begins.

Figure 23: READ Burst Followed by PRECHARGE – RL = 3, BL = 8, RU(tRTP(MIN)/tCK) = 2

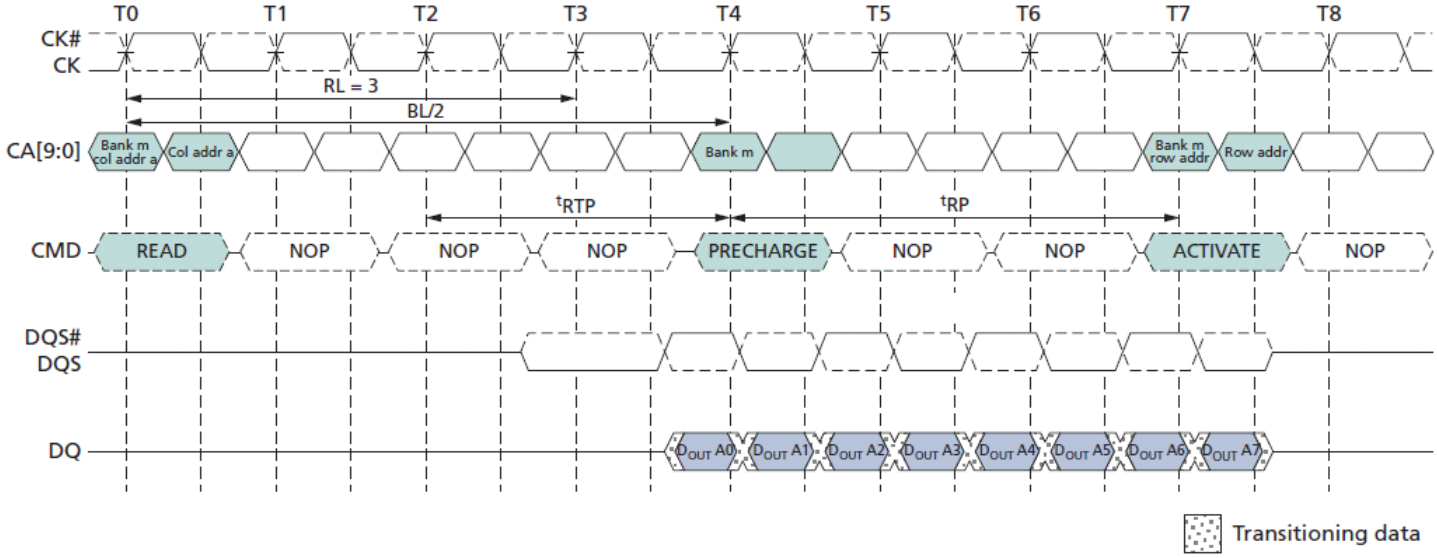
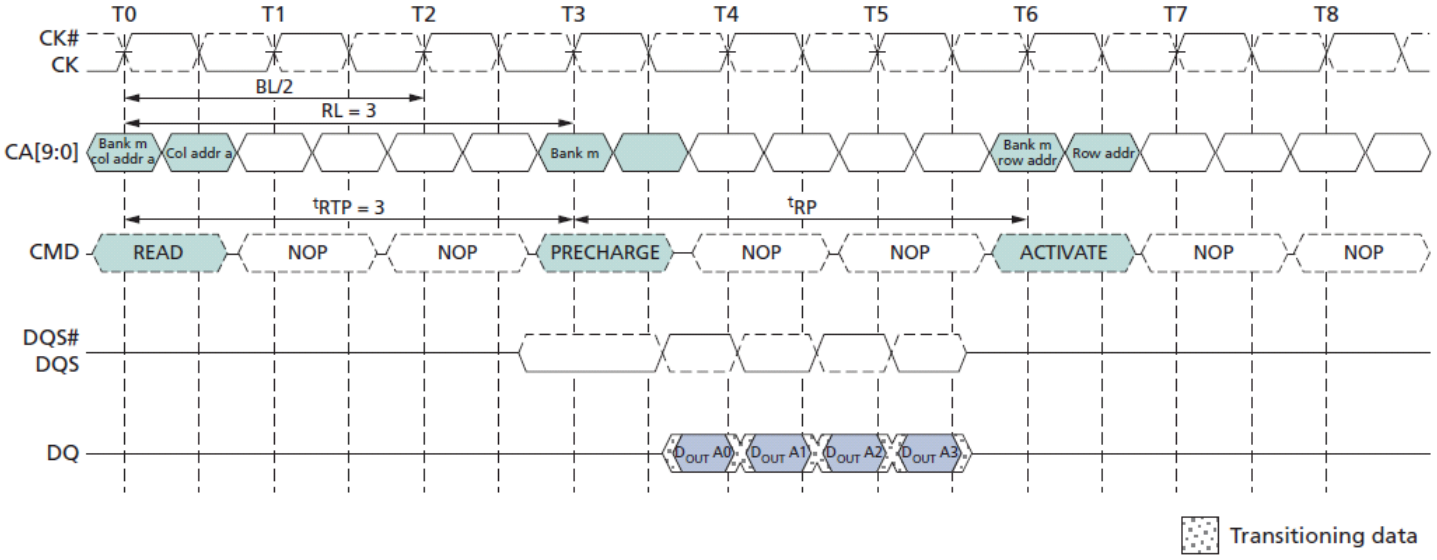


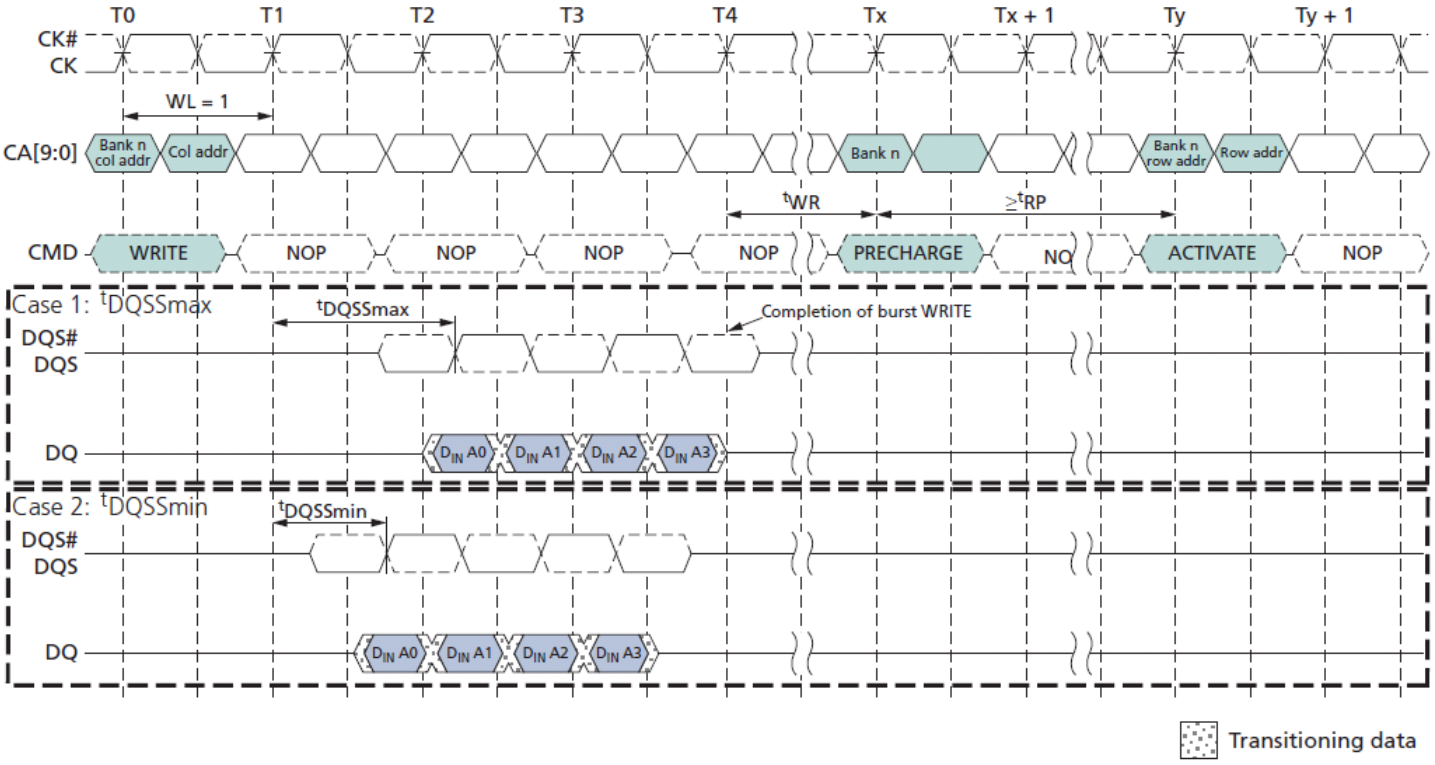
Figure 24: READ Burst Followed by PRECHARGE – RL = 3, BL = 4, RU(tRTP(MIN)/tCK) = 3



WRITE Burst Followed by PRECHARGE

For WRITE cycles, aWRITE recovery time (tWR) must be provided before a PRECHARGE command can be issued. tWR delay is referenced from the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the tWR delay. For WRITE-to-PRECHARGE timings see Table 23. These devices write data to the array in prefetch quadruples (prefetch = 4). An internal WRITE operation can only begin after a prefetch group has been completely latched. The minimumWRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For untruncated bursts, BL is the value set in the mode register. For truncated bursts, BL is the effective burst length.

Figure 25 : WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4



Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function.When a READ or WRITE command is issued to the device, the auto precharge bit (AP) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

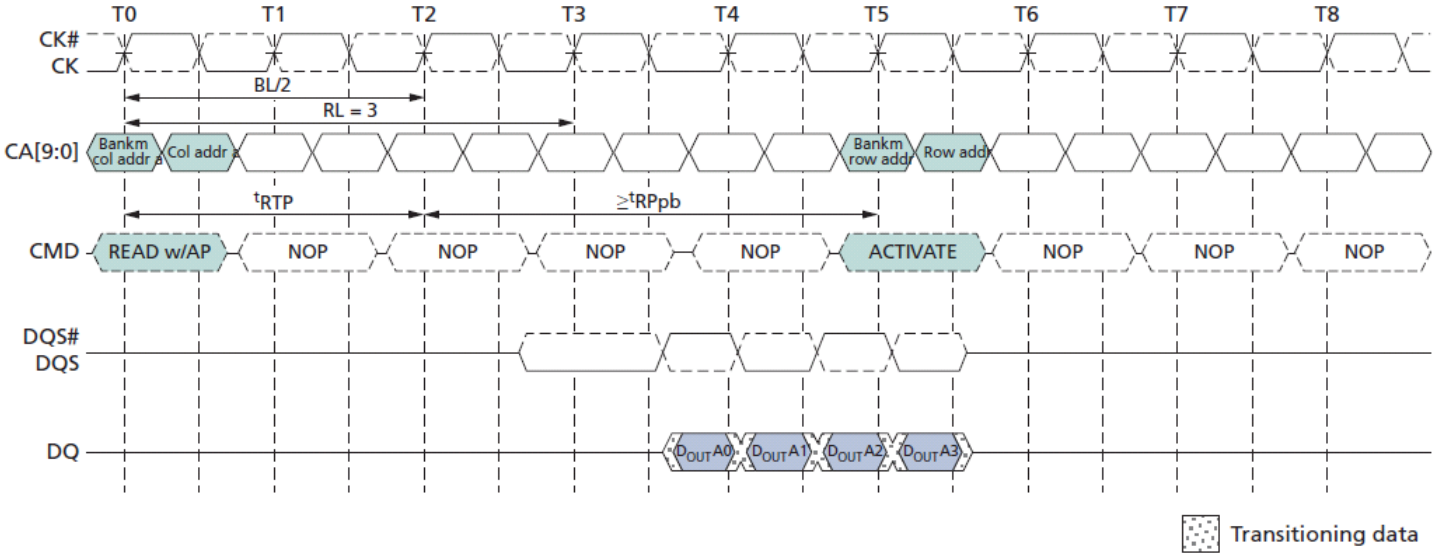
READ Burst with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged.

These devices start an auto precharge on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the READ with auto precharge command, whichever is greater. For auto precharge calculations see Table 23 . Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Figure 26 : READ Burst with Auto Precharge – RL = 3, BL = 4, RU(tRTP(MIN)/tCK) = 2



WRITE Burst with Auto Precharge

If AP (CA0f) is HIGH when aWRITE command is issued, theWRITE with auto precharge function is engaged.

The device starts an auto precharge at the clock rising edge tWR cycles after the completion of the burst WRITE. Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Figure 27 : Write Burst with Auto Precharge – WL=1, BL=4

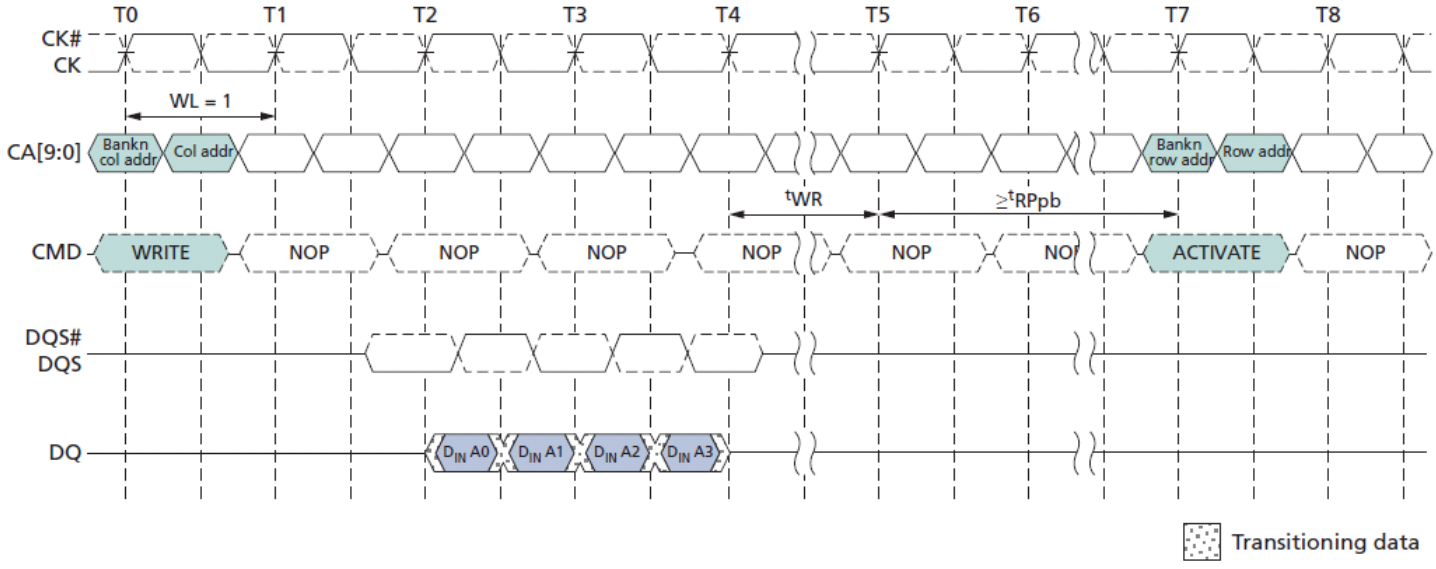


Table23 : Precharge and Auto Precharge Clarification

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
READ	Precharge to same bank as read	BL/2 + MAX(2, RU(tRTP/tCK)) - 2	CLK	1
	Precharge all	BL/2 + MAX(2, RU(tRTP/tCK)) - 2	CLK	1
BST	Precharge to same bank as read	1	CLK	1
	Precharge all	1	CLK	1
READ w/AP	Precharge to same bank as read w/AP	BL/2 + MAX(2, RU(tRTP/tCK)) - 2	CLK	1, 2
	Precharge all	BL/2 + MAX(2, RU(tRTP/tCK)) - 2	CLK	1
	Activate to same bank as read w/AP	BL/2 + MAX(2, RU(tRTP/tCK)) - 2 + RU(tRPpb/tCK)	CLK	1
	Write or WRITE w/AP (same bank)	Illegal	CLK	3
	Write or WRITE w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	CLK	3
	Read or read w/AP (same bank)	Illegal	CLK	3
	Write or WRITE w/AP (different bank)	BL/2	CLK	3
WRITE	Precharge to same bank as write	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
	Precharge all	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
BST	Precharge to same bank as write	WL + RU(tWR/tCK) + 1	CLK	1
	Precharge all	WL + RU(tWR/tCK) + 1	CLK	1
WRITE w/AP	Precharge to same bank as WRITE w/AP	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1, 2
	Precharge all	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
	Activate to same bank as write w/AP	WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRPpb/tCK)	CLK	1
	Write or WRITE w/ap (same bank)	Illegal	CLK	3
	Write or WRITE w/ap (different bank)	BL/2	CLK	3
	Read or read w/ap (same bank)	Illegal	CLK	3
	Read or read w/ap (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	CLK	3
Precharge	Precharge to same bank as precharge	1	CLK	1
	Precharge all	1	CLK	1
Precharge all	Precharge	1	CLK	1
	Precharge all	1	CLK	1

Notes : 1. For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command either a one-bank RECHARGE or PRECHARGE ALL issued to that bank.
The PRECHARGE period is satisfied after tRP, depending on the latest PRECHARGE command issued to that bank.

2. Any command issued during the specified minimum delay time is illegal.
3. After READ with auto precharge, seamless READ operations to different banks are supported. After WRITE with auto precharge, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge must not be interrupted or truncated.

REFRESH Command

The REFRESH command is initiated with CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock. Per-bank REFRESH is only supported in devices with eight banks.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device.The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin :

0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh.

Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command (see Table 22). A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command. The REFpb command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied after the prior REFab command.
- tRFCpb has been satisfied after the prior REFpb command.
- tRP has been satisfied after the prior PRECHARGE command to that bank .
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks within the device are accessible and can be addressed during the cycle.

During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command.
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank.
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank.
- tRFCpb must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks.

All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command.
- tRFCpb has been satisfied following the prior REFpb command.
- tRP has been satisfied following the prior PRECHARGE commands.

After an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an ACTIVATE command.
- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Table24 : Refresh Command Scheduling Separation Requirements

Symbol	Minimum delay From	To	Notes
tRFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	
tRRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note : 1. A bank must be in the idle state before it is refreshed, so REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

Mobile LPDDR2 devices provide significant flexibility in scheduling REFRESH commands as long as the required boundary conditions are met (see Figure 32).

In the most straightforward implementations, a REFRESH command should be scheduled every tREFI. In this case, self refresh can be entered at any time. Users may choose to deviate from this regular refresh pattern, for instance, to enable a period in which no refresh is required. As an example, using a 1Gb LPDDR2 device, the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by tREFBW), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows :

tREFW - (R/8) × tREFBW = tREFW - R × 4 × tRFCab.

For example, a 1Gb device atTC ≤ 85˚C can be operated without a refresh for up to 32ms - 4096 × 4 × 130ns ≈ 30ms.

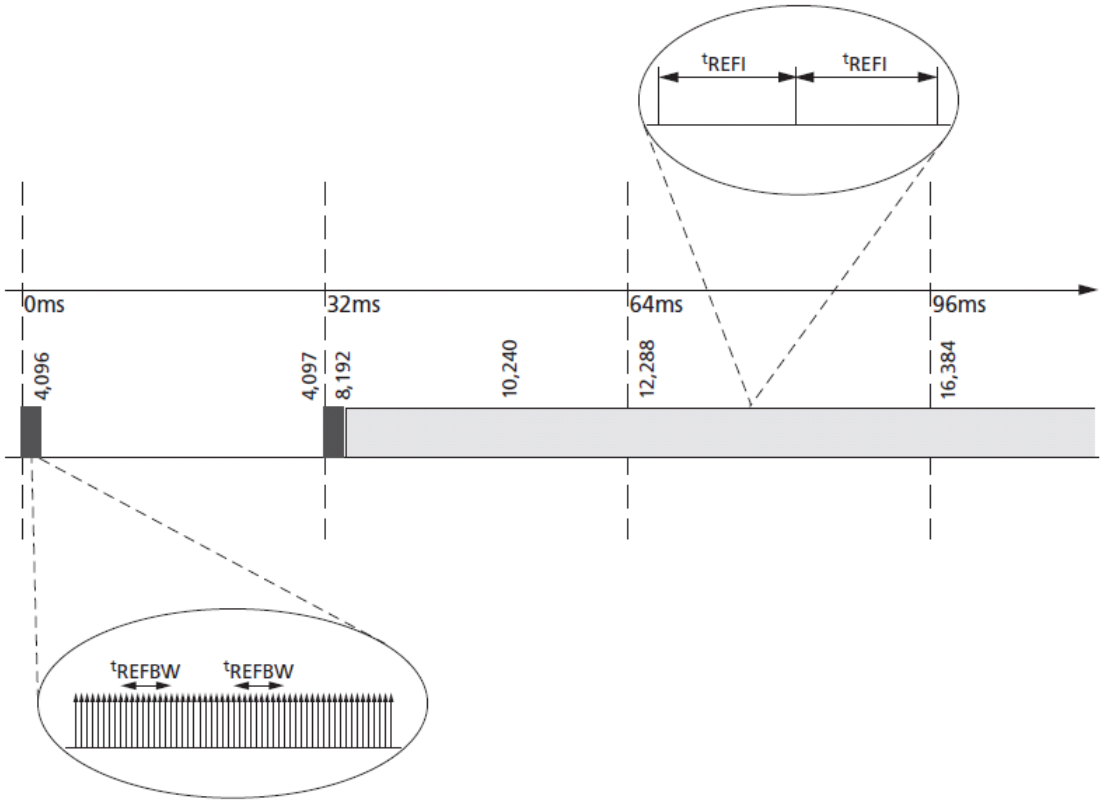
Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in *every* rolling refresh window during refresh pattern transitions.

The supported transition from a burst pattern to a regular distributed pattern is shown in Figure 28. If this transition occurs immediately after the burst refresh phase, all rolling tREFW intervals will meet the minimum required number of REFRESH commands.

A nonsupported transition is shown in Figure 55. In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling tREFW intervals, the minimum number of REFRESH commands is not satisfied.

Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed refresh pattern must be assumed. Fidelix recommends entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase (see Figure 31).

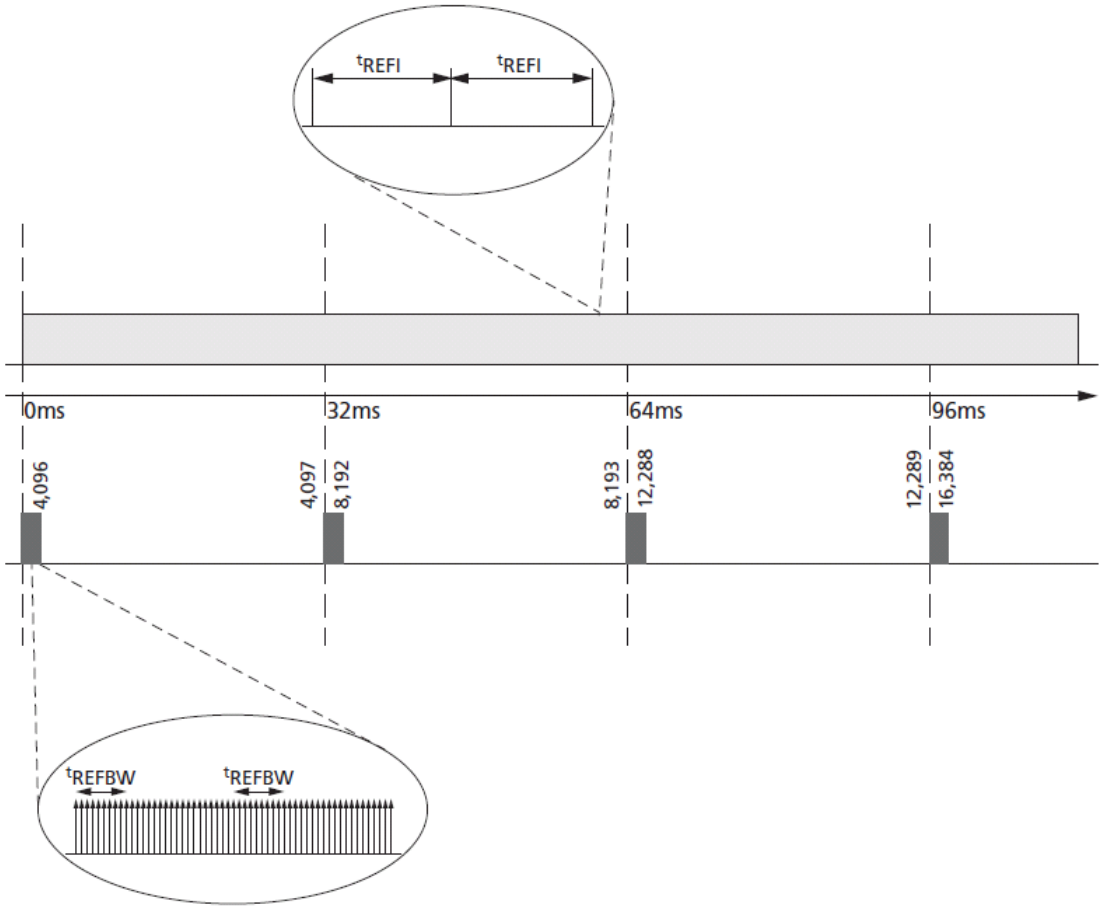
Figure28 : Regular Distributed Refresh Pattern



Notes : 1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.

2. As an example, in a 1Gb LPDDR2 device at TC ≤ 85˚C, the distributed refresh pattern has one REFRESH command per 7.8μs; the burst refresh pattern has one REFRESH command per 0.52μs, followed by ≈ 30ms without any REFRESH command.

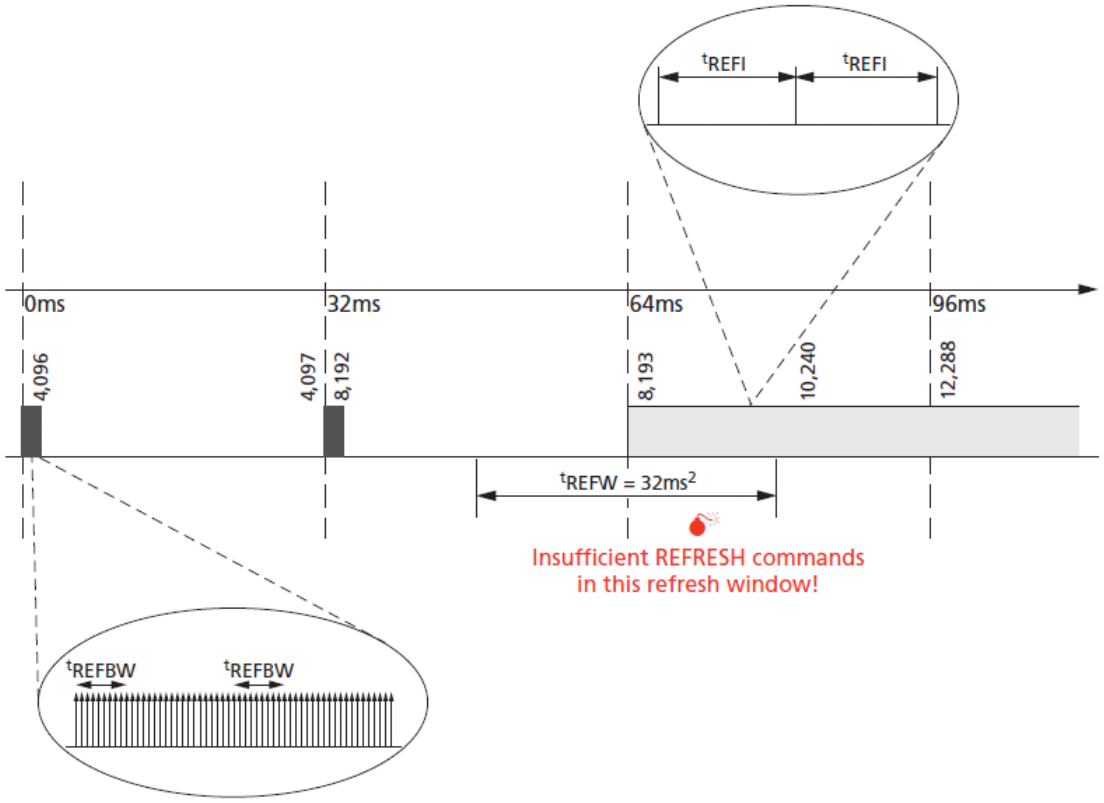
Figure29 : Supported Transition from Repetitive REFRESH Burst



Notes : 1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.

2. As an example, in a 1Gb LPDDR2 device at TC ≤ 85˚C, the distributed refresh pattern has one REFRESH command per 7.8μs; the burst refresh pattern has one REFRESH command per 0.52μs, followed by ≈ 30ms without any REFRESH command.

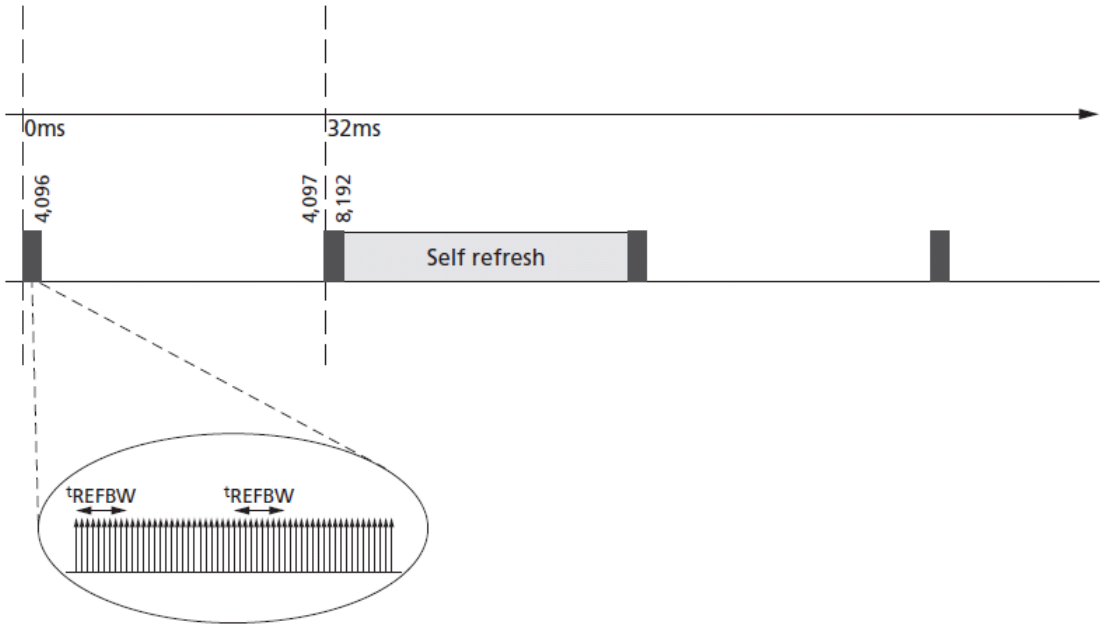
Figure30 : Nonsupported Transition from Repetitive REFRESH Burst



Notes : 1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.

2. There are only ≈ 2048 REFRESH commands in the indicated tREFW window. This does not provide the required minimum number of REFRESH commands (R). PDF:

Figure31 : Recommended Self Refresh Entry and Exit



Note : 1. In conjunction with a burst/pause refresh pattern.

REFRESH Requirements

1. Minimum Number of REFRESH Commands

Mobile LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (tREFW = 32 ms @ MR4[2:0] = 011 orTC ≤ 85˚C). For actual values per density and the resulting average refresh interval (tREFI), (see Table 75).

For tREFW and tREFI refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) table.

For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

2. Burst REFRESH Limitation

To limit current consumption, a maximum of eight REFab commands can be issued in any rolling tREFBW (tREFBW = 4 × 8 × tRFCab). This condition does not apply if REFpb commands are used.

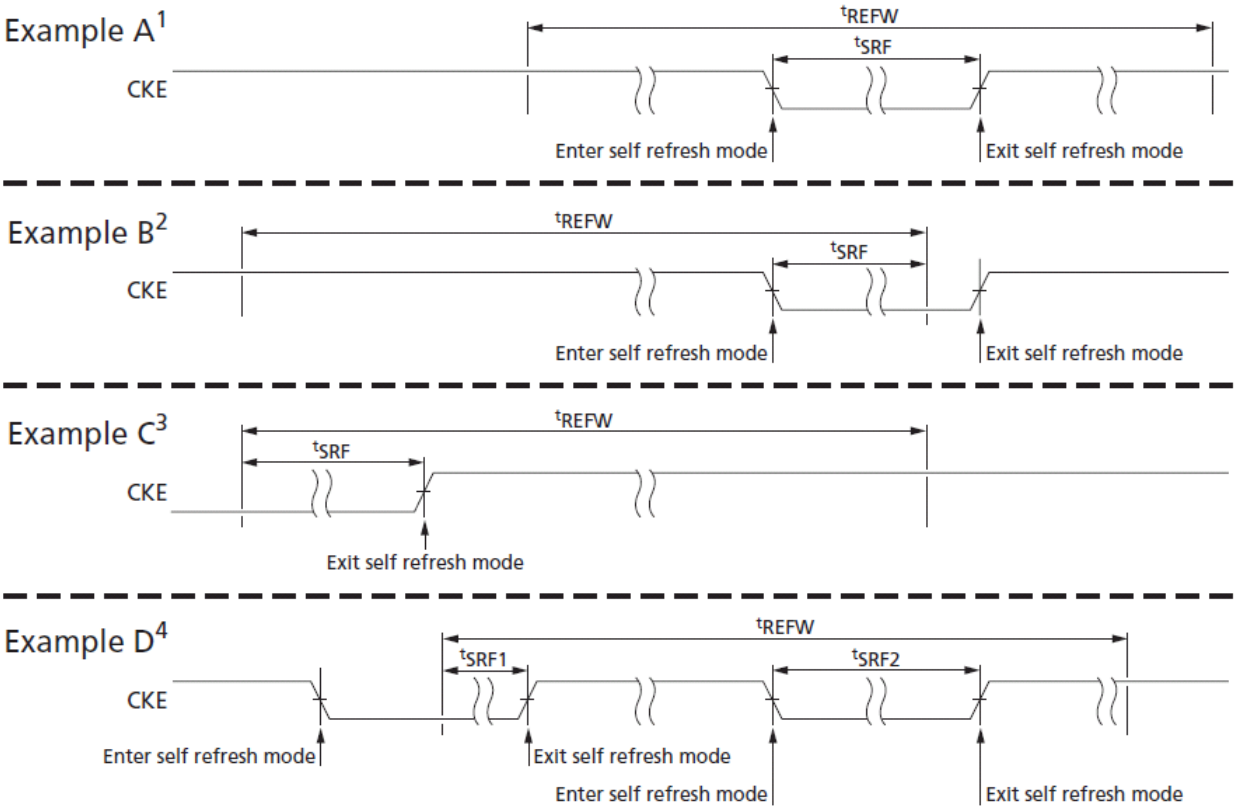
3. REFRESH Requirements and Self Refresh

If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in that window is reduced to the following:

$$R' = RU\left(\frac{tSRF}{tREFI}\right) = R - RU\left(R \times \frac{tSRF}{tREFW}\right)$$

Where RU represents theround-up function.

Figure 32: tSRF Definition



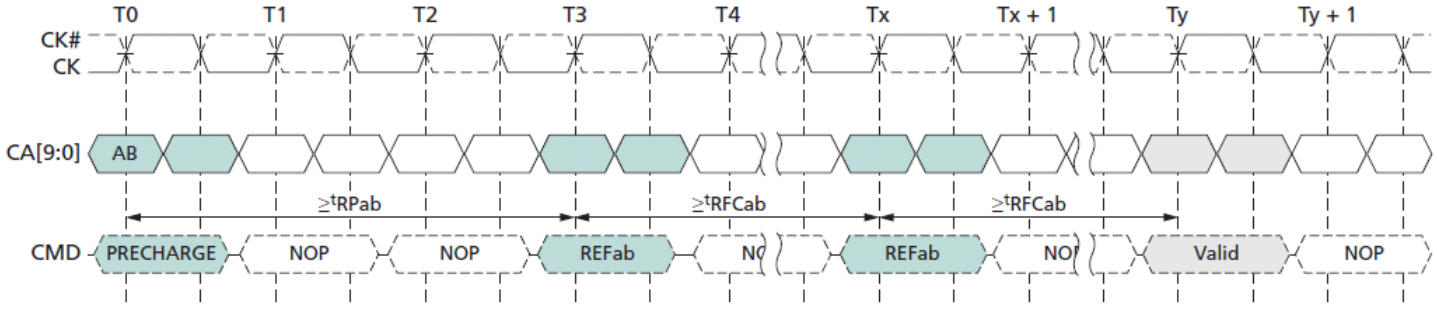
Notes : 1. Time in self refresh mode is fully enclosed in the refresh window (tREFW).

2. At self refresh entry.

3. At self refresh exit.

4. Several intervals in self refresh during one tREFW interval. In this example, tSRF = tSRF1 + tSRF2.

Figure 33 All-Bank REFRESH Operation



Notes : 1. Prior to T0, the REFpb bank counter points to bank 0.

2. Operations to banks other than the bank being refreshed are supported during the tRFCpb period.

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is executed by taking CKE LOW, CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock.

CKE must be HIGH during the clock cycle preceding a SELF REFRESH command. A NOP command must be driven in the clock cycle following the SELF REFRESH command. After the power-down command is registered, CKE must be held LOW to keep the device in self refresh mode.

Mobile LPDDR2 devices can operate in self refresh mode in both the standard and extended temperature ranges. These devices also manage self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range. See Table 59 for details.

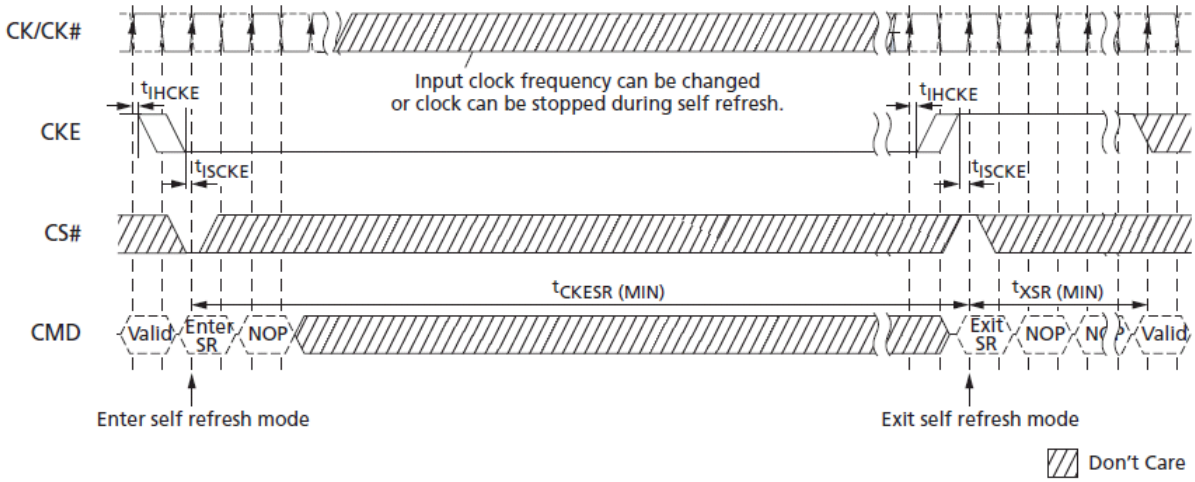
After the device has entered self refresh mode, all external signals other than CKE are “Don’t Care.” For proper self refresh operation, power supply pins (VDD1, VDD2, VDDQ, and VDDCA) must be at valid levels. VDDQ can be turned off during self refresh. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting self refresh, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges (see the Single-Ended AC and DC Input Levels for DQ and DM table). VREFDQ can be at any level between 0 and VDDQ; VREFCA can be at any level between 0 and VDDCA during self refresh.

Before exiting self refresh, VREFDQ and VREFCA must be within specified limits (see AC and DC Logic Input Measurement Levels for Single-Ended Signals (page 78)). After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during tCKESR. The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least tCKESR. The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.

Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval (tXSR), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout tXSR, except during self refresh re-entry. NOP commands must be registered on each rising clock edge during tXSR.

Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command or eight per-bank commands) must be issued before issuing a subsequent SELF REFRESH command.

Figure 35: SELF REFRESH Operation



Notes : 1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of two cycles of stable clocks are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.

2. The device must be in the all banks idle state prior to entering self refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command can be issued only after tXSR is satisfied. NOPs must be issued during tXSR.

Partial-Array Self Refresh – Bank Masking

Devices in densities of 64Mb–512Mb are comprised of four banks; densities of 1Gb and higher are comprised of eight banks. Each bank can be configured independently whether or not a SELF REFRESH operation will occur in that bank. One 8-bit mode register (accessible via the MRW command) is assigned to program the bank-masking status of each bank up to eight banks.
For bank masking bit assignments, see the MR16 PASR Bank Mask (MA[7:0] = 010h) and MR16 Op-Code Bit Definitions tables.

The mask bit to the bank enables or disables a refresh operation of the entire memory space within the bank.
If a bank is masked using the bank mask register, a REFRESH operation to the entire bank is blocked and bank data retention is not guaranteed in self refresh mode.To enable a REFRESH operation to a bank, the corresponding bank mask bit must be programmed as “unmasked.”When a bank mask bit is unmasked, the array space being refreshed within that bank is determined by the programmed status of the segment mask bits.

Partial-Array Self Refresh – Segment Masking

Programming segment mask bits is similar to programming bank mask bits. For densities 1Gb and higher, eight segments are used for masking (see the MR17 PASR Segment Mask (MA[7:0] = 011h) and MR17 PASR Segment Mask Definitions tables). A mode register is used for programming segment mask bits up to eight bits. For densities less than 1Gb, segment masking is not supported.
When the mask bit to an address range (represented as a segment) is programmed as “masked,” a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled.
A segment masking scheme can be used in place of or in combination with a bank masking scheme. Each segment mask bit setting is applied across all banks. For segment masking bit assignments, see the tables noted above.

Table26 : Bank and Segment Masking Example

	Segment Mask(MR17)	Bank0	Bank1	Bank2	Bank3	Bank4	Bank5	Bank6	Bank7
Bank Mask(MR16)		0	1	0	0	0	0	0	1
Segment 0	0	-	M	-	-	-	-	-	M
Segment 1	0	-	M	-	-	-	-	-	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	-	M	-	-	-	-	-	M
Segment 4	0	-	M	-	-	-	-	-	M
Segment 5	0	-	M	-	-	-	-	-	M
Segment 6	0	-	M	-	-	-	-	-	M
Segment 7	1	M	M	M	M	M	M	M	M

Note : 1. This table provides values for an 8-bank device with REFRESH operations masked to banks 1 and 7, and segments 2 and 7.

MODE REGISTER READ

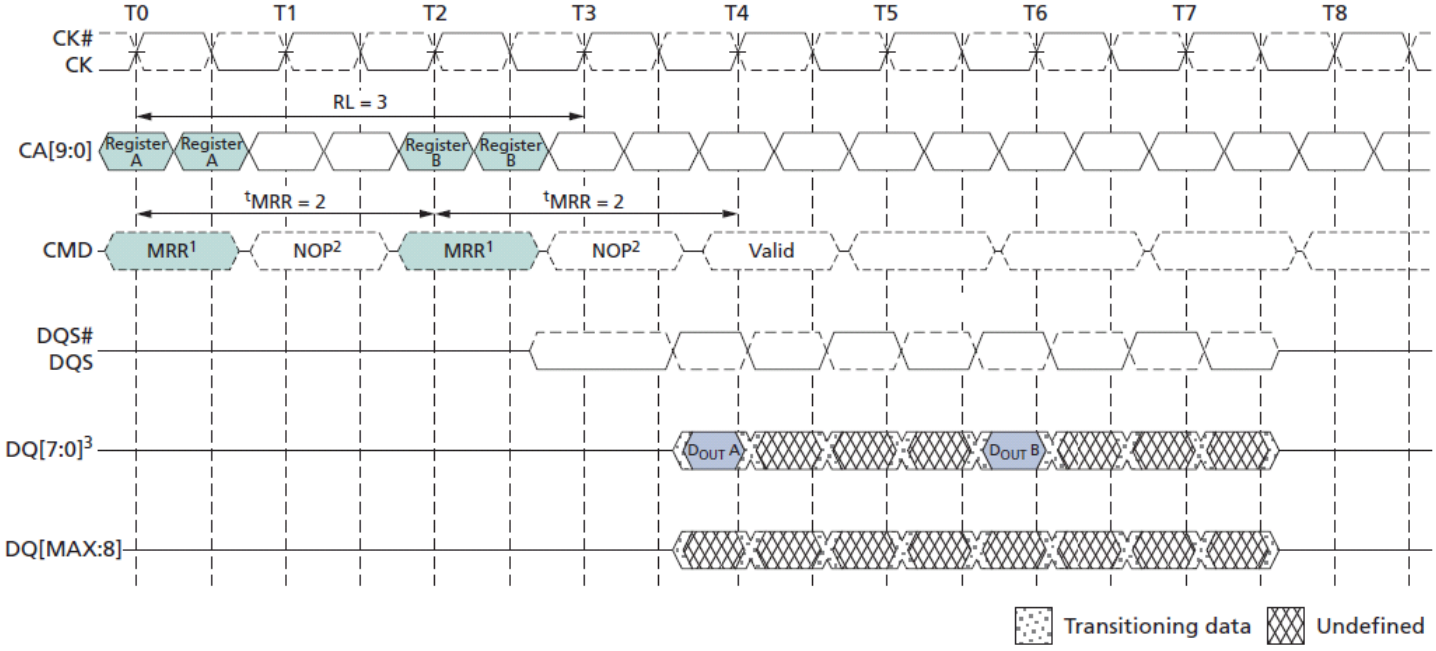
The MODE REGISTER READ (MRR) command is used to read configuration and status data from SDRAM mode registers.

The MRR command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock.

The mode register is selected by CA1f–CA0f and CA9r–CA4r.The mode register contents are available on the first data beat of DQ[7:0] after RL × tCK + tDQSCK + tDQSQ and following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in Table 28. All DQS are toggled for the duration of the mode register READ burst.

The MRR command has a burst length of four. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted.The MRR command period (tMRR) is two clock cycles.

Figure 36: MRR Timing – RL = 3, tMRR = 2

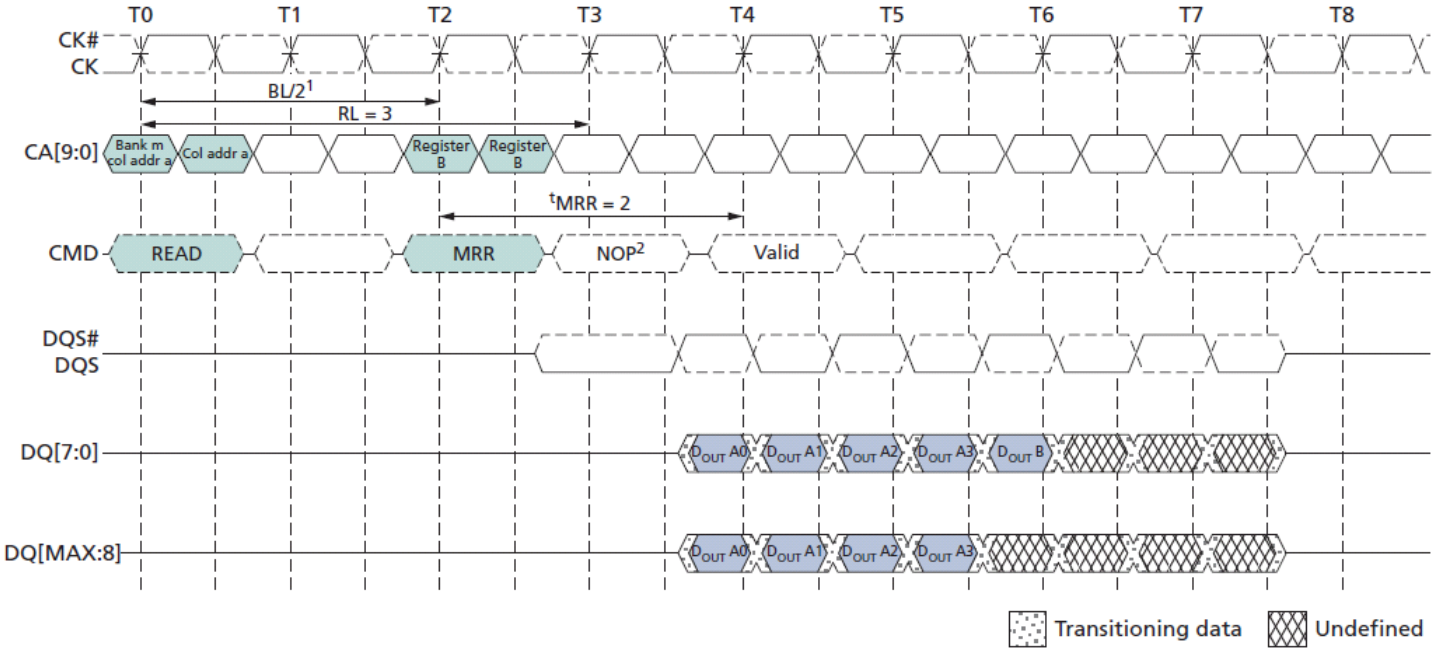


Notes : 1. MRRs to DQ calibration registers MR32 and MR40 are described in DQ Calibration (page 48).

Notes : 1. MRRs to DQ calibration registers MR32 and MR40 are described in DQ Calibration (page 48).
2. Only the NOP command is supported during tMRR.
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4. Minimum MRR to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
5. Minimum MRR to MRW latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 clock cycles.

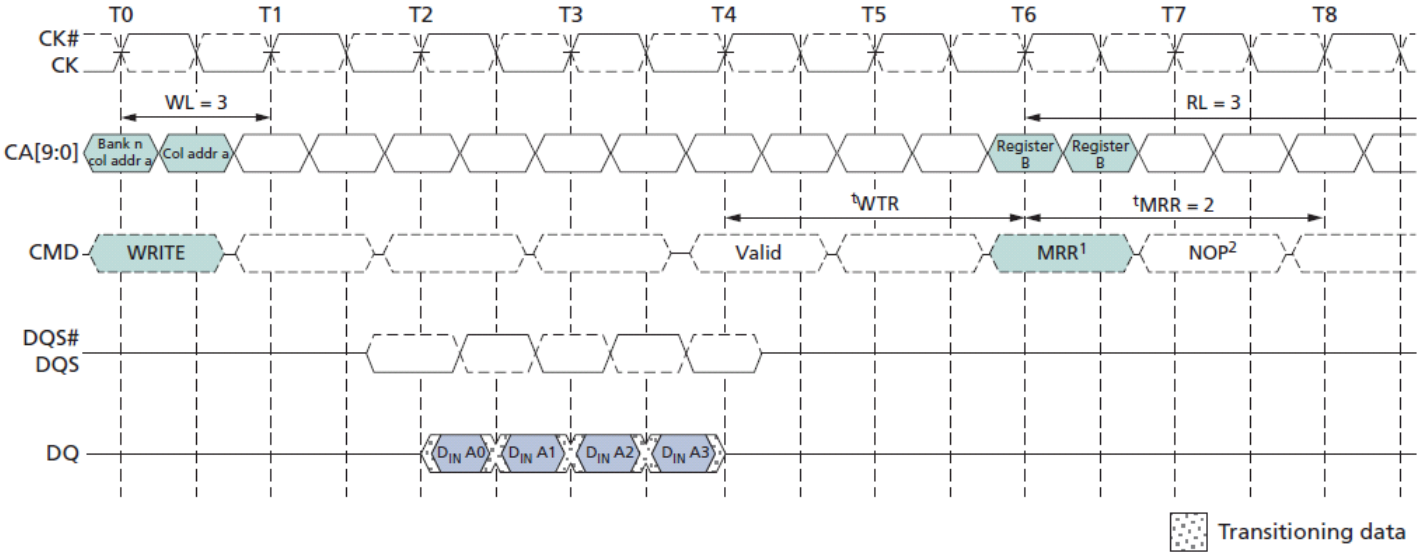
READ bursts andWRITE bursts cannot be truncated by MRR. Following a READ command, the MRR command must not be issued before BL/2 clock cycles have completed. Following A WRITE command, the MRR command must not be issued before WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles have completed. If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the BL value.

Figure 37: READ to MRR Timing – RL = 3, tMRR = 2



Notes : 1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Only the NOP command is supported during tMRR.

Figure 38: Burst WRITE Followed by MRR – RL = 3, WL = 1, BL = 4



Notes : 1. The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL+1+BL/2+ RU(tWTR/tCK)].
2. Only the NOP command is supported during tMRR.

Temperature Sensor

Mobile LPDDR2 devices feature a temperature sensor whose status can be read from MR4.

This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine whether operating temperature requirements are being met (see Operating Temperature Range table).

Temperature sensor data can be read from MR4 using the mode register read protocol. Upon exiting self-refresh or power-down, the device temperature status bits will be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges (see table noted above).

For example,TCASE could be above 85˚C when MR4[2:0] equals 011b. To ensure proper operation using the temperature sensor, applications must accommodate the parameters in the temperature sensor definitions table.

Table 27: Temperature Sensor Definitions and Operating Conditions

Parameter	Description	Symbol	Min/Max	Value	Unit
System Temperature Gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2˚C	TempGradient	MAX	System dependent	˚C/s
MR4 READ interval	Time period between MR4 READs from the System	ReadInterval	MAX	System dependent	ms
Temperature Sensor interval	Maximum delay between internal updates of MR4	tTSI	MAX	32	ms
System response delay	Maximum response time from an MR4 READ to the system response	SysRespDelay	MAX	System dependent	ms
Device temperature margin	Margin above maximum temperature to support controller response	TempMargin	MAX	2	˚C

Mobile LPDDR2 devices accommodate the temperature margin between the point at which the device temperature enters the extended temperature range and the point at which the controller reconfigures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system according to the following equation:

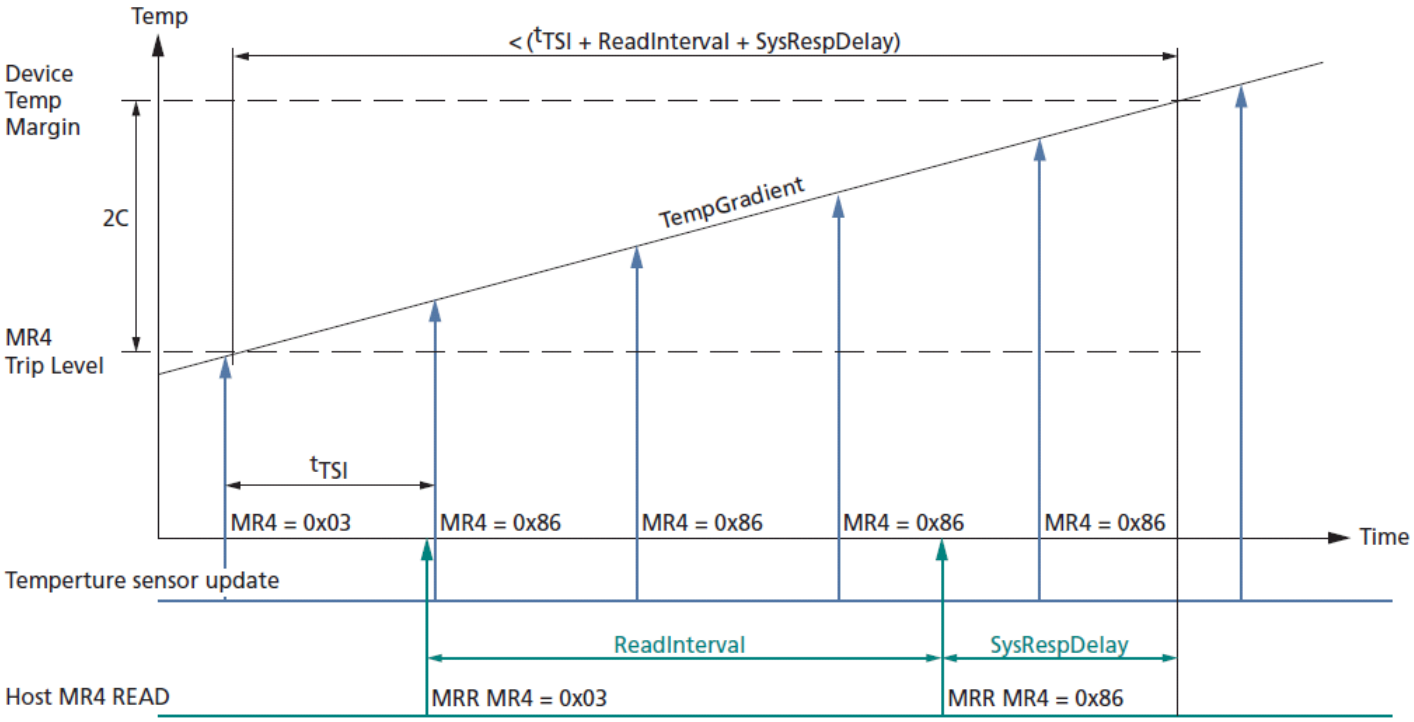
TempGradient × (ReadInterval + ^{t}TSI + SysRespDelay) ≤ 2°C

For example, ifTempGradient is 10˚C/s and the SysRespDelay is 1ms:

10°C/s X (ReadInterval + 32ms +1ms) ≤ 2°C

In this case, ReadInterval must not exceed 167ms.

Figure 39: Temperature Sensor Timing



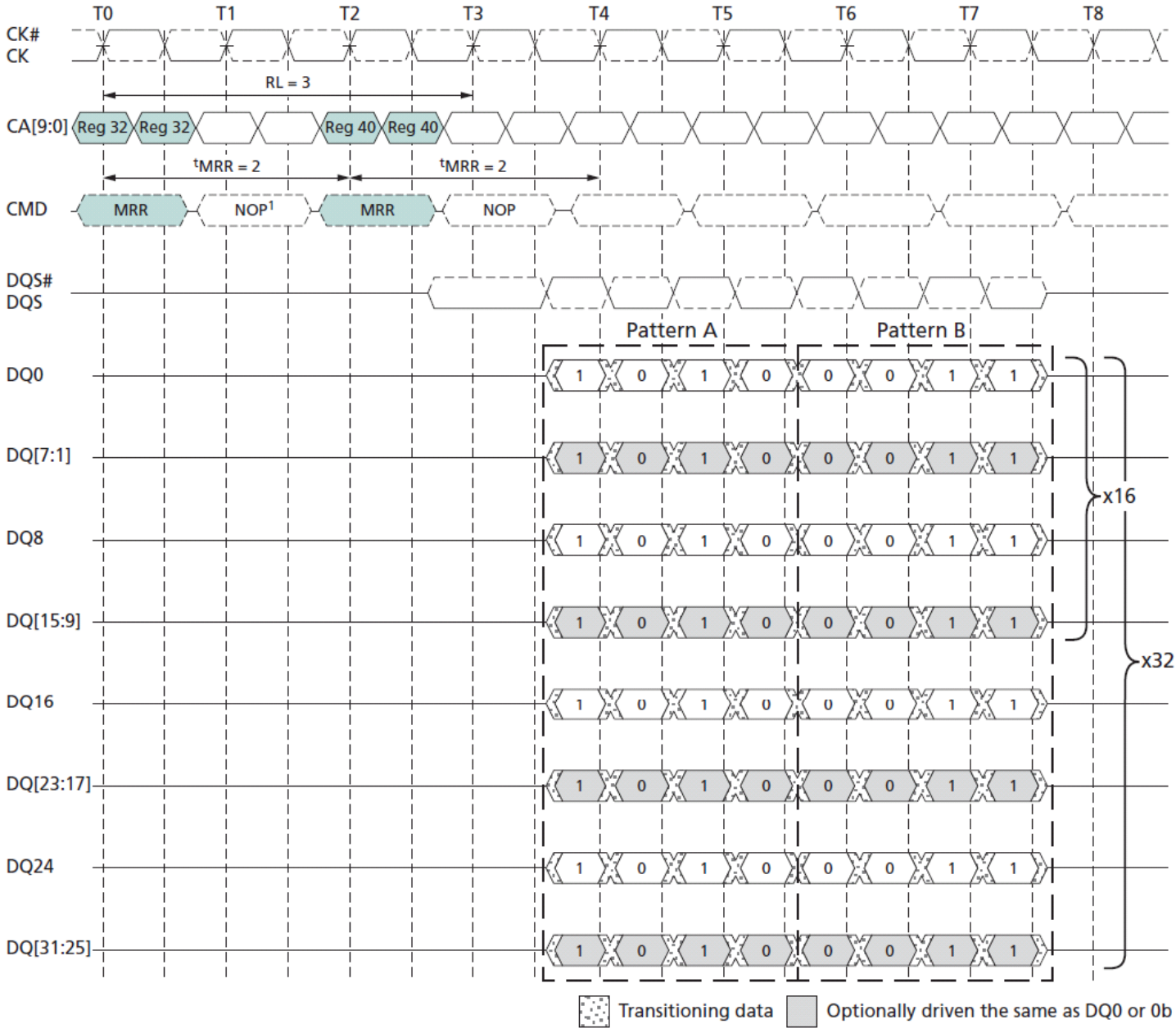
DQ Calibration

Mobile LPDDR2 devices feature a DQ calibration function that outputs one of two predefined system timing calibration patterns.

For x16 devices, pattern A (MRR to MRR32), and pattern B (MRR to MRR40), will return the specified pattern on DQ0 and DQ8; x32 devices return the specified pattern on DQ0, DQ8, DQ16, and DQ24.

For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.

Figure 40: MR32 and MR40 DQ Calibration Timing – RL = 3, tMRR = 2



Note : 1. Only the NOP command is supported during tMRR.

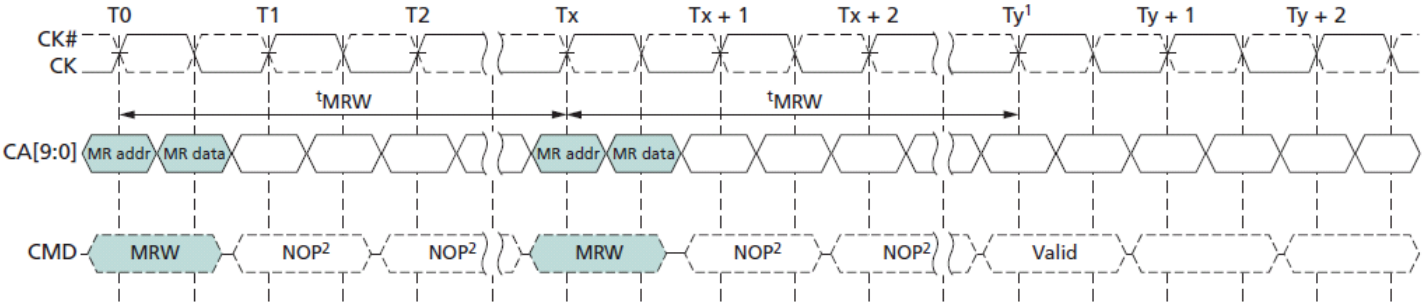
Table28 : Data Calibration Pattern Description

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Description
Pattern A	MR32	1	0	1	0	Reads to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	Reads to MR40 return DQ calibration pattern B

MODE REGISTER WRITE Command

The MODE REGISTERWRITE (MRW) command is used to write configuration data to the mode registers.
The MRW command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock.
The mode register is selected by CA1f–CA0f, CA9r–CA4r.The data to be written to the mode register is contained in CA9f–CA2f.
The MRW command period is defined by tMRW. MRWs to read-only registers have no impact on the functionality of the device.
MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE ALL command.

Figure 41: MODE REGISTER WRITE Timing – RL = 3, tMRW = 5



Notes : 1. At time Ty, the device is in the idle state.
2. Only the NOP command is supported during tMRW.

Table29 : Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
	MRW (RESET)	Resetting, device auto initialization	All banks idle
Bank(s) active	MRR	Reading mode register, bank(s) idle	Bank(s) active
	MRW	Not allowed	Not allowed
	MRW (RESET)	Not allowed	Not allowed

MRW RESET Command

The MRW RESET command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence (see 2. RESET Command under Power-Up (page 7)).
The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values.
Only the NOP command is supported during tINIT4.
After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command has completed. For MRW RESET timing, see Figure 1.

MRW ZQ Calibration Commands

The MRW command is used to initiate a ZQ calibration command that calibrates output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration.To achieve tighter tolerances, proper ZQ calibration must be performed.
There are four ZQ calibration commands and related timings: tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT is used for initialization calibration; tZQRESET is used for resetting ZQ to the default output impedance; tZQCL is used for long calibration(s); and tZQCS is used for short calibration(s). See the MR10 Calibration (MA[7:0] = 0Ah) table for ZQ calibration command code definitions.
ZQINIT must be performed for LPDDR2 devices. ZQINIT provides an output impedance accuracy of ±15%.
After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15%.
A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.
ZQRESET resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature.
This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.
One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within tZQCS for all speed bins, assuming the maximum sensitivities specified in Table 68 and Table 69 are met.The appropriate interval between ZQCS commands can be determined using these tables and system-specific parameters.
Mobile LPDDR2 devices are subject to temperature drift rate (Tdriftrate) and voltage drift rate (Vdriftrate) in various applications.
To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

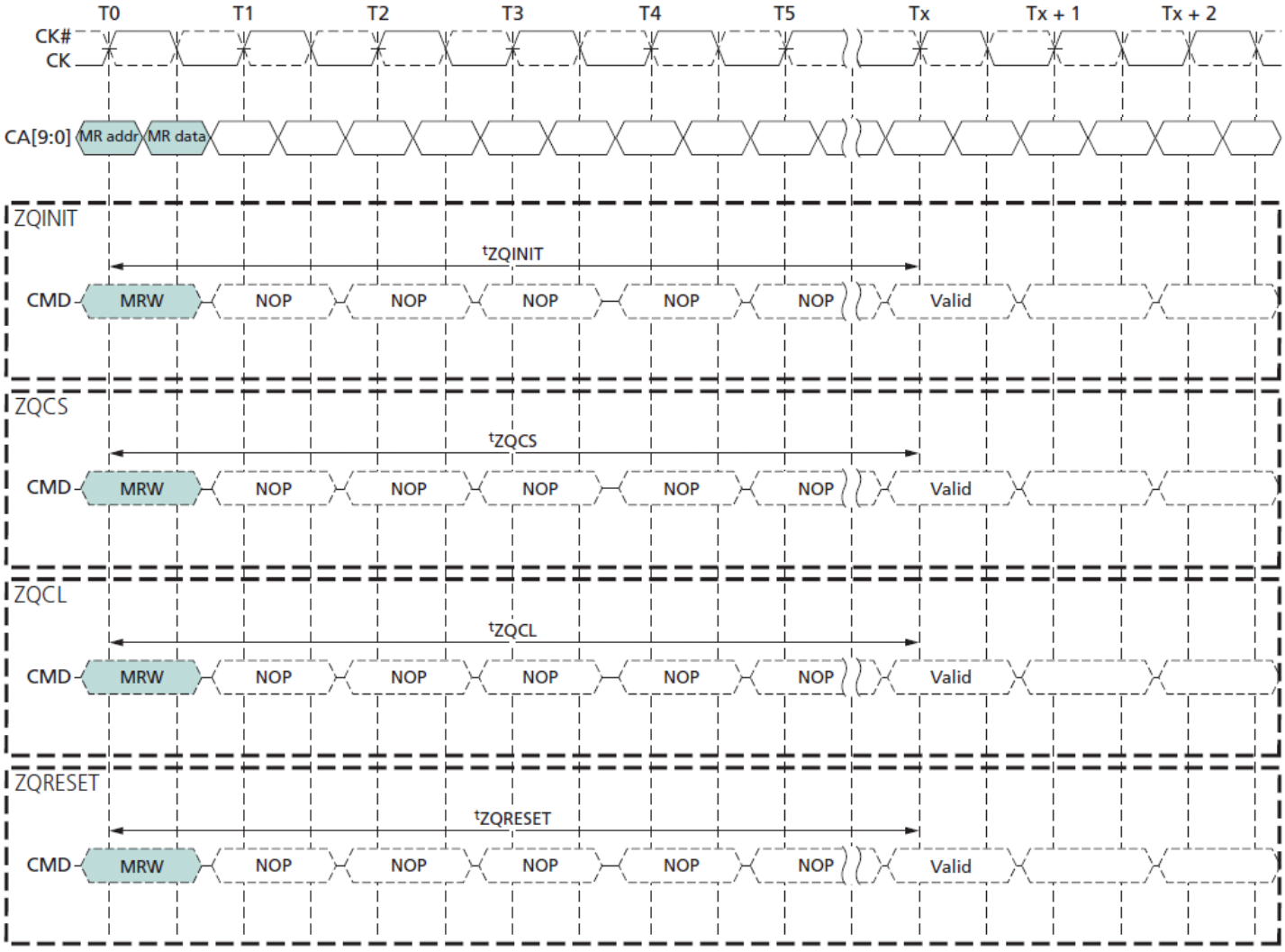
$$\frac{\text{ZQcorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{Vsens} \times \text{Vdriftrate})}$$

Where Tsens = MAX (dRONdT) andVsens = MAX (dRONdV) define temperature and voltage sensitivities.
For example, ifTsens = 0.75%/˚C,Vsens= 0.20%/mV,Tdriftrate = 1˚C/sec, and Vdriftrate = 15 mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4\text{s}$$

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged.
No other activities can be performed on the data bus during calibration periods (tZQINIT, tZQCL, or tZQCS).
The quiet time on the data bus helps to accurately calibrate output impedance.
There is no required quiet time after the ZQRESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.
In systems sharing a ZQ resistor between devices, the controller must prevent tZQINIT, tZQCS, and tZQCL overlap between the devices. ZQRESET overlap is acceptable. If the ZQ resistor is absent from the system, ZQ must be connected to VDDCA.
In this situation, the device must ignore ZQ calibration commands and the device will use the default calibration settings.

Figure 42: ZQ Timings



Notes : 1. Only the NOP command is supported during ZQ calibrations.

2. CKE must be registered HIGH continuously during the calibration period.

3. All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm (±1% tolerance) external resistor must be connected between the ZQ pin And ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap.The total capacitive loading on the ZQ pin must be limited (see the Input/Output Capacitance table).

Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS# is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as ACTIVATE, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down;

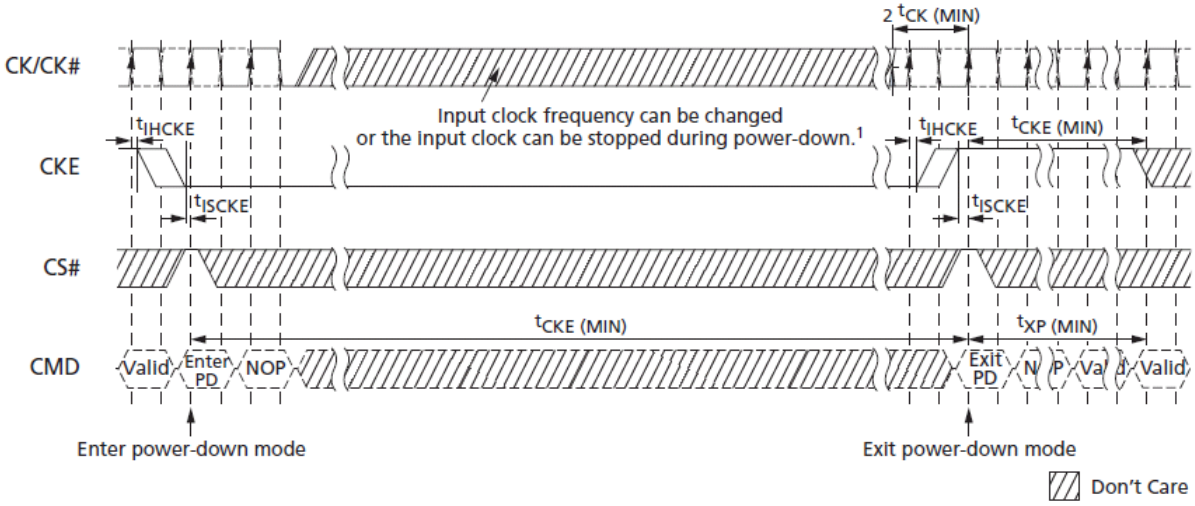
if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until tCKE is satisfied.VREFCA must be Maintained at a valid level during power-down. VDDQ can be turned off during power-down. IfVDDQ is turned off,VREFDQ must also be turned off. Prior to exiting power-down, bothVDDQ andVREFDQ must be within their respective minimum/maximum operating ranges (see AC and DC Operating Conditions).

No refresh operations are performed in power-down mode.The maximum duration in power-down mode is only limited by the refresh requirements outlined in REFRESH Command. The power-down state is exited when CKE is registered HIGH.

The controller must drive CS# HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the ACTiming section.

Figure 43: Power-Down Entry and Exit Timing



Note : 1. Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of two stable clocks complete.

Figure 44: CKE Intensive Environment

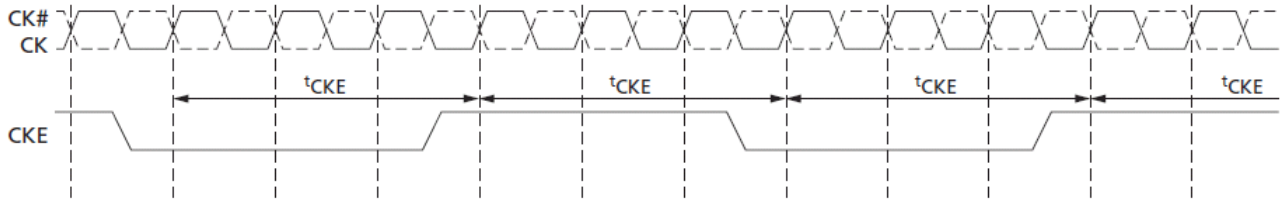
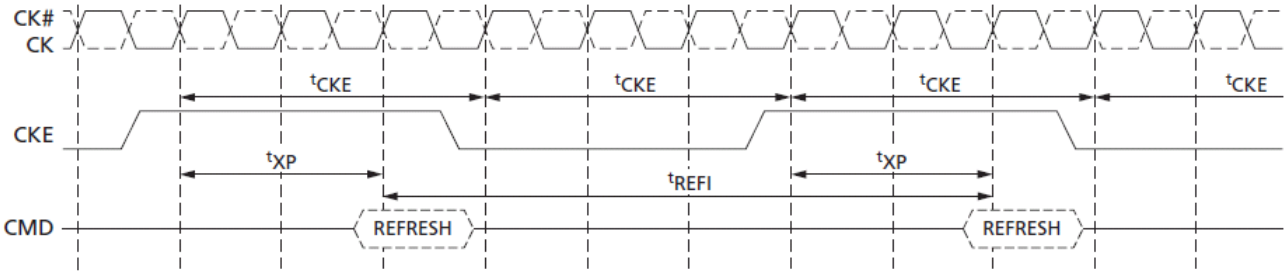


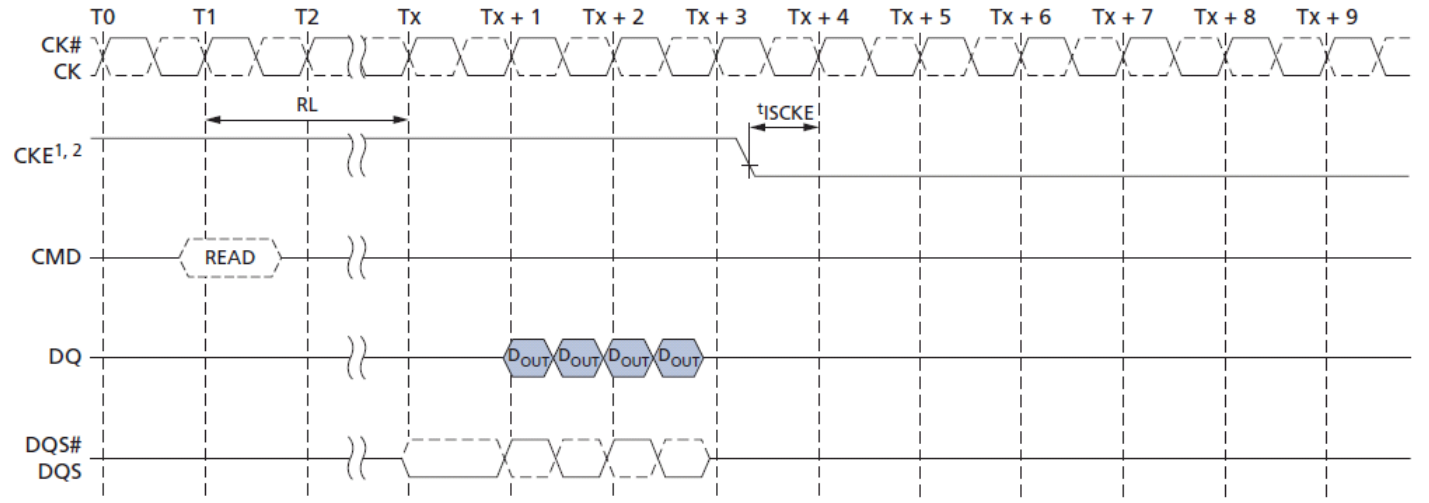
Figure 45: REFRESH-to-REFRESH Timing in CKE Intensive Environments



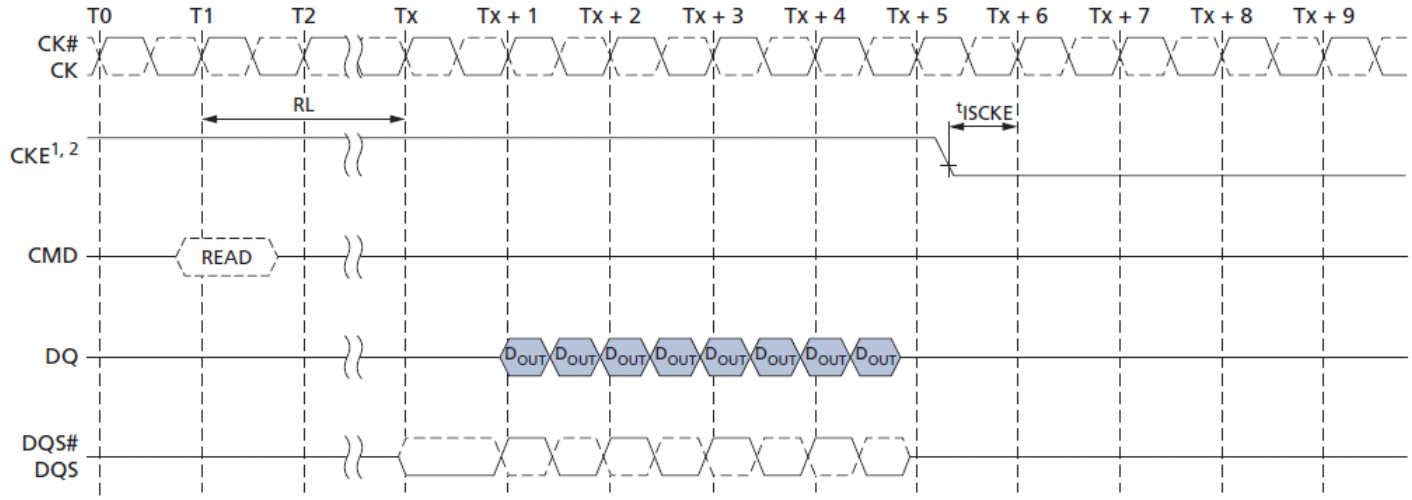
Note : 1. The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

Figure 46: READ to Power-Down Entry

BL = 4



BL = 8

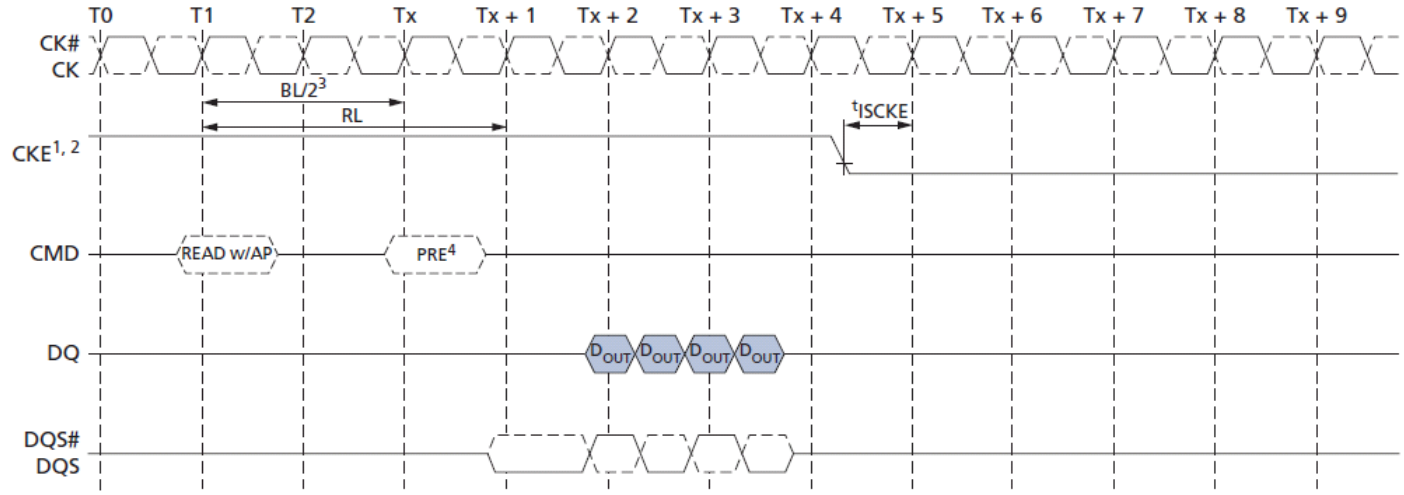


Notes : 1. CKE must be held HIGH until the end of the burst operation.

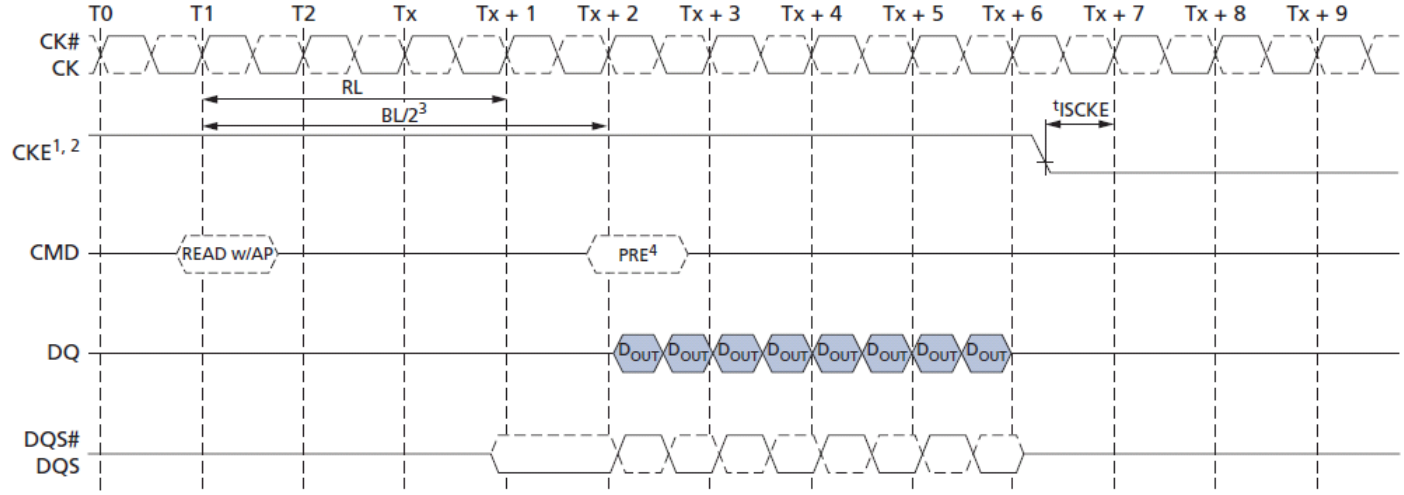
2. CKE can be registered LOW at (RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1) clock cycles after the clock on which the READ command is registered.

Figure 47: READ with Auto Precharge to Power-Down Entry

BL = 4



BL = 8

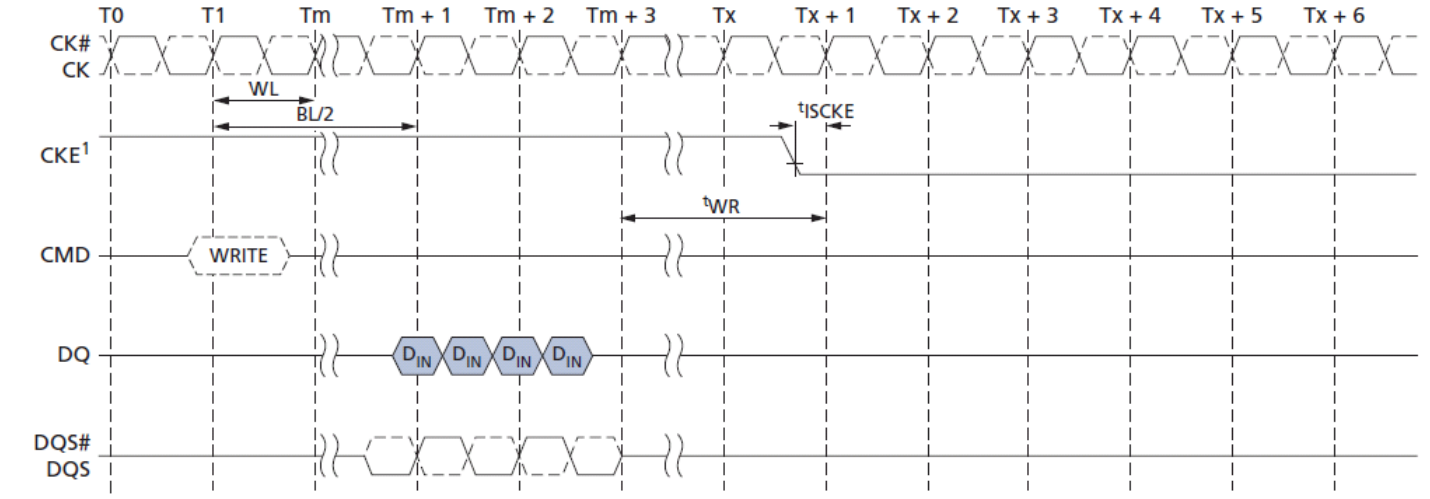


Notes : 1. CKE must be held HIGH until the end of the burst operation.

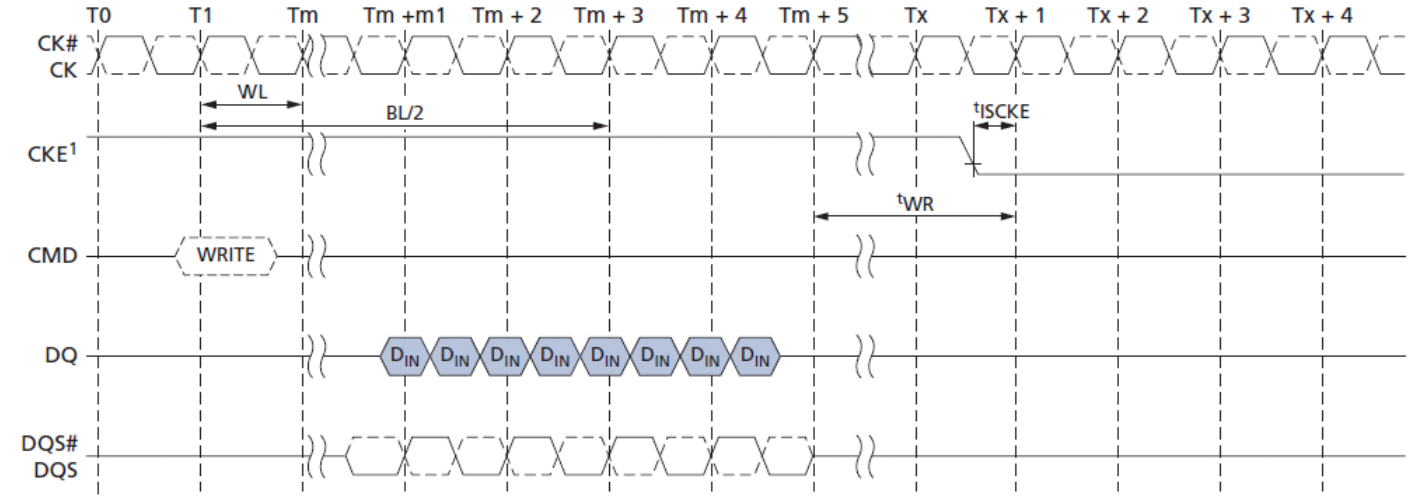
2. CKE can be registered LOW at (RL + RU(tDQSCK/tCK)+ BL/2 + 1) clock cycles after the clock on which the READ command is registered.
3. BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.
4. Start internal PRECHARGE.

Figure 48: WRITE to Power-Down Entry

BL = 4



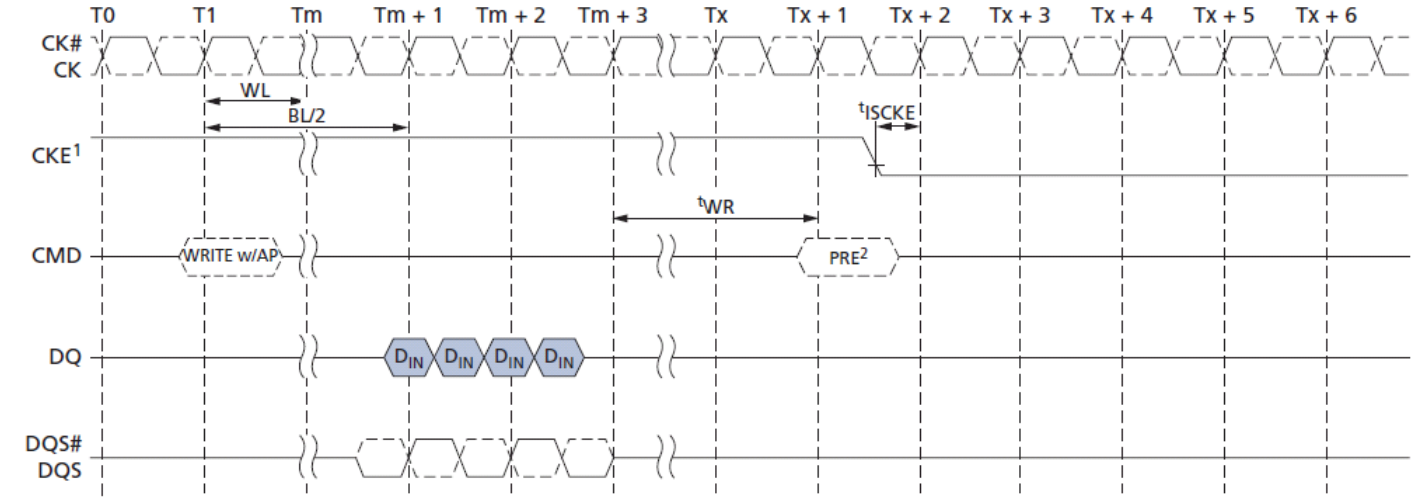
BL = 8



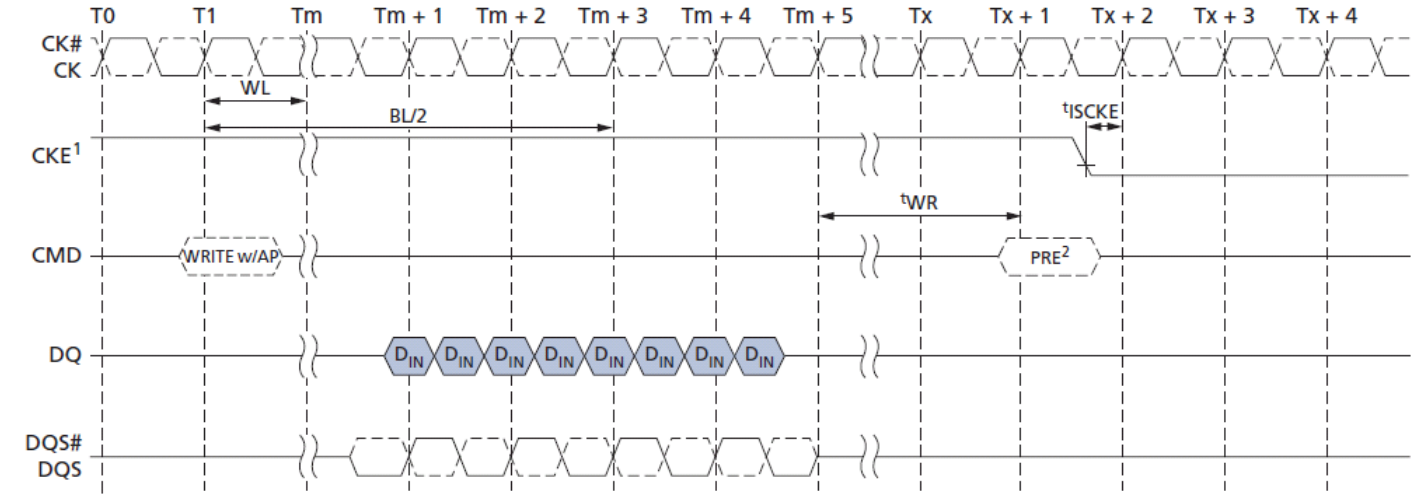
Note : 1. CKE can be registered LOW at (WL + 1 + BL/2 + RU(tWR/tCK)) clock cycles after the clock on which the WRITE command is registered.

Figure 49: WRITE with Auto Precharge to Power-Down Entry

BL = 4



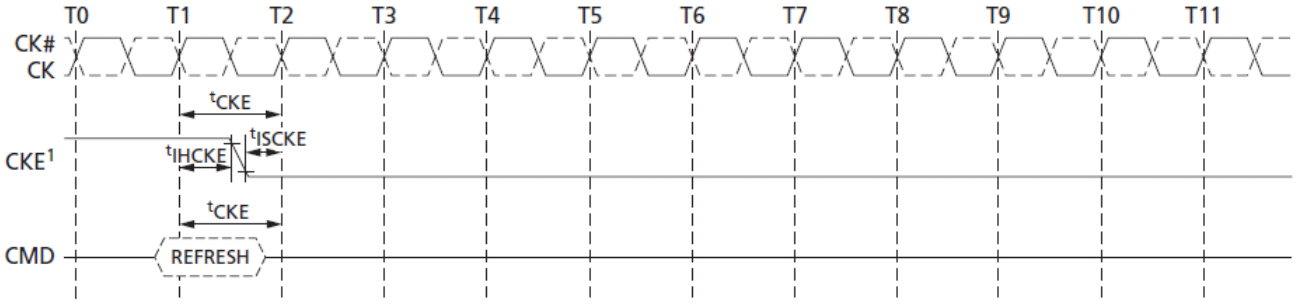
BL = 8



Notes : 1. CKE can be registered LOW at (WL + 1 + BL/2 + RU(tWR/tCK + 1) clock cycles after the WRITE command is registered.

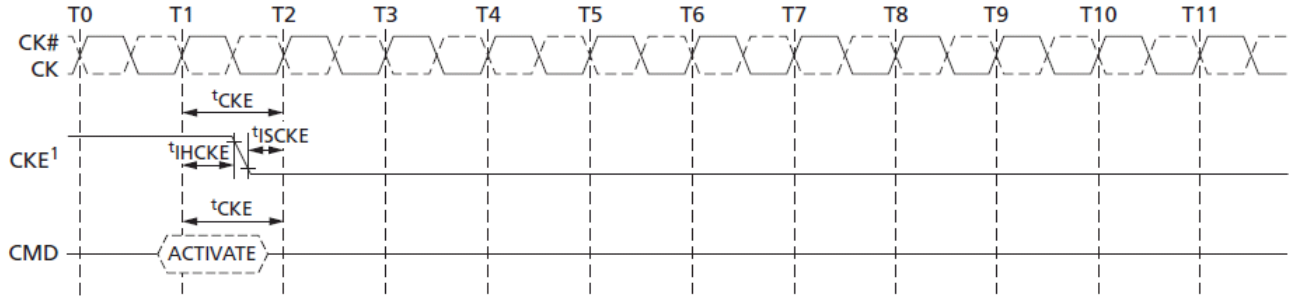
2. Start internal PRECHARGE.

Figure 50: REFRESH Command to Power-Down Entry



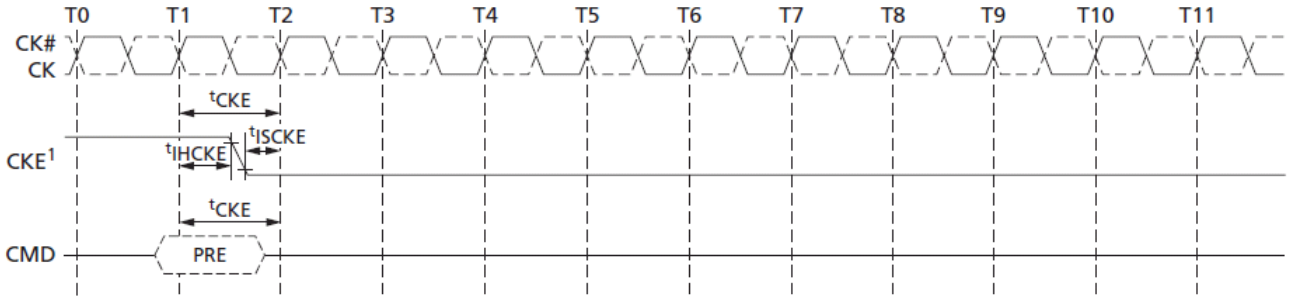
Note : 1. CKE can go LOW t_{IHCKE} after the clock on which the REFRESH command is registered.

Figure 51: ACTIVATE Command to Power-Down Entry



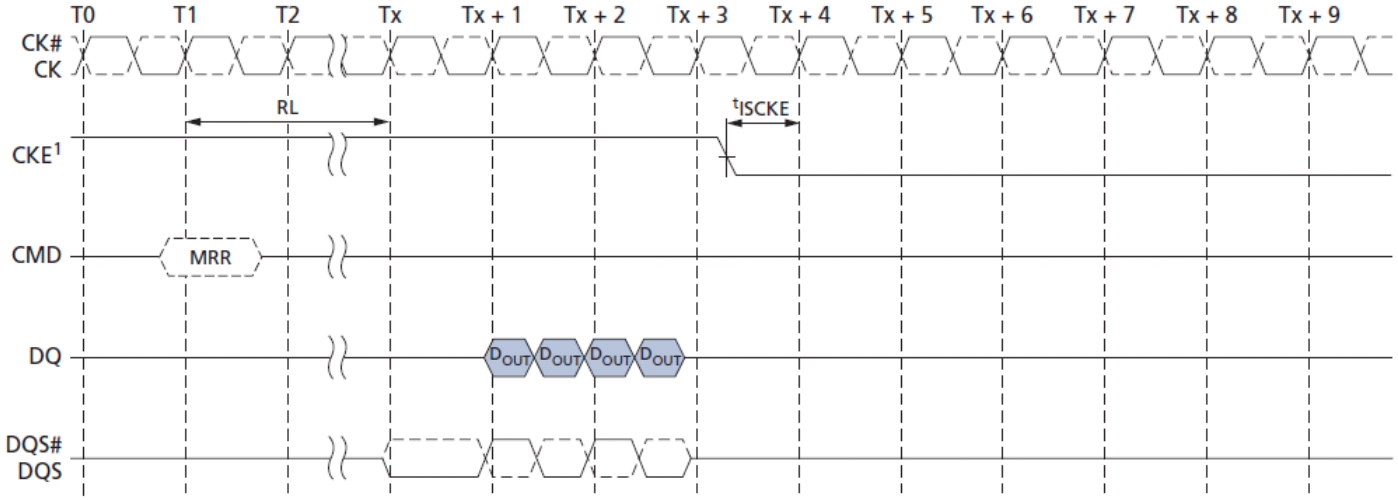
Note : 1. CKE can go LOW at t_{IHCKE} after the clock on which the ACTIVATE command is registered.

Figure 52: PRECHARGE Command to Power-Down Entry



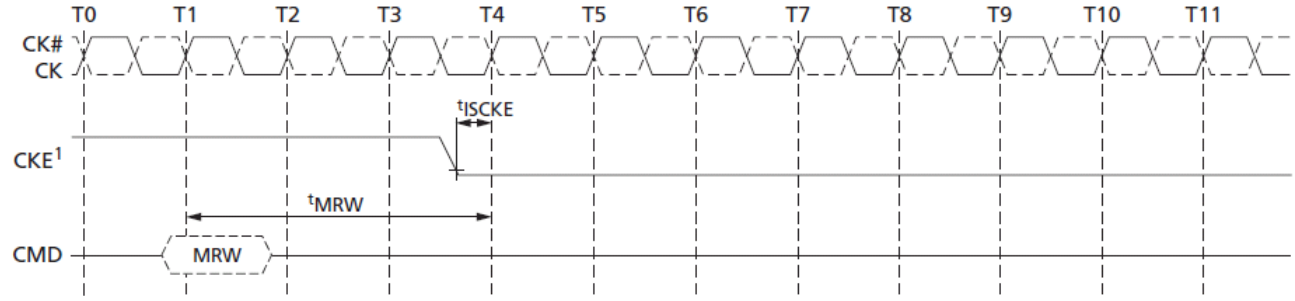
Note : 1. CKE can go LOW t_{IHCKE} after the clock on which the PRECHARGE command is registered.

Figure 53: MRR Command to Power-Down Entry



Note : 1. CKE can be registered LOW at (RL + RU(tDQSCK/tCK)+ BL/2 + 1) clock cycles after the clock on which the MRR command is registered.

Figure 54: MRW Command to Power-Down Entry



Note : 1. CKE can be registered LOW tMRW after the clock on which the MRW command is registered.

Deep Power-Down

Deep power-down (DPD) is entered when CKE is registered LOW with CS# LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock.The NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR or MRW operations are in progress. CKE can go LOW while other operations such as ACTIVATE, auto precharge, PRECHARGE, or REFRESH are in progress, however, deep power-down IDD specifications will not be applied until those operations complete.

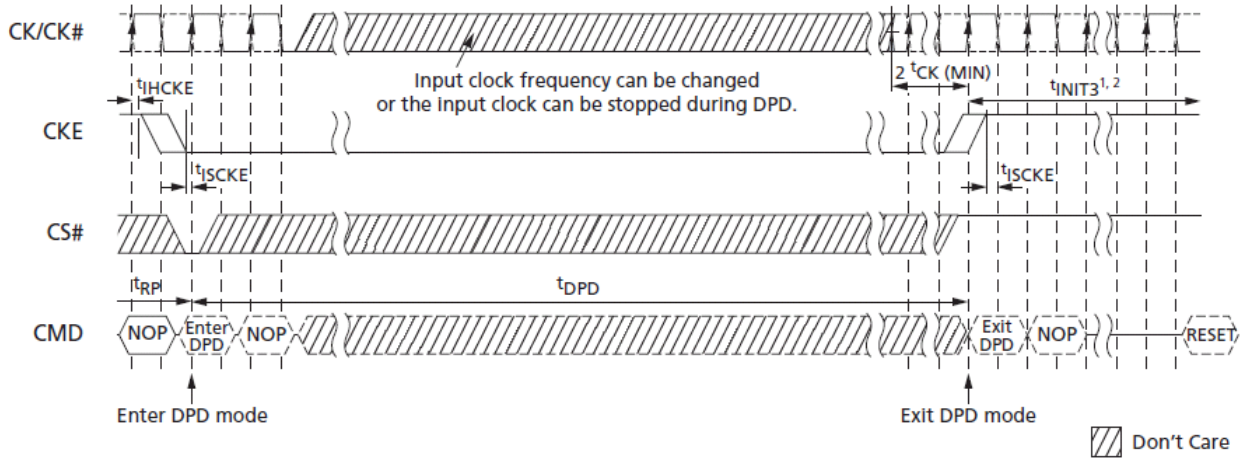
The contents of the array will be lost upon entering DPD mode.

In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device.VREFDQ can be at any level between 0 and VDDQ, andVREFCA can be at any level between 0 andVDDCA during DPD.

All power supplies (including VREF) must be within the specified limits prior to exiting DPD (see AC and DC Operating Conditions).

To exit DPD, CKE must be HIGH, tISCKE must be complete, and the clock must be stable. To resume operation, the device must be fully reinitialized using the power-up initialization sequence.

Figure 55: Deep Power-Down Entry and Exit Timing



Notes : 1. The initialization sequence can start at any time after Tx + 1.

2. tINIT3 and Tx + 1 refer to timings in the initialization sequence. For details, see Mode Register Definition.

Input Clock Frequency Changes and Stop Events

Input Clock Frequency Changes and Clock Stop with CKE LOW

During CKE LOW, Mobile LPDDR2 devices support input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,tRCD and tRP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of two clock cycles after CKE goes LOW
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of two clock cycles prior to CKE going HIGH

For input clock frequency changes, tCK(MIN) and tCK(MAX) must be met for each clock cycle.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set theWR, RL, etc.

These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK is held LOW and CK# is held HIGH.

Input Clock Frequency Changes and Clock Stop with CKE HIGH

During CKE HIGH, LPDDR2 devices support input clock frequency changes and clock stop under the following conditions:

- REFRESH requirements are met.
- Any ACTIVATE, READ, WRITE, PRECHARGE, MRW, or MRR commands must have completed, including any associated data bursts, prior to changing the frequency.
- Related timing conditions, tRCD, tWR, tWRA, tRP, tMRW, and tMRR, etc., are met
- CS# must be held HIGH
- Only REFab or REFpb commands can be in process

The device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 × tCK + tXP.

For input clock frequency changes, tCK(MIN) and tCK(MAX) must be met for each clock cycle.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK is held LOW and CK# is held HIGH.

NO OPERATION Command

The NO OPERATION (NOP) command prevents the device from registering any unwanted commands issued between operations. A NOP command can only be issued at clock cycle N when the CKE level is constant for clock cycle N-1 and clock cycle N. The NOP command has tw possible encodings: CS# HIGH at the clock rising edge N; and CS# LOW with CA0,

CA1, CA2 HIGH at the clock rising edge N.

The NOP command will not terminate a previous operation that is still in process, such as a READ burst or WRITE burst cycle.

Simplified Bus Interface State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications.

The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks.

Truth Tables

Truth tables provide complementary information to the state diagram.They also clarify device behavior and applicable restrictions when considering the actual state of the banks. Unspecified operations and timings are illegal.To ensure proper operation after an illegal event, the device must be powered down and then restarted using the specified initialization sequence before normal operation can continue.

Table30 : Command Truth table

Notes 1–11 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE		/CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
	H	H	X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
	H	H	X	MA6	MA7	X								
REFRESH (per bank)	H	H	L	L	L	H	L	X						
	H	H	X	X										
REFRESH (all banks)	H	H	L	L	L	H	H	X						
	H	H	X	X										
Enter self refresh	H	L	L	L	L	H	X							
	X	L	X	X										
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	
	H	H	X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	
WRITE(bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
READ bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
PRECHARGE (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	
	H	H	X	X										
BST	H	H	L	H	H	L	L	X						
	H	H	X	X										
Enter DPD	H	L	L	H	H	L	X							
	X	L	X	X										
NOP	H	H	L	H	H	H	X							
	H	H	X	X										
Maintain PD, SREF, DPD, (NOP)	L	L	L	H	H	H	X							
	L	L	X	X										
NOP	H	H	H	X										
	H	H	X	X										
Maintain PD, SREF, DPD, (NOP)	L	L	H	X										
	L	L	X	X										
Enter power-down	H	L	H	X										
	X	L	X	X										
Exit PD, SREF, DPD	L	H	H	X										
	X	H	X	X										

Notes : 1. All commands are defined by the current state of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.

2. Bank addresses (BA) determine which bank will be operated upon.
3. AP HIGH during a READ or WRITE command indicates that an auto precharge will occur To the bank associated with the READ or WRITE command.

4. X indicates a “Don’t Care” state, with a defined logic level, either HIGH (H) or LOW (L).
5. Self refresh exit and DPD exit are asynchronous.
6. VREF must be between 0 and VDDQ during self refresh and DPD operation.
7. CAxr refers to command/address bit “x” on the rising edge of clock.
8. CAxf refers to command/address bit “x” on the falling edge of clock.
9. CS# and CKE are sampled on the rising edge of the clock.
10. Per-bank refresh is only supported in devices with eight banks.
11. he least-significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.

Table31 : CKE Truth Table

Notes 1–5 apply to all parameters and conditions ; L=LOW , H=HIGH , X=“Don’t Care”

Current State	CKEn-1	CKEn	CS#	Command n	Operation n	Next State	Notes
Active power-down	L	L	X	X	Maintain active power-down	Active power-down	
	L	H	H	NOP	Exit active power-down	Active	6, ,7
Idle power-down	L	L	X	X	Maintain idle power-down	Idle power-down	
	L	H	H	NOP	Exit idle power-down	Idle	6, 7
Resetting idle power-down	L	L	X	X	Maintain resetting power-down	Resetting power-down	
	L	H	H	NOP	Exit resetting power-down	Idle or resetting	6, 7, 8
Deep power-down	L	L	X	X	Maintain deep power-down	Deep power-down	
	L	H	H	NOP	Exit deep power-down	Power-on	9
Self refresh	L	L	X	X	Maintain self refresh	Self refresh	
	L	H	H	NOP	Exit self refresh	Idle	10, 11
Bank(s) active	H	L	H	NOP	Enter active power-down	Active power-down	
All banks idle	H	L	H	NOP	Enter idle power-down	Idle power-down	
	H	L	L	Enter self refresh	Enter self refresh	Self refresh	
	H	L	L	DPD	Enter deep power-down	Deep power-down	
Resetting	H	L	H	NOP	Enter deep power-down	Resetting power-down	
Other states	H	H	Refer to the command truth table				

Notes : 1. Current state = the state of the device immediately prior to the clock rising edge *n.*

2. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
3. CKE*n = the logic state of CKE at clock rising edge n; CKEn-1 was the state of CKE at the* previous clock edge.
4. CS#= the logic state of CS# at the clock rising edge *n.*
5. Command *n = the command registered at clock edge n, and operation n is a result of* command *n.*
6. Power-down exit time (tXP) must elapse before any command other than NOP is issued.

7. The clock must toggle at least twice prior to the tXP period.
8. Upon exiting the resetting power-down state, the device will return to the idle state if tINIT5 has expired.
9. The DPD exit procedure must be followed as described in Deep Power-Down (page 60).
10. Self refresh exit time (tXSR) must elapse before any command other than NOP is issued.
11. The clock must toggle at least twice prior to the tXSR time.

Table32 : Current State Bank *n* to Command to Bank *n* Truth Table

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current state	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (per bank)	Begin to refresh	Refreshing (per bank)	6
	Refresh (all banks)	Begin to refresh	Refreshing (all banks)	7
	MRW	Load value to mode register	MR writing	7
	MRR	Read value from mode register	Idle, MR reading	
	RESET	Begin device auto initialization	Resetting	7, 8
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9, 10
Row active	READ	Select column and start read burst	Reading	
	WRITE	Select column and start write burst	Writing	
	MRR	Read value from mode register	Active MR reading	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9
Reading	READ	Select column and start new read burst	Reading	11, 12
	WRITE	Select column and start write burst	Writing	11, 12, 13
	BST	Read burst terminate	Active	14
Writing	WRITE	Select column and start new write burst	Writing	11, 12
	READ	Select column and start read burst	Reading	11, 12, 15
	BST	Write burst terminate	Active	14
Power-on	MRW RESET	Begin device auto initialization	Resetting	7, 9
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes : 1. Values in this table apply when both CKE*n -1 and CKEn are HIGH, and after tXSR or tXP* has been met, if the previous state was power-down.

2. All states and sequences not shown are illegal or reserved.
3. Current state definitions: Idle: The bank or banks have been precharged, and tRP has been met.
   Active : A row in the bank has been activated, and tRCD has been met. No data bursts or accesses and no register accesses are in progress. Reading: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated. Writing: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
4. The states listed below must not be interrupted by a command issued to the same bank.
   NOP commands or supported commands to the other bank must be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state, and the definitions given in Table 33 .

Precharge: Starts with registration of a PRECHARGE command and ends when tRP is met. After tRP is met, the bank is in the idle state.

Row activate: Starts with registration of an ACTIVATE command and ends when tRCD is met. After tRCD is met, the bank is in the active state. READ with AP enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.

WRITE with AP enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied to each rising clock edge during these states. Refresh (per bank): Starts with registration of a REFRESH (per bank) command and ends when tRFCpb is met. After tRFCpb is met, the bank is in the idle state. Refresh (all banks): Starts with registration of a REFRESH (all banks) command and ends when tRFCab is met. After tRFCab is met, the device is in the all banks idle state. Idle MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in the all banks idle state.

   Resetting MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in the all banks idle state. Active MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the bank is in the active state. MR writing: Starts with registration of the MRW command and ends when tMRW is met.

   After tMRW is met, the device is in the all banks idle state. Precharging all: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. After tRP is met, the device is in the all banks idle state.
6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. If a PRECHARGE command is issued to a bank in the idle state, tRP still applies.
11. A command other than NOP should not be issued to the same bank while a burst READ or burst WRITE with auto precharge is enabled.
12. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
13. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.
14. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ / WRITE command, regardless of bank.
15. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

Table 33: Current State Bank *n* to Command to Bank *m* Truth Table

Notes 1–6 apply to all parameters and conditions

Current State of Bank n	Command to Bank m	Operation	Next State for Bank m	notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command supported to Bank m	-	7
Row activating, active, or precharging	ACTIVATE	Select and activate row in bank m	Active	8
	READ	Select column and start READ Burst from bank m	Reading	9
	WRITE	Select column and start WRITE burst to bank m	Writing	9
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
	MRR	READ value from mode register	Idle MR reading or Active MR reading	11,12,13
	BST	READ or WRITE burst terminates an ongoing READ/WRITE from/to bank m	Active	7
Reading (auto precharge disabled)	READ	Select column and start READ burst from bank m	Reading	9
	WRITE	Select column and start WRITE burst to bank m	Writing	9,14
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing (auto precharge disabled)	READ	Select column and start READ burst from bank m	Reading	9,15
	WRITE	Select column and start WRITE burst to bank m	Writing	9
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Reading with auto precharge	READ	Select column and start READ burst from bank m	Reading	9,16
	WRITE	Select column and start WRITE burst to bank m	Writing	9,14,16
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing with auto precharge	READ	Select column and start READ burst from bank m	Reading	9,15,16
	WRITE	Select column and start WRITE burst to bank m	Writing	9,16
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Power-on	MRW RESET	Begin device auto initialization	Resetting	17,18
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes : 1. This table applies when: the previous state was self refresh or power-down ; after tXSR or tXP has been met; *and both CKEn -1 and CKEn are HIGH.*

2. All states and sequences not shown are illegal or reserved.

3. Current state definitions:
   Idle: The bank has been precharged and tRP has been met.
   Active: A row in the bank has been activated, tRCD has been met, no data bursts or accesses and no register accesses are in progress. Read: A READ burst has been initiated with auto precharge disabled and the READ has not yet terminated or been terminated. Write: A WRITE burst has been initiated with auto precharge disabled and the WRITE has not yet terminated or been terminated.
4. Refresh, self refresh, and MRW commands can only be issued when all banks are idle.
5. A BST command cannot be issued to another bank; it applies only to the bank represented by the current state.
6. The states listed below must not be interrupted by any executable command.
   NOP commands must be applied during each clock cycle while in these states:
   Idle MRR: Starts with registration of the MRR command and ends when tMRR has been met.
   After tMRR is met, the device is in the all banks idle state.
   Reset MRR: Starts with registration of the MRR command and ends when tMRR has been met.
   After tMRR is met, the device is in the all banks idle state.
   Active MRR: Starts with registration of the MRR command and ends when tMRR has been met.
   After tMRR is met, the bank is in the active state.
   MRW: Starts with registration of the MRW command and ends when tMRW has been met.
   After tMRW is met, the device is in the all banks idle state.
7. BST is supported only if a READ or WRITE burst is ongoing.
8. tRRD must be met between the ACTIVATE command to bank *n and any subsequent* ACTIVATE command to bank *m.*
9. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
10. This command may or may not be bank-specific.
    If all banks are being precharged, they must be in a valid state for precharging.
11. MRR is supported in the row-activating state.
12. MRR is supported in the precharging state.
13. The next state for bank *m depends on the current state of bank m (idle, row-activating,* precharging, or active).
14. A WRITE command can be issued after the completion of the READ burst;
    otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. A READ command can be issued after the completion of the WRITE burst;
    otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.
16. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided that the timing restrictions in the PRECHARGE and Auto Precharge Clarification table are met.
17. Not bank-specific; requires that all banks are idle and no bursts are in progress.
18. RESET command is achieved through MODE REGISTER WRITE command.

Table 34: DM Truth Table

Functional Name	DM	DQ	notes
Write enable	L	Valid	1
Write inhibit	H	X	1

Note : 1. Used to mask write data, and is provided simultaneously with the corresponding input data.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this document is not implied.

Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 35: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	–0.4	+2.3	V	1
VDD2 supply voltage relative to VSS	VDD2 (1.2V)	–0.4	+1.6	V	1
VDDCA supply voltage relative to VSSCA	VDDCA	–0.4	+1.6	V	1,2
VDDQ supply voltage relative to VSSQ	VDDQ	–0.4	+1.6	V	1,3
Voltage on any ball relative to VSS	V_{IN}, V_{OUT}	–0.4	+1.6	V	
Storage temperature	T_{STG}	–0.4	+125	°C	4

Notes : 1. See 1. Voltage Ramp under Power-Up (page 7).

2. V_{REFCA} 0.6 ≤ V_{DDCA}; however, V_{REFCA} may be ≥ V_{DDCA} provided that V_{REFCA} ≤ 300mV.
3. V_{REFDQ} 0.6 ≤ V_{DDQ}; however, V_{REFDQ} may be ≥ V_{DDQ} provided that V_{REFDQ} ≤ 300mV.
4. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Input/Output Capacitance

Table 36: Input/Output Capacitance

Note 1 applies to all parameters and conditions

Parameter	Symbol	LPDDR2 1066-466		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		
Input capacitance, CK and CK#	CCK	1.0	2.0	1.0	2.0	pF	1
Input capacitance delta, CK and CK#	CDCK	0	0.2	0	0.25	pF	1
Input capacitance, all other input Only pins	CI	1.0	2.0	1.0	2.0	pF	1,2
Input capacitance delta, all other input Only pins	CDI	-0.40	+0.40	-0.50	+0.50	pF	1,3
Input/output capacitance, DQ,DM,DQS, DQS#	CIO	1.25	2.5	1.25	2.5	pF	
Input/output capacitance delta, DQS, DQS#	CDDQS	0	0.25	0	0.30	pF	
Input/output capacitance delta, DQ,DM	CDIO	-0.5	+0.5	-0.6	+0.6	pF	
Input/output capacitance ZQ	CZQ	0	2.5	0	2.5	pF	4

Notes : 1. T_C –25°C to +105°C; V_{DDQ} = 1.14–1.3V; V_{DDCA} = 1.14–1.3V; V_{DD1} = 1.7–1.95V; V_{DD2} = 1.14–1.3V.

2. This parameter applies to die devices only (does not include package capacitance).
3. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSCA}, and V_{SSQ} applied; all other pins are left floating.
4. Absolute value of C_{CK} - $C_{CK\#}$.
5. C_I applies to CS#, CKE, and CA[9:0].

6. $C_{DI} = C_I - 0.5 \times (C_{CK} + C_{CK\#})$.
7. DM loading matches DQ and DQS.
8. MR3 I/O configuration drive strength OP[3:0] = 0001b (34.3 ohm typical).
9. Absolute value of C_{DQS} and $C_{DQS\#}$.
10. $C_{DIO} = C_{IO} - 0.5 \times (C_{DQS} + C_{DQS\#})$ in byte-lane.
11. Maximum external load capacitance on ZQ pin: 5pF.

Electrical Specifications – IDD Specifications and Conditions

The following definitions and conditions are used in the IDD measurement tables unless stated otherwise:

- LOW:VIN ≤VIL(DC)max
- HIGH:VIN ≥VIH(DC)min
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following three tables

Table 37: Switching for CA Input Signals

Notes 1–3 apply to all parameters and conditions

Parameter	CK Rising/ CK# Falling	CK Rising/ CK# Falling	CK Rising/ CK# Falling	CK Rising/ CK# Falling	CK Rising/ CK# Falling	CK Rising/ CK# Falling	CK Rising/ CK# Falling	CK Rising/ CK# Falling
Cycle	N		N+1		N+2		N+3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes : 1. CS# must always be driven HIGH.

2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
3. The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 38: Switching for I_{DD4R}

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	HLH	LHLLHLH	L
Rising	H	L	N+2	Read_Rising	HLH	LHLLHLH	H
Falling	H	L	N+2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	HLH	LHLHLHL	L

Notes : 1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.

2. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4R}

Table 39: Switching for I_{DD4W}

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write Rising	LLH	LHLHLHL	L
Falling	H	L	N	Write Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	LLH	LHLLHLH	L
Rising	H	L	N+2	Write Rising	LLH	LHLLHLH	H
Falling	H	L	N+2	Write Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	LLH	LHLHLHL	L

Notes : 1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.

2. Data masking (DM) must always be driven LOW.

3. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4W}.

Table 40: IDD Specification and Conditions(X16)

Parameter / Condition	Symbol	Power Supply	Data Rate			Unit	Notes
			-18	-25	-30		
Operating one bank active-precharge current (SDRAM) : tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	IDD01	VDD1	TBD	20	TBD	mA	
	IDD02	VDD2	TBD	65	TBD		
	IDD0in	VDDCA,VDDQ	TBD	8	TBD		4
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	IDD2P1	VDD1	TBD	800	TBD	µA	
	IDD2P2	VDD2	TBD	1600	TBD		
	IDD2P,in	VDDCA,VDDQ	TBD	100	TBD		4
Idle power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	IDD2PS1	VDD1	TBD	800	TBD	µA	
	IDD2PS2	VDD2	TBD	1600	TBD		
	IDD2PS,in	VDDCA,VDDQ	TBD	100	TBD		4
Idle non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	IDD2N1	VDD1	TBD	1.7	TBD	mA	
	IDD2N2	VDD2	TBD	38	TBD		
	IDD2N,in	VDDCA,VDDQ	TBD	8	TBD		4
Idle non-power-down standby current with clock stopped: CK = LOW; CK# = HIGH; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	IDD2NS1	VDD1	TBD	1.7	TBD	mA	
	IDD2NS2	VDD2	TBD	16	TBD		
	IDD2NS,in	VDDCA, VDDQ	TBD	8	TBD		4
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	IDD3P1	VDD1	TBD	2000	TBD	µA	
	IDD3P2	VDD2	TBD	4	TBD	mA	
	IDD3P,in	VDDCA, VDDQ	TBD	120	TBD	µA	4
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	IDD3PS1	VDD1	TBD	2000	TBD	µA	
	IDD3PS2	VDD2	TBD	4	TBD	mA	
	IDD3PS,in	VDDCA, VDDQ	TBD	120	TBD	µA	4
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	IDD3N1	VDD1	TBD	2	TBD	mA	
	IDD3N2	VDD2	TBD	40	TBD		
	IDD3N,in	VDDCA, VDDQ	TBD	8	TBD		4
Active non-power-down standby current with clock stopped : CK = LOW, CK# = HIGH CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	IDD3NS1	VDD1	TBD	2	TBD	mA	
	IDD3NS2	VDD2	TBD	24	TBD		
	IDD3NS,in	VDDCA, VDDQ	TBD	8	TBD		4

Table 41: IDD Specification and Conditions(X16) (continued)

Parameter / Condition	Symbol	Power Supply	Data Rate			Unit	Notes
			-18	-25	-30		
Operating burst READ current: tCK = tCKmin; CS# is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer	IDD4R1	VDD1	TBD	5	TBD	mA	
	IDD4R2	VDD2	TBD	220	TBD		
	IDD4R,in	VDDCA	TBD	8	TBD		
Operating burst WRITE current: tCK = tCKmin; CS# is HIGH between valid commands; One bank is active; BL = 4; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer	IDD4W1	VDD1	TBD	10	TBD	mA	
	IDD4W2	VDD2	TBD	185	TBD		
	IDD4W,in	VDDCA, VDDQ	TBD	28	TBD		4
All-bank REFRESH burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	IDD51	VDD1	TBD	20	TBD	mA	
	IDD52	VDD2	TBD	130	TBD		
	IDD5IN	VDDCA, VDDQ	TBD	8	TBD		4
All-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable	IDD5AB1	VDD1	TBD	6	TBD	mA	
	IDD5AB2	VDD2	TBD	40	TBD		
	IDD5AB,in	VDDCA, VDDQ	TBD	8	TBD		4
Per-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable	IDD5PB1	VDD1	TBD	6	TBD	mA	5
	IDD5PB2	VDD2	TBD	40	TBD		5
	IDD5PB,in	VDDCA, VDDQ	TBD	8	TBD		4, 5
Self refresh current (–25˚C to +85˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	IDD61	VDD1	TBD	1400	TBD	µA	6
	IDD62	VDD2	TBD	3000	TBD		6
	IDD6IN	VDDCA, VDDQ	TBD	100	TBD		4,6
Deep power-down current: CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	IDD81	VDD1	TBD	50	TBD	µA	7
	IDD82	VDD2	TBD	30	TBD		7
	IDD8IN	VDDCA, VDDQ	TBD	30	TBD		4, 7

Notes : 1. IDD values are the maximum of the distribution of the arithmetic mean.

2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the sum of VDDQ and VDDCA.
5. Per-bank REFRESH is only applicable for LPDDR2-S4 device densities 1Gb or higher.
6. This is the general definition that applies to full-array self refresh.
7. IDD6ET and IDD8 are typical values, are sampled only, and are not tested.

Table 42: IDD Specification and Conditions(X32)

Parameter / Condition	Symbol	Power Supply	Data Rate			Unit	Notes
			-18	-25	-30		
Operating one bank active-precharge current (SDRAM) : tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	IDD01	VDD1	TBD	20	TBD	mA	
	IDD02	VDD2	TBD	65	TBD		
	IDD0in	VDDCA,VDDQ	TBD	8	TBD		4
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	IDD2P1	VDD1	TBD	800	TBD	µA	
	IDD2P2	VDD2	TBD	1600	TBD		
	IDD2P,in	VDDCA,VDDQ	TBD	100	TBD		4
Idle power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	IDD2PS1	VDD1	TBD	800	TBD	µA	
	IDD2PS2	VDD2	TBD	1600	TBD		
	IDD2PS,in	VDDCA,VDDQ	TBD	100	TBD		4
Idle non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	IDD2N1	VDD1	TBD	1.7	TBD	mA	
	IDD2N2	VDD2	TBD	38	TBD		
	IDD2N,in	VDDCA,VDDQ	TBD	8	TBD		4
Idle non-power-down standby current with clock stopped: CK = LOW; CK# = HIGH; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	IDD2NS1	VDD1	TBD	1.7	TBD	mA	
	IDD2NS2	VDD2	TBD	16	TBD		
	IDD2NS,in	VDDCA, VDDQ	TBD	8	TBD		4
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	IDD3P1	VDD1	TBD	2000	TBD	µA	
	IDD3P2	VDD2	TBD	4	TBD	mA	
	IDD3P,in	VDDCA, VDDQ	TBD	120	TBD	µA	4
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	IDD3PS1	VDD1	TBD	2000	TBD	µA	
	IDD3PS2	VDD2	TBD	4	TBD	mA	
	IDD3PS,in	VDDCA, VDDQ	TBD	120	TBD	µA	4
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	IDD3N1	VDD1	TBD	2	TBD	mA	
	IDD3N2	VDD2	TBD	40	TBD		
	IDD3N,in	VDDCA, VDDQ	TBD	8	TBD		4
Active non-power-down standby current with clock stopped : CK = LOW, CK# = HIGH CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	IDD3NS1	VDD1	TBD	2	TBD	mA	
	IDD3NS2	VDD2	TBD	24	TBD		
	IDD3NS,in	VDDCA, VDDQ	TBD	8	TBD		4

Table 43: IDD Specification and Conditions(X32) (continued)

Parameter / Condition	Symbol	Power Supply	Data Rate			Unit	Notes
			-18	-25	-30		
Operating burst READ current: tCK = tCKmin; CS# is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer	IDD4R1	VDD1	TBD	5	TBD	mA	
	IDD4R2	VDD2	TBD	220	TBD		
	IDD4R,in	VDDCA	TBD	8	TBD		
Operating burst WRITE current: tCK = tCKmin; CS# is HIGH between valid commands; One bank is active; BL = 4; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer	IDD4W1	VDD1	TBD	10	TBD	mA	
	IDD4W2	VDD2	TBD	185	TBD		
	IDD4W,in	VDDCA, VDDQ	TBD	28	TBD		4
All-bank REFRESH burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	IDD51	VDD1	TBD	20	TBD	mA	
	IDD52	VDD2	TBD	130	TBD		
	IDD5IN	VDDCA, VDDQ	TBD	8	TBD		4
All-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable	IDD5AB1	VDD1	TBD	6	TBD	mA	
	IDD5AB2	VDD2	TBD	40	TBD		
	IDD5AB,in	VDDCA, VDDQ	TBD	8	TBD		4
Per-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable	IDD5PB1	VDD1	TBD	6	TBD	mA	5
	IDD5PB2	VDD2	TBD	40	TBD		5
	IDD5PB,in	VDDCA, VDDQ	TBD	8	TBD		4, 5
Self refresh current (–25˚C to +85˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	IDD61	VDD1	TBD	1400	TBD	µA	6
	IDD62	VDD2	TBD	3000	TBD		6
	IDD6IN	VDDCA, VDDQ	TBD	100	TBD		4,6
Deep power-down current: CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	IDD81	VDD1	TBD	50	TBD	µA	7
	IDD82	VDD2	TBD	30	TBD		7
	IDD8IN	VDDCA, VDDQ	TBD	30	TBD		4, 7

Notes : 1. IDD values are the maximum of the distribution of the arithmetic mean.

2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the sum of VDDQ and VDDCA.
5. Per-bank REFRESH is only applicable for LPDDR2-S4 device densities 1Gb or higher.
6. This is the general definition that applies to full-array self refresh.
7. IDD6ET and IDD8 are typical values, are sampled only, and are not tested.

Table 44: IDD6 Partial-Array Self Refresh Current

VDD2, VDDQ, VDDCA = 1.14–1.30V; VDD1 = 1.70–1.95V

PASR	Symbol	Power Supply	Unit
Full array	VDD1	1400	µA
	VDD2	3000	
	VDDi	100	
1/2 array	VDD1	1200	
	VDD2	2500	
	VDDi	100	
1/4 array	VDD1	1000	
	VDD2	2300	
	VDDi	100	
1/8 array	VDD1	1000	
	VDD2	2000	
	VDDi	100	

AC and DC Operating Conditions

Operation or timing that is not specified is illegal.To ensure proper operation, the device must be initialized properly.

Table 45: Recommended DC Operating Conditions

Symbol	LPDDR2-S4B			Power Supply	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core power 1	V
VDD2	1.14	1.20	1.30	Core power2	V
VDDCA	1.14	1.20	1.30	Input buffer power	V
VDDQ	1.14	1.20	1.30	I/O buffer power	V

Note : 1. V_{DD1} uses significantly less power than V_{DD2}.

Table 46: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current : For CA, CKE, CS#, CK, CK#; Any input 0V ≤ V_{IN} ≤ V_{DDCA}; (All other pins not under test = 0V)	I_L	-2	2	uA	1
VREF supply leakage current : V_{REFDQ}=V_{DDQ}/2, or V_{REFCA}=V_{DDCA}/2; (All other pins not under test = 0V)	I_{VREF}	-1	1	uA	2

Note : 1. Although DM is for input only, the DM leakage must match the DQ and DQS/DQS# output leakage specification.
2. The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

Table 47: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
IT temperature range	T_{CASE}	-40	+85	˚C
AT temperature range		-40	+105	˚C

Note : 1. Operating temperature is the case surface temperature at the center of the top side of the device.
For measurement conditions, refer to the JESD51-2 standard.

2. Some applications require operation in the maximum case temperature range, between 85˚C and 105˚C. For some LPDDR2 devices, derating may be necessary to operate in this range (see the MR4 Device Temperature (MA[7:0] = 04h) table).
3. Either the device operating temperature or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor (page 47)). When using the temperature sensor, the actual device case temperature may be higher than the T_{CASE} rating that applies for the operating temperature range. For example, T_{CASE} could be above 85˚C when the temperature sensor indicates a temperature of less than 85˚C.

AC and DC Logic Input Measurement Levels for Single-Ended Signals

Table 48: Single-Ended AC and DC Input Levels for CA and CS# Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	notes
		Min	Max	Min	Max		
$V_{IHCA(AC)}$	AC input logic HIGH	V_{REF}+0.220	Note 2	V_{REF}+0.300	Note 2	V	1,2
$V_{ILCA(AC)}$	AC input logic LOW	note 2	V_{REF}-0.220	note 2	V_{REF}-0.300	V	1,2
$V_{IHCA(DC)}$	DC input logic HIGH	V_{REF}+0.130	V_{DDCA}	V_{REF}+0.200	V_{DDCA}	V	1
$V_{ILCA(DC)}$	DC input logic LOW	V_{SSCA}	V_{REF}-0.130	V_{SSCA}	V_{REF}-0.200	V	1
VREFCA(DC)	Reference voltage for CA and CS# inputs	0.49 × VDDCA	0.51 × VDDCA	0.49 × VDDCA	0.51 × VDDCA	V	3, 4

Note : 1. For CA and CS# input-only pins. VREF = VREFCA(DC).
2. See Figure 65.
3. The AC peak noise on VREFCA could prevent VREFCA from deviating more than ±1% VDDCA from VREFCA(DC) (for reference, approximately ±12mV).
4. For reference, approximately VDDCA/2 ±12mV.

Table 49: Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	notes
V_{IHCKE}	CKE input HIGH level	0.8 X VDDCA	Note 1	V	1
V_{ILCKE}	CKE input LOW level	Note 1	0.2 X VDDCA	V	1

Note : 1. See Figure 65.

Table 50: Single-Ended AC and DC Input Levels for DQ and DM

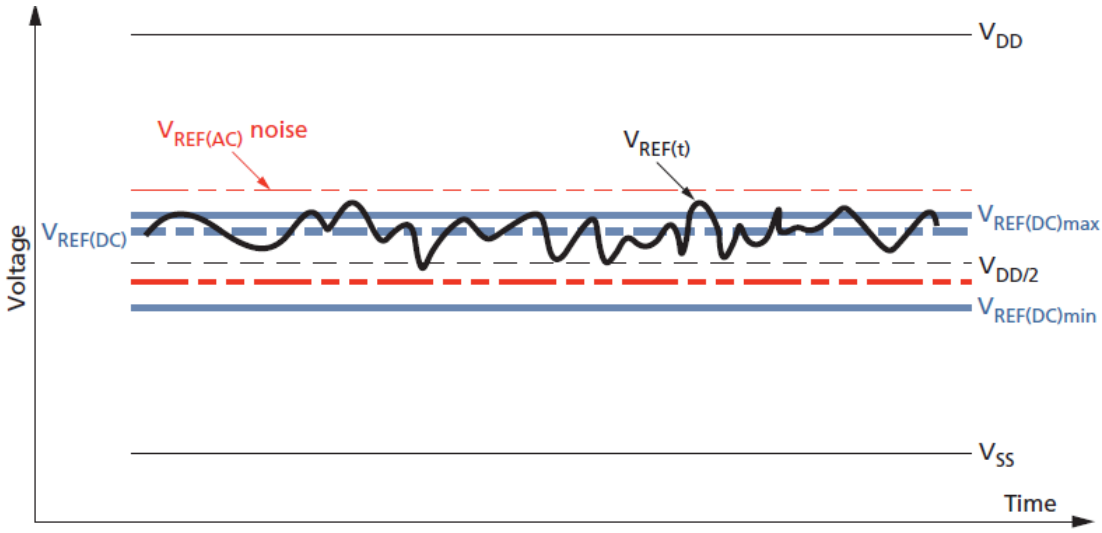
Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	notes
		Min	Max	Min	Max		
VIHDQ(AC)	AC input logic HIGH	VREF+0.220	Note 2	VREF+0.300	Note 2	V	1,2
VILDQ(AC)	AC input logic LOW	note 2	VREF-0.220	Note 2	VREF-0.300	V	1,2
VIHDQ(DC)	DC input logic HIGH	VREF+0.130	VDDQ	VREF+0.200	VDDQ	V	1
VILDQ(DC)	DC input logic LOW	VSSQ	VREF-0.130	VSSQ	VREF-0.200	V	1
VREFDQ(DC)	Reference voltage for DQ and DM inputs	0.49 X VDDQ	0.51X VDDQ	0.49 X VDDQ	0.51 X VDDQ	V	3, 4

Note : 1. For DQ input-only pins. V_{REF} = $V_{REFDQ(DC)}$.
2. See Figure 65.
3. The AC peak noise on V_{REFDQ} could prevent V_{REFDQ} from deviating more than ±1% V_{DDQ} from $V_{REFDQ(DC)}$ (for reference, approximately ±12mV).
4. For reference, approximately. V_{DDQ}/2 ±12mV.

VREF Tolerances

The DC tolerance limits and AC noise limits for the reference voltages VREFCA and VREFDQ are illustrated below.
This figure shows a valid reference voltageVREF(t) as a function of time.VDD is used in place ofVDDCA forVREFCA, and VDDQ for VREFDQ. VREF(DC) is the linear average ofVREF(t) over a very long period of time (for example, 1 second) and is specified as a fraction of the linear average ofVDDQ orVDDCA, also over a very long period of time (for example, 1 second).This average must meet the MIN/MAX requirements in Table 48. Additionally,VREF(t) can temporarily deviate from VREF(DC) by no more than ±1%VDD. VREF(t) cannot track noise onVDDQ orVDDCA if doing so would forceVREF outside these specifications.

Figure 56: V_{REF} DC Tolerance and V_{REF} AC Noise Limits



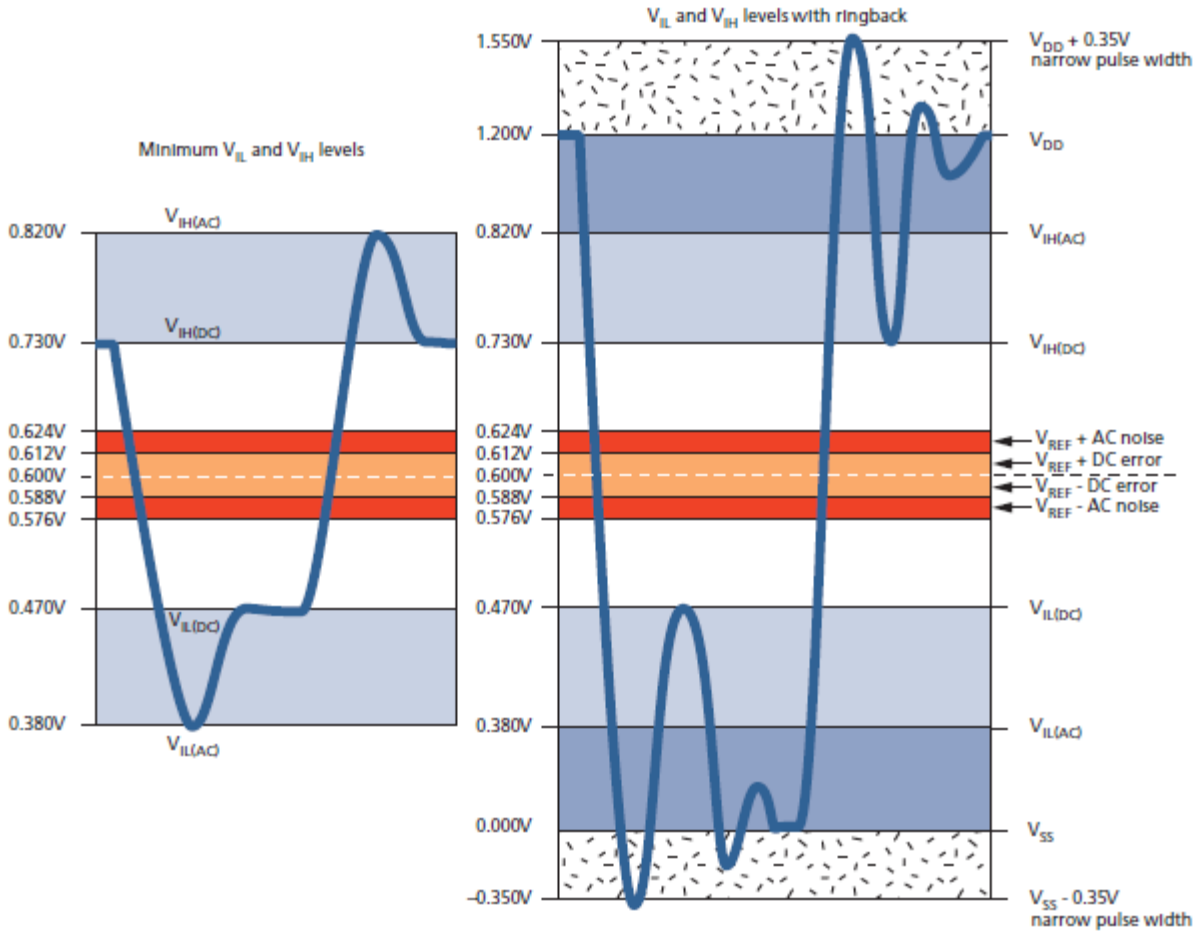
The voltage levels for setup and hold time measurementsVIH(AC),VIH(DC),VIL(AC), and VIL(DC) are dependent onVREF. VREF DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When VREF is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

- VREF is maintained between 0.44 xVDDQ (orVDDCA) and 0.56 xVDDQ (orVDDCA), *and*
- the controller achieves the required single-ended AC and DC input levels from instantaneous VREF (see Table).

System timing and voltage budgets must account forVREF deviations outside this range. The setup/hold specification and derating values must include time and voltage associated withVREF AC noise. Timing and voltage effects due to AC noise onVREF up to the specified limit (±1%VDD) are included in LPDDR2 timings and their associated deratings.

Input Signal

Figure 57: LPDDR2-466 to LPDDR2-1066 Input Signal

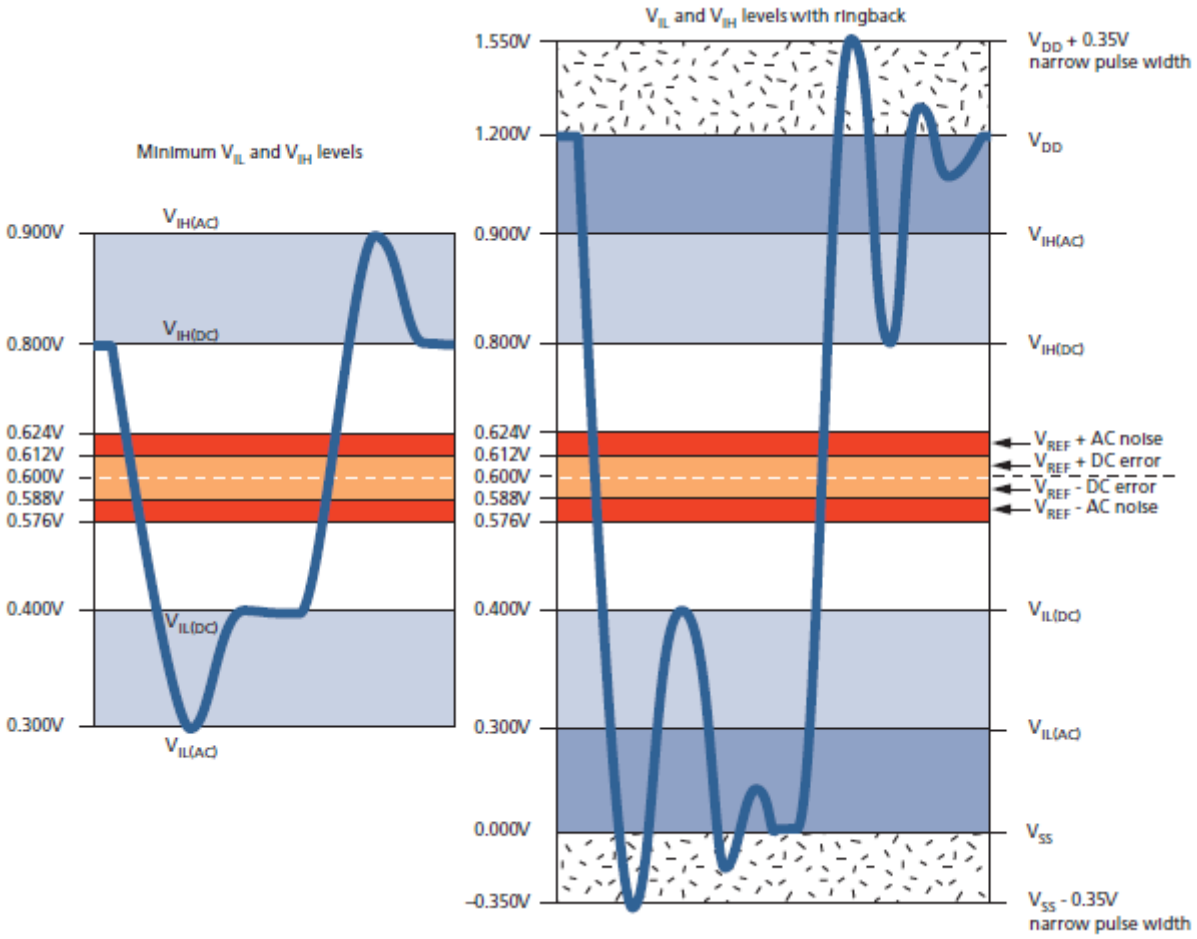


Notes : 1. Numbers reflect typical values.

2. For CA[9:0], CK, CK#, and CS# V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and DQS#, V_{DD} stands for V_{DDQ}.

3. For CA[9:0], CK, CK#, and CS# V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and DQS#, V_{SS} stands for V_{SSQ}.

Figure 58: LPDDR2-200 to LPDDR2-400 Input Signal



Notes : 1. Numbers reflect typical values.

2. For CA[9:0], CK, CK#, and CS# V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and DQS#, V_{DD} stands for V_{DDQ}.

3. For CA[9:0], CK, CK#, and CS# V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and DQS#, V_{SS} stands for V_{SSQ}.

Figure 59: Differential AC Swing Time and tDVAC

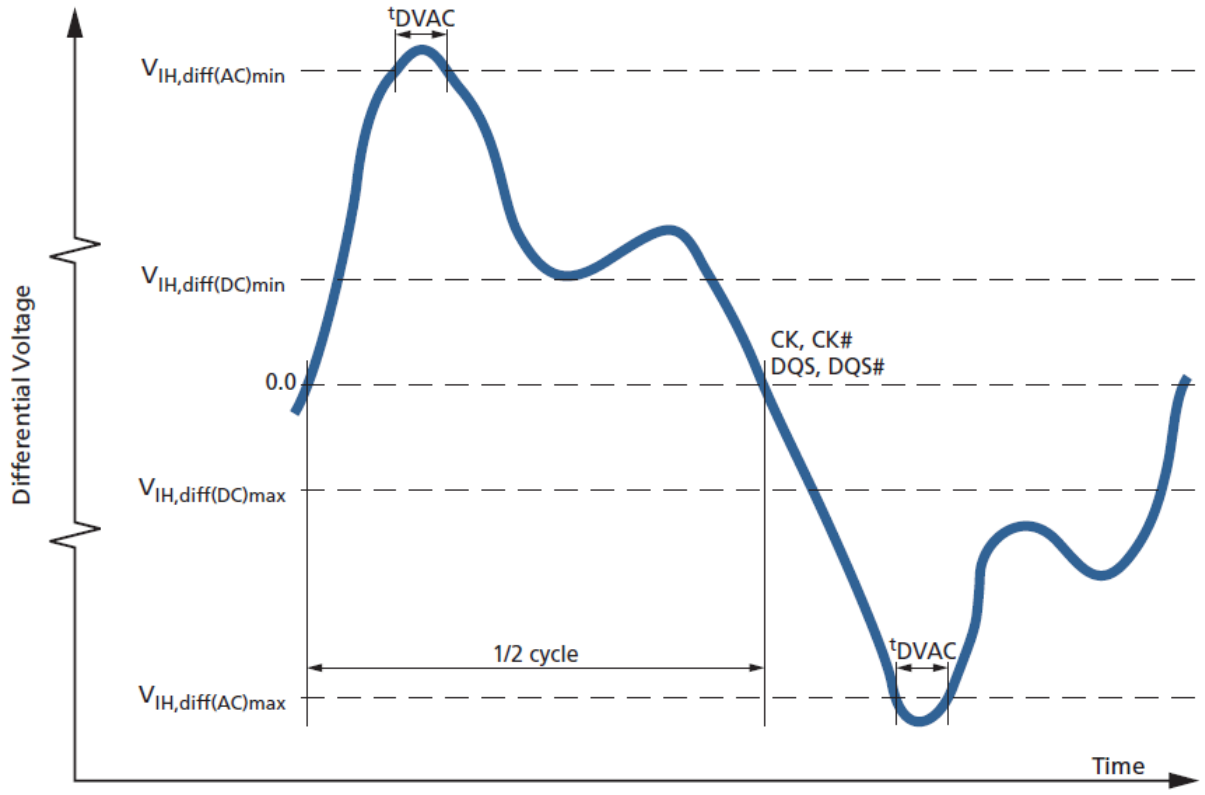


Table 51: Differential AC and DC Input Levels

For CK and CK#, $V_{REF} = V_{REFCA(DC)}$; For DQS and DQS# $V_{REF} = V_{REFDQ(DC)}$

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	notes
		Min	Max	Min	Max		
$V_{IH,diff(AC)}$	Differential input HIGH AC	2 × ($V_{IH(AC)}$ - V_{REF})	note1	2 × ($V_{IH(AC)}$ - V_{REF})	note1	V	2
$V_{IL,diff(AC)}$	Differential input LOW AC	note 1	2 × ($V_{IH(AC)}$ – V_{REF})	note 1	2 × (V_{REF} - $V_{IL(AC)}$)	V	2
$V_{IH,diff(DC)}$	Differential input HIGH	2 × ($V_{IH(DC)}$ - V_{REF})	note 1	2 × ($V_{IH(DC)}$ - V_{REF})	note 1	V	3
$V_{IL,diff(DC)}$	Differential input LOW	note1	2 × (V_{REF} - $V_{IL(DC)}$)	note1	2 × (V_{REF} - $V_{IL(DC)}$)	V	3

Notes : 1. These values are not defined, however the single-ended signals CK, CK#, DQS, and DQS# must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals and must comply with the specified limitations for overshoot and undershoot (see Figure 65).

2. For CK and CK#, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS and DQS#, use $V_{IH}/V_{IL(AC)}$ of DQ and V_{REFDQ}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.

3. Used to define a differential signal slew rate.

Table 52: CK/CK# and DQS/DQS# Time Requirements Before Ringback (tDVAC)

Slew Rate (V/ns)	tDVAC(ps) at $V_{IH}/V_{ILdiff(AC)}$ = 440mV	tDVAC(ps) at $V_{IH}/V_{ILdiff(AC)}$ = 600mV
	Min	Min
>4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
<1.0	150	0

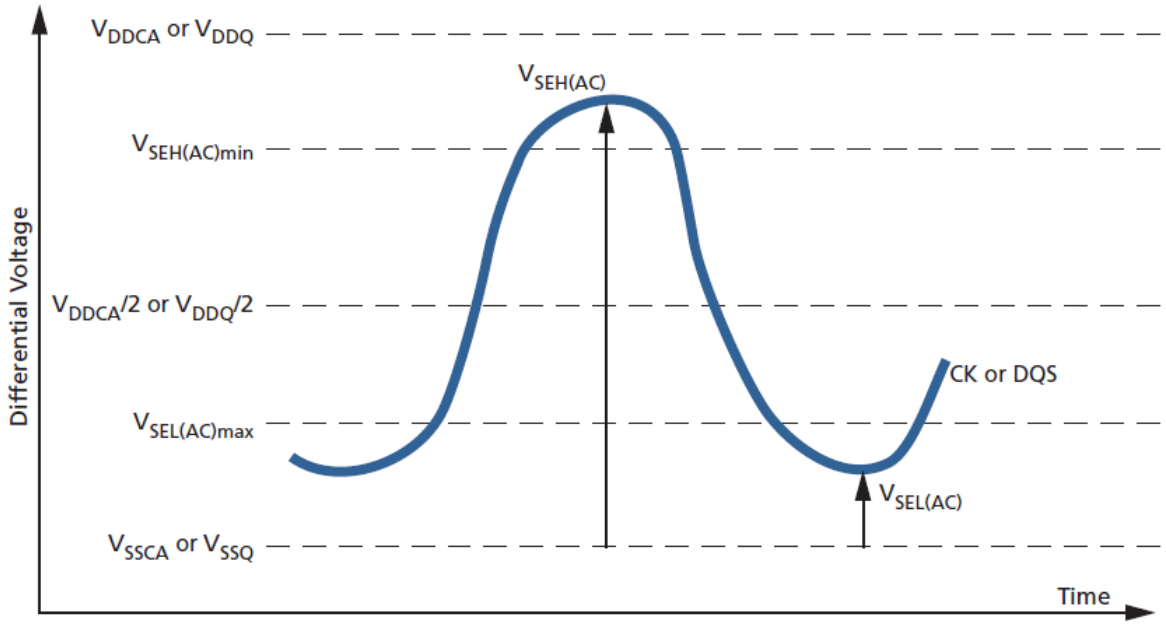
Single-Ended Requirements for Differential Signals

Each individual component of a differential signal(CK, CK#, DQS, and DQS#) must also comply with certain requirements for single-ended signals.

CK and CK# must meetVSEH(AC)min/VSEL(AC)max in every half cycle. DQS, DQS# must meet VSEH(AC)min/VSEL(AC)max in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed bin.

Figure 60: Single-Ended Requirements for Differential Signals



Note that while CA and DQ signal requirements are referenced toVREF, the single-ended components of differential signals also have a requirement with respect to VDDQ/2 for DQS, andVDDCA/2 for CK.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach VSEL(AC)max orVSEH(AC)min has no bearing on timing.This requirement does, however, add a restriction on the common mode characteristics of these signals (see Table 48) for CK/CK# single-ended requirements, and Table 48 for DQ and DQM single-ended requirements).

Table 53: Single-Ended Levels for CK, CK#, DQS, DQS#

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	(V_{DDQ}/2)+0.220	note1	(V_{DDQ}/2)+0.300	note1	V	2,3
	Single-ended HIGH level for CK, CK#	(V_{DDCA}/2)+0.220	note1	(V_{DDCA}/2)+0.300	note1	V	2,3
$V_{SEL(AC)}$	Single-ended LOW level for strobes	note1	(V_{DDQ}/2)-0.220	note1	(V_{DDQ}/2)+0.300	V	2,3
	Single-ended LOW level for CK, CK#	note1	(V_{DDCA}/2)-0.220	note1	(V_{DDCA}/2)+0.300	V	2,3

Notes : 1. These values are not defined, however, the single-ended signals CK, CK#, DQS0, DQS#0, DQS1, DQS#1, DQS2, DQS#2, DQS3, DQS#3 must be within the respective limits($V_{IH(DC)max}$/ $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot (see Figure 65).

2. For CK and CK#, use V_{SEH}/$V_{SEL(AC)}$ of CA; for strobes (DQS[3:0] and DQS#[3:0]), use V_{IH}/$V_{IL(AC)}$ of DQ.
3. $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ}; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA}.
   If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.

Differential Input Crosspoint Voltage

To ensure tight setup and hold times as well as output skew parameters with respect to clock and strobe, each crosspoint voltage of differential input signals (CK, CK#, DQS, and DQS#) must meet the specifications in Table 53.

The differential input crosspoint voltage **(**VIX**)** is measured from the actual crosspoint of the true signal and its and complement to the midlevel between VDD and VSS.

Figure 61: VIX Definition

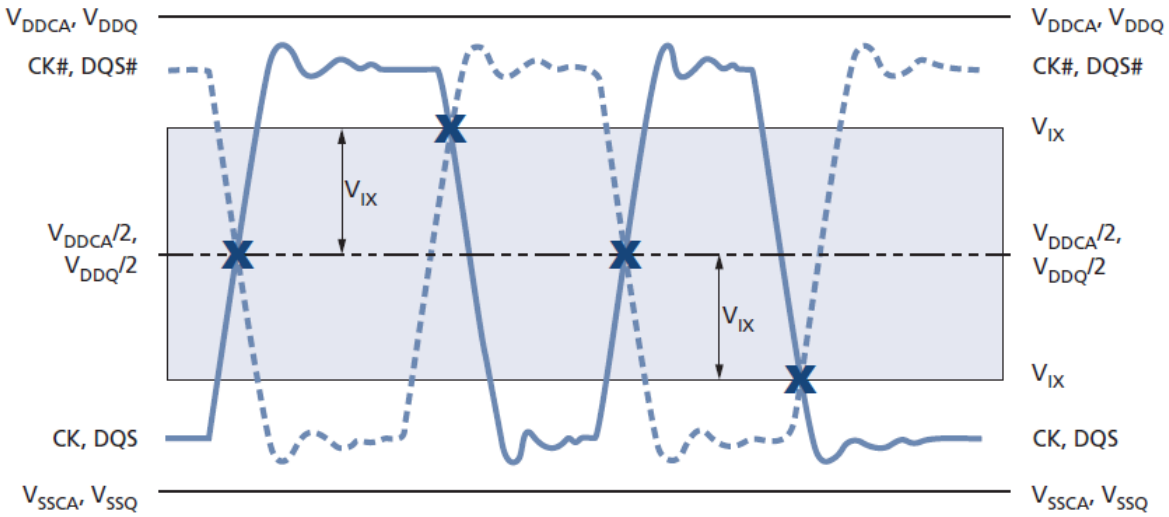


Table 54: Crosspoint Voltage for Differential Input Signals (CK, CK#, DQS, DQS#)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	notes
		Min	Max		
$V_{IXCA(AC)}$	Differential input cross point voltage relative to V_{DDCA}/2 for CK and CK#	-120	120	mV	1,2
$V_{IXDQ(AC)}$	Differential input cross point voltage relative to V_{DDQ}/2 for DQS and DQ#	-120	120	mV	1,2

Notes : 1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and it is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

2. For CK and CK#, V_{REF} = $V_{REFCA(DC)}$. For DQS and DQS#, V_{REF} = $V_{REFDQ(DC)}$.

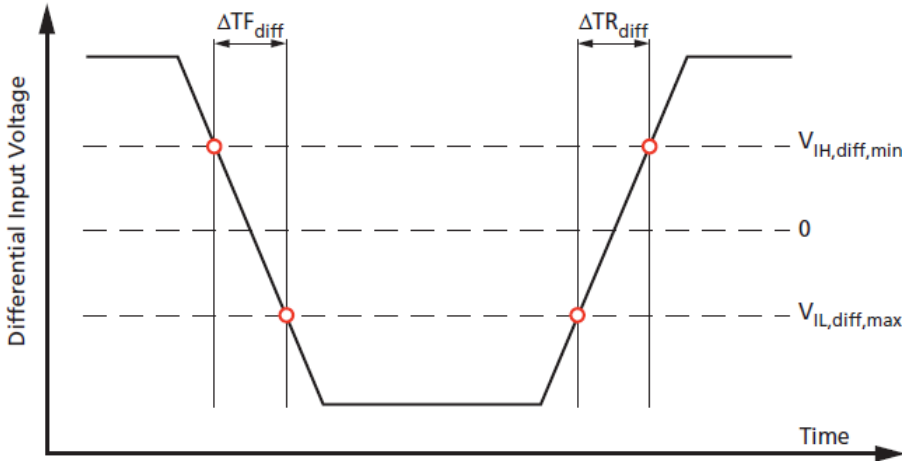
Input Slew Rate

Table 55: Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK/CK# and DQS/DQS#)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK/CK# and DQS/DQS#)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TF_{diff}$

Note : 1. The differential signals (CK/CK# and DQS/DQS#) must be linear between these thresholds.

Figure 62: Differential Input Slew Rate Definition for CK, CK#, DQS, and DQS#



Output Characteristics and Operating Conditions

Table 56: Single-Ended AC and DC Output Levels

Symbol	Parameter		Value	Unit	Notes
$V_{OH(AC)}$	AC output HIGH measurement level(for output slew rate)		VREF+0.12	V	
$V_{OL(AC)}$	AC output LOW measurement level(for output slew rate)		VREF-0.12	V	
$V_{OH(DC)}$	DC output HIGH measurement level(for I-V curve linearity)		0.9 x VDDQ	V	1
$V_{OL(DC)}$	DC output LOW measurement level(for I-V curve linearity)		0.1 x VDDQ	V	2
I_{OZ}	Output leakage current (DQ, DM, DQS, DQS#); DQ, DQS, DQS# are disabled; 0V ≤ VOUT ≤ VDDQ	MIN	-5	uA	
		MAX	+5	uA	
MMpupd	Delta output impedance between pull-up and pull-down for DQ/DM	MIN	-15	%	
		MAX	+15	%	

Notes : 1. IOH = -0.1mA
2. IOL = 0.1mA

Table 57: Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit
$V_{OHdiff(AC)}$	AC differential output HIGH measurement level(for output SR)	+0.2 x V_{DDQ}	V
$V_{OLdiff(AC)}$	AC differential output LOW measurement level(for output SR)	-0.2 x V_{DDQ}	V

Single-Ended Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single-ended signals.

Table 58: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / ΔTR_{SE}
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / ΔTF_{SE}

Note : 1. Output slew rate is verified by design and characterization and may not be subject to production testing.

Figure 63: Single-Ended Output Slew Rate Definition

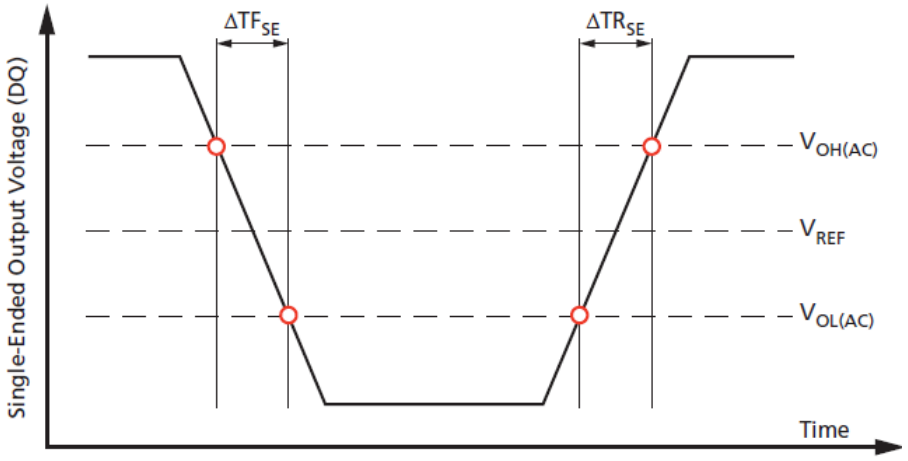


Table 59: Single-Ended Output Slew Rate

Notes 1–5 apply to all parameters conditions

Parameter	Symbol	Value		Unit
		Min	Max	
single-ended output slew rate(output impedance=40Ω±30%)	SRQ_{SE}	1.5	3.5	V/ns
single-ended output slew rate(output impedance=60Ω±30%)	SRQ_{SE}	1.0	2.5	V/ns
Output slew-rate-matching ratio(pull-up to pull-down		0.7	1.4	-

Notes : 1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
2. Measured with output reference load.

3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
5. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

Differential Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL,diff(AC) and VOH, diff(AC) for differential signals.

Table 60: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,\ diff(AC)} - V_{OL,\ diff(AC)}] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,\ diff(AC)} - V_{OL,\ diff(AC)}] / \Delta TF_{diff}$

Note : 1. Output slew rate is verified by design and characterization and may not be subject to production testing.

Figure 64: Differential Output Slew Rate Definition

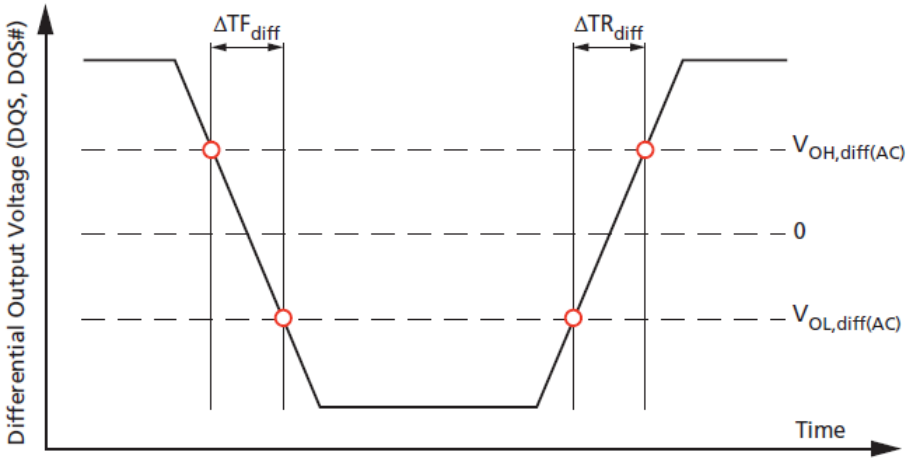


Table 61: Differential Output Slew Rate

Parameter	Symbol	Value		Unit
		Min	Max	
Differential output slew rate(output impedance=40Ω±30%)	SRQdiff	3.0	7.0	V/ns

Table 62: Differential Output Slew Rate (Continued)

Parameter	Symbol	Value		Unit
		Min	Max	
Differential output slew rate(output impedance=60Ω±30%)	SRQdiff	2.0	5.0	V/ns

Notes : 1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

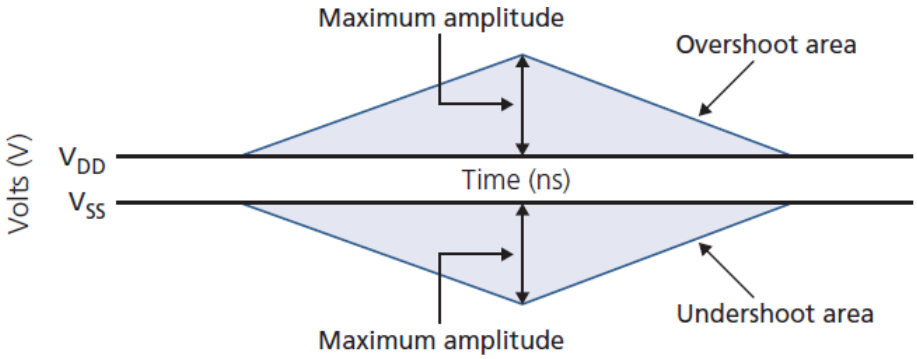
Table 63: AC Overshoot/Undershoot Specification

Applies for CA[9:0], CS#, CKE, CK, CK#, DQ, DQS, DQS#, DM

Parameter	1066	933	800	667	533	400	333	Unit
Maximum peak amplitude provided for overshoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum area above V_{DD}	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V/ns
Maximum area below V_{SS}	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V/ns

Notes : 1. V_{DD} stands for V_{DDCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, DQS, and DQS#.
2. V_{SS} stands for V_{SSCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, DQS, and DQS#.

Figure 65: Overshoot and Undershoot Definition

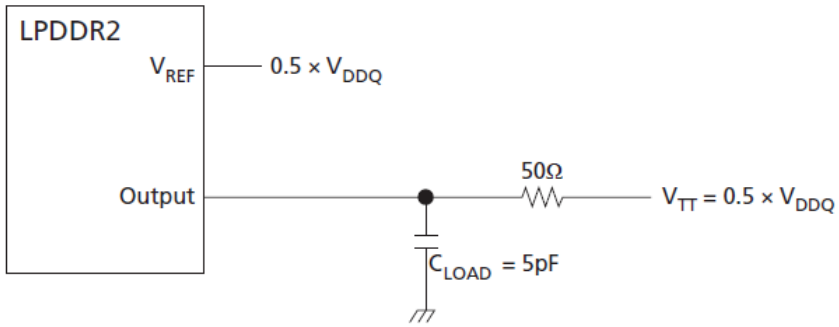


Notes : 1. V_{DD} stands for V_{DDCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, DQS, and DQS#.
2. V_{SS} stands for V_{SSCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, DQS, and DQS#.

HSUL_12 Driver Output Timing Reference Load

The timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally with one or more coaxial transmission lines terminated at the tester electronics.

Figure 66: HSUL_12 Driver Output Reference Load for Timing and Slew Rate



Note : 1. All output timing parameter values (tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Output Driver Impedance

Output driver impedance is selected by a mode register during initialization. To achieve tighter tolerances, ZQ calibration is required. Output specifications refer to the default output drive unless specifically stated otherwise.The output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

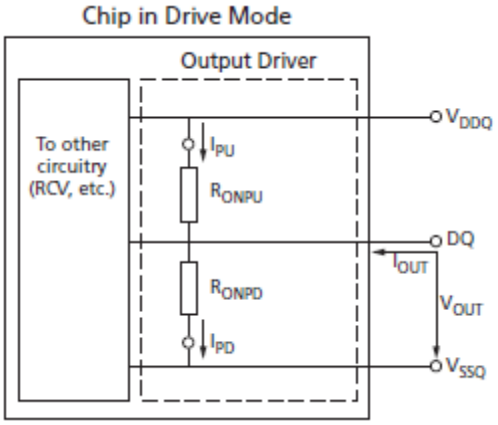
$$R_{ONPU} = \frac{VDDQ - VOUT}{ABS(I_{OUT})}$$

When RONPD is turned off.

$$R_{ONPD} = \frac{V_{OUT}}{ABS(I_{OUT})}$$

When RONPU is turned off.

Figure 67: Output Driver



Output Driver Impedance Characteristics with ZQ Calibration

Output driver impedance is defined by the value of the external reference resistor RZQ. Typical RZQ is 240 ohms.

Table 67: Output Driver DC Electrical Characteristics with ZQ Calibration

Notes 1–4 apply to all parameters and conditions

R_{ONnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit	notes
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	
	R_{ON34PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	
	R_{ON40PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	
	R_{ON48PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	
60.0Ω	R_{ON60PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/4	
	R_{ON60PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/4	
80.0Ω	R_{ON80PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/3	
	R_{ON80PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/3	
120.0Ω	$R_{ON120PD}$	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/2	
	$R_{ON120PU}$	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/2	
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	5

Notes : 1. Applies across entire operating temperature range after calibration.

2. RZQ=240Ω
3. The tolerance limits are specified after calibration, with fixed voltage and temperature.
4. For behavior of the tolerance limits if temperature or voltage changes after calibration.
5. Pull-down and pull-up output driver impedances should be calibrated at 0.5 x V_{DDQ}.
6. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}:
   Measure R_{ONPU} and R_{ONPD}, both at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

For example, with MM_{PUPD} (MAX) = 15% and R_{ONPD} = 0.85, RON_{PU} must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen.

Table 68: Output Driver Sensitivity Definition

Resistor	V_{OUT}	Min	Max	Unit
R_{ONPD}	0.5 × V_{DDQ}	85-($dR_{ON}dT \cdot \lvert\Delta T\rvert$)-($dR_{ON}dV \cdot \lvert\Delta V\rvert$)	115-($dR_{ON}dT \cdot \lvert\Delta T\rvert$)-($dR_{ON}dV \cdot \lvert\Delta V\rvert$)	%
R_{ONPU}				

Notes : 1. $\Delta T = T - T$ (at calibration). $\Delta V = V - V$ (at calibration).

2. $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production testing; they are verified by design and characterization.

Table 69: Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	V_{OUT}	Min	Max	Unit
R_{ONPD}	R_{ON} temperature sensitivity	0.5 × V_{DDQ}	0.00	0.75	%/˚C
R_{ONPU}	R_{ON} voltage sensitivity	0.5 × V_{DDQ}	0.00	0.20	%/mV

Output Impedance Characteristics Without ZQ Calibration

Output driver impedance is defined by design and characterization as the default setting.

Table 70: Output Driver DC Electrical Characteristics Without ZQ Calibration

R_{ONnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/7
	R_{ON34PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/7
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/6
	R_{ON40PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/6
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/5
	R_{ON48PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/5
60.0Ω	R_{ON60PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/4
	R_{ON60PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/4
80.0Ω	R_{ON80PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/3
	R_{ON80PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/3
120.0Ω	$R_{ON120PD}$	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/2
	$R_{ON120PU}$	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/2

Notes : 1. Applies across entire operating temperature range without calibration.

2. R_{ZQ}=240Ω

Table 71: I-V Curves

Voltage	R_{ON}=240Ω(R_{ZQ})							
	Pull-Down				Pull-Up			
	Current(mA) / R_{ON}(ohms)				Current(mA) / R_{ON}(ohms)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
	Min(mA)	Max(mA)	Min(mA)	Max(mA)	Min(mA)	Max(mA)	Min(mA)	Max(mA)
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

Figure 68 : Output Impedance = 240 Ohms, I-V Curves After ZQRESET

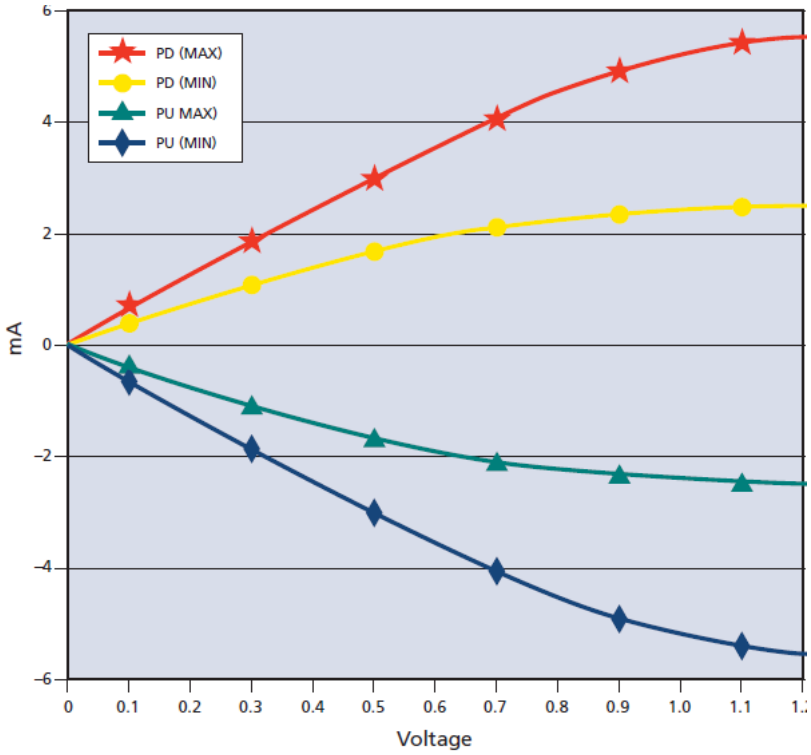
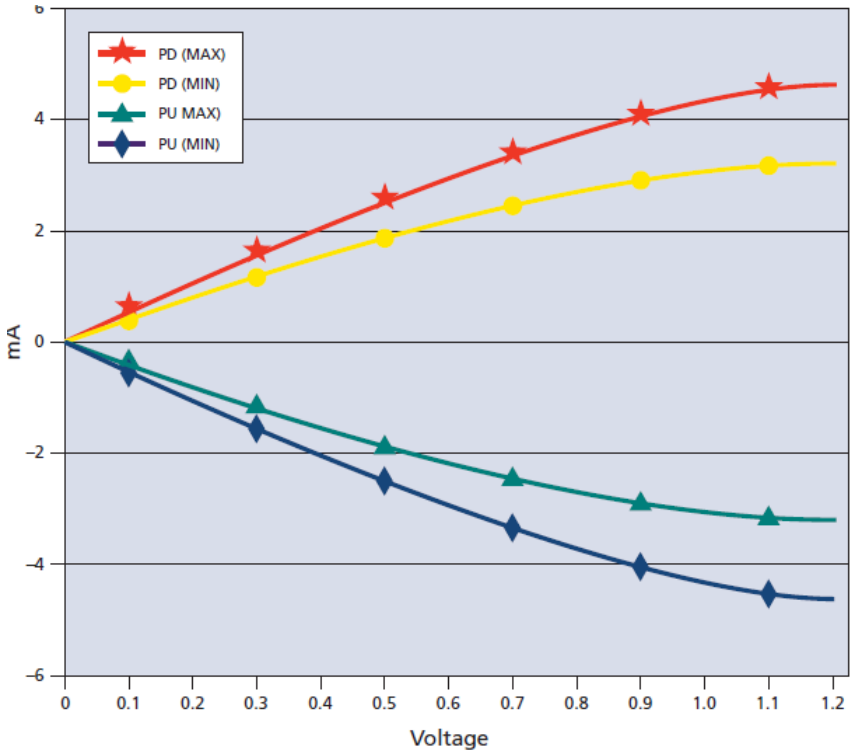


Figure 69: Output Impedance = 240 Ohms, I-V Curves After Calibration



Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 72: Definitions and Calculations

Symbol	Description	Calculation	Notes
tCK(avg) and nCK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit tCK(avg) represents the actual clock average tCK (avg) of the input clock under operation. Unit nCK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. tCK (avg) can change no more than ±1% within a 100clock cycle window, provided that all jitter and timing specifications are met.	$tCK(avg) = \left(\sum_{j=1}^{N} tCKj\right) / N$ Where N = 200	
tCK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
tCH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$tCH(avg) = \left(\sum_{j=1}^{N} tCHj\right) / (N \times tCK(avg))$ Where N = 200	
tJIT(per)	The single-period jitter defined as the largest deviation of any signal tCK from tCK(avg).	$tCL(avg) = \left(\sum_{j=1}^{N} tCLj\right) / (N \times tCK(avg))$ Where N = 200	
tJIT(per), act	The actual clock jitter for a given system.	tJIT(per) = min/max of (tCKi – tCK(avg)) Where i = 1 to 200	
tJIT(per), allowed	The specified clock period jitter allowance.		
tJIT(CC)	The absolute difference in clock periods between two consecutive clock cycles. tJIT(cc) defines the cycle-to-cycle jitter.	$tJIT(cc) = \max \text{ of } (tCK_{i+1} - tCKi)$	1
tERR(nper)	The cumulative error across n multiple consecutive cycles from tCK(avg).	$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCKj\right) - (N \times tCK(avg))$	1
tERR(nper), act	The actual cumulative error over n cycles for a given system.		
tERR(nper), allowed	The specified cumulative error allowance over n cycles.		
tERR(nper), min	The minimum tERR(nper).	tERR(nper),min = (1 + 0.68LN(n)) × tJIT(per),min	2

Table 73: Definitions and Calculations (Continued)

Symbol	description	Calculation	Notes
tERR(nper), max	The maximum tERR(nper).	tERR(nper),max = (1 + 0.68LN(n)) × tJIT(per),max	2
tJIT(duty)	Defined with absolute and average specifications for tCH and tCL, respectively.	tJIT(duty),min = MIN((tCH(abs),min – tCH(avg),min), (tCL(abs),min – tCL(avg),min)) × tCK(avg) tJIT(duty),max = MAX((tCH(abs),max – tCH(avg),max), (tCL(abs),max – tCL(avg),max)) × tCK(avg)	

Notes : 1. Not subject to production testing.

2. Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

tCK(abs), tCH(abs), and tCL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Table 74: tCK(abs), tCH(abs), and tCL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min + tJIT(duty),min2/tCK(avg)min	tCK(avg)
Absolute clock LOW width	tCL(abs)	tCL(avg),min + tJIT(duty),min2/tCK(avg)min	tCK(avg)

Notes : 1. tCK(avg),min is expressed in ps for this table.

2. tJIT(duty),min is a negative value.

Clock Period Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (tJIT(per)) in excess of the values found in the ACTiming section. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles.Within the specification limits, the device is characterized and verified to support t*n*PARAM = RU[tPARAM/tCK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks or tCK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (t*nPARAM), when tCK(avg) and tERR(tnPARAM),act exceed* tERR(t*nPARAM),allowed, cycle time derating may be required for core timing parameters.*

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{t\text{PARAM} + t\text{ERR}(t\text{nPARAM}),\text{act} - t\text{ERR}(t\text{nPARAM}),\text{allowed}}{t\text{nPARAM}} - t\text{CK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (t*nPARAM), clock cycle* derating should be specified with tJIT(per). For a given number of clocks (t*nPARAM), when tCK(avg) plus (tERR(tnPARAM),act) exceed* the supported cumulative tERR (t*nPARAM),allowed, derating is required. If the* equation below results in a positive value for a core timing parameter (tCORE), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{{}^{t}\text{PARAM} + {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{allowed}}{{}^{t}\text{CK(avg)}}\right\} - {}^{t}\text{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb) are measured from a command / address signal (CKE, CS, or CA[9:0]) transition edge to its respective clock signal (CK/CK#) crossing.

The specification values are not affected by the tJIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

tRPRE

When the device is operated with input clock jitter, tRPRE must be derated by the tJIT(per),act,max of the input clock that exceeds tJIT(per),allowed,max. Output deratings are relative to the input clock :

$${}^{t}\text{RPRE(min,derated)} = 0.9 - \left(\frac{{}^{t}\text{JIT(per),act,max} - {}^{t}\text{JIT(per),allowed,max}}{{}^{t}\text{CK(avg)}}\right)$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500ps, tJIT(per), act, min = –172ps, and tJIT(per), act, max= +193ps, then tRPRE, min, derated =0.9 - (tJIT(per), act, max - tJIT(per), allowed, max)/tCK(avg) = 0.9 – (193 - 100)/2500 =0.8628 tCK(avg).

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DM*n* or DQ*m*, where: *n* = 0, 1, 2, or 3; and *m* = DQ[31:0]), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by tJIT(per).

tQSH, tQSL

These parameters are affected by duty cycle jitter, represented by tCH(abs)min and tCL(abs)min. These parameters determine the absolute data valid window at the device pin. The absolute minimum data valid window at the device pin = min [(tQSH(abs)min × tCK(avg)min - tDQSQmax - tQHSmax), (tQSL(abs)min × tCK(avg)min - tDQSQmax -tQHSmax)]. This minimum data valid window must be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter, represented by tCL(abs). Therefore, tRPST(abs)min can be specified by tCL(abs)min. tRPST(abs)min = tCL(abs)min - 0.05 = tQSL(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

tDS, tDH

These parameters are measured from a data signal (DM*n* *or* DQ*m*, where *n* = 0, 1, 2, 3; and *m* = DQ[31:0]) transition edge to its respective data strobe signal (DQS*n*, DQS*n*#: *n* = 0,1,2,3) crossing. The specification values are not affected by the amount of tJIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

tDSS, tDSH

These parameters are measured from a data strobe signal crossing (DQS*x*, DQS*x*#) to its clock signal crossing (CK/CK#).
The specification values are not affected by the amount of tJIT(per)) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

tDQSS

tDQSS is measured from the clock signal crossing (CK/CK#) to the first latching data strobe signal crossing (DQS*x, DQSx#). When the device is operated with input clock jitter,* this parameter must be derated by the actual tJIT(per),act of the input clock in excess of tJIT(per),allowed.

$$t_{DQSS(min,derated)} = 0.75 - \left(\frac{t_{JIT(per),act,min} - t_{JIT(per),allowed,min}}{t_{CK(avg)}}\right)$$

$$t_{DQSS(max,derated)} = 1.25 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}}\right)$$

For example,
if the measured jitter into an LPDDR2-800 device has tCK(avg)=2500ps, tJIT(per) ,act, min=-172ps, and tJIT(per), act, max=+193ps, then : tDQSS,(min, derated)=0.75 - (tJIT(per), act, min - tJIT(per), allowed, min)/tCK(avg)=0.75 - (-172 + 100)/2500=0.7788 tCK(avg), *and* tDQSS,(max, derated)=1.25 - (tJIT(per), act, max - tJIT(per), allowed, max)/tCK(avg)=1.25 - (193 - 100)/2500=1.2128 tCK(avg).

Refresh Requirements

Table 75: Refresh Requirement Parameters (Per Density)

Parameter		Symbol	64Mb	128Mb	256Mb	512Mb	1Gb	2Gb	4Gb	8Gb	Unit
Number of banks			4	4	4	4	8	8	8	8	
Refreshwindow:TCASE≤85˚		tREFW	32	32	32	32	32	32	32	32	ms
Refresh window 85˚C<TCASE≤105˚C		tREFW	8	8	8	8	8	8	8	8	ms
Required number of REFRESH command(MIN)		R	2048	2048	4096	4096	4096	8192	8192	8192	
Average time between REFRESH commands (for reference only) TCASE ≤ 85˚C	REFab	tREFI	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	us
	REFpb	tREFIpb	(REFpb not supported below 1Gb)				0.9750	0.4875	0.4875	0.4875	us
Refresh cycle time		tRFCab	90	90	90	90	130	130	130	210	ns
Per-bank REFRESH cycle time		tRFCpb	na				60	60	60	90	ns
Burst REFRESH window = 4 × 8 × tRFCab		tREFBW	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	us

Table 77: AC Timing

Notes 1–2 apply to all parameters and conditions.

AC timing parameters must satisfy the tCK minimum conditions(in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min / Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Maximum frequency		-	-	533	466	400	333	266	200	166	MHz	
Clock timing												
Average clock period	tCK (avg)	MIN	-	1.875	2.15	2.5	3	3.75	5	6	ns	
		MAX	-	-	-	-	-	-	-	-		
Average HIGH pulse width	tCH (avg)	MIN	-	0.45	0.45	0.45	0.45	0.45	0.45	0.45	tCK (avg)	
		MAX	-	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Average LOW pulse width	tCL (avg)	MIN	-	0.45	0.45	0.45	0.45	0.45	0.45	0.45	tCK (avg)	
		MAX	-	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Absolute clock period	tCK (abs)	MIN	-	tCK(avg)min ± JIT(per)min							ps	
Absolute clock HIGH pulse width	tCH (abs)	MIN	-	0.43	0.43	0.43	0.43	0.43	0.43	0.43	tCK (avg)	
		MAX	-	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Absolute clock LOW pulse width	tCL (abs)	MIN	-	0.43	0.43	0.43	0.43	0.43	0.43	0.43	tCK (avg)	
		MAX	-	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Clock period jitter (with supported jitter)	tJIT(per), allowed	MIN	-	-90	-95	-100	-110	-120	-140	-150	ps	
		MAX	-	90	95	100	110	120	140	150		
Maximum clock jitter between two consecutive clock cycles (with supported jitter)	tJIT(cc), allowed	MAX	-	180	190	200	220	240	280	300	ps	
Duty cycle jitter (with supported jitter)	JIT(duty), allowed	MIN	-	MIN ((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) × tCK(avg)							ps	
		MAX	-	MAX ((tCH(abs),max - tCH(avg), max), (tCL(abs),max - tCL(avg), max)) × tCK(avg)								
Cumulative errors across 2cycles	ERR(2per), allowed	MIN	-	-132	-140	-147	-162	-177	-206	-221	ps	
		MAX	-	132	140	147	162	177	206	221		
Cumulative errors across 3cycles	ERR(3per), allowed	MIN	-	-157	-166	-175	-192	-210	-245	-262	ps	
		MAX	-	157	166	175	192	210	245	262		
Cumulative errors across 4cycles	ERR(4per), allowed	MIN	-	-175	-185	-194	-214	-233	-272	-291	ps	
		MAX	-	175	185	194	214	233	272	291		
Cumulative errors across 5cycles	ERR(5per), allowed	MIN	-	-188	-199	-209	-230	-251	-293	-314	ps	
		MAX	-	188	199	209	230	251	293	314		
Cumulative errors across 6cycles	ERR(6per), allowed	MIN	-	-200	-211	-222	-244	-266	-311	-333	ps	
		MAX	-	200	211	222	244	266	311	333		
Cumulative errors across 7cycles	ERR(7per), allowed	MIN	-	-209	-221	-232	-256	-279	-325	-348	ps	
		MAX	-	209	221	232	256	279	325	348		

Table 77: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions.

AC timing parameters must satisfy the tCK minimum conditions(in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min /Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Cumulative errors across 8 cycles	tERR(8per) allowed	MIN	-	-217	-229	-241	-266	-290	-338	-362	ps	
		MAX	-	217	229	241	266	290	338	362		
Cumulative errors across 9 cycles	tERR(9per) allowed	MIN	-	-224	-237	-249	-274	-299	-349	-374	ps	
		MAX	-	224	237	249	274	299	349	374		
Cumulative errors across 10 cycles	tERR(10per) allowed	MIN	-	-231	-244	-257	-282	-308	-359	-385	ps	
		MAX	-	-231	-244	-257	-282	-308	-359	-385		
Cumulative errors across 11 cycles	tERR(11per) allowed	MIN	-	-237	-250	-263	-289	-316	-368	-395	ps	
		MAX	-	237	250	263	289	316	368	395		
Cumulative errors across 12 cycles	tERR(12per) allowed	MIN	-	-242	-256	-269	-296	-323	-377	-403	ps	
		MAX	-	242	256	269	296	323	377	403		
Cumulative errors across n = 13,14,15,···, 49, 50 cycles	tERR(nper) allowed	MIN	-	tERR(nper), allowed, min = (1 + 0.68ln(n)) × tJIT(per),allowed, min							ps	
		MAX	-	tERR(nper), allowed, max = (1 + 0.68ln(n)) × tJIT(per), allowed, max								
ZQ Calibration Parameters												
Initialization calibration time	tZQINIT	MIN	-	1	1	1	1	1	1	1	us	
Long calibration time	tZQCL	MIN	6	360	360	360	360	360	360	360	ns	
Short calibration time	tZQCS	MIN	6	90	90	90	90	90	90	90	ns	
Calibration RESET time	tZQRESET	MIN	3	50	50	50	50	50	50	50	ns	
READ Parameter												
DQS output access Time from CK/CK#	tDQSCK	MIN	-	2500	2500	2500	2500	2500	2500	2500	ps	
		MAX	-	5500	5500	5500	5500	5500	5500	5500		
DQSCK delta short	tDQSCKDS	MAX	-	330	380	450	540	670	900	1080	ps	4
DQSCK delta medium	tDQSCKDM	MAX	-	680	780	900	1050	1350	1800	1900	ps	5
DQSCK delta long	tDQSCKDL	MAX	-	920	1050	1200	1400	1800	2400	-	ps	6
DQS-DQ skew	tDQSQ	MAX	-	200	220	240	280	340	400	500	ps	
Data-hold skew factor	tQHS	MAX	-	230	260	280	340	400	480	600	ps	
DQS output HIGH pulse width	tQSH	MIN	-	tCH(abs) - 0.05							tCK (avg)	
DQS output LOW pulse width	tQSL	MIN	-	tCL(abs) - 0.05							tCK (avg)	
DATA half period	tQHP	MIN	-	MIN (tQSH, tQSL)							tCK (avg)	
DQ/DQS output hold time from DQS	tQH	MIN	-	tQHP - tQHS							ps	

Table 78: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions.

AC timing parameters must satisfy the tCK minimum conditions(in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min / Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
READ preamble	tRPRE	MIN	-	0.9	0.9	0.9	0.9	0.9	0.9	0.9	tCK (avg)	
READ postamble	tRPST	MIN	-	tCL(abs) - 0.05							tCK (avg)	
DQS Low-Z from clock	tLZ(DQS)	MIN	-	tDQSCK (MIN) - 300							ps	
DQ Low-Z from clock	tLZ(DQ)	MIN	-	tDQSCK(MIN) - (1.4 × tQHS(MAX))							ps	
DQS High-Z from clock	tHZ(DQS)	MAX	-	tDQSCK (MAX) - 100							ps	
DQ High-Z from clock	tHZ(DQ)	MAX	-	tDQSCK(MAX) + (1.4 × tDQSQ(MAX))							ps	
WRITE Parameter												
DQ and DM input hold time(VREF=based)	tDH	MIN	-	210	235	270	350	430	480	600	ps	
DQ and DM input setup time(VREF=based)	tDS	MIN		210	235	270	350	430	480	600	ps	
DQ and DM input pulse width	tDIPW	MIN		0.35	0.35	0.35	0.35	0.35	0.35	0.35	tCK (avg)	
Write command to first DQS latching transition	tDQSS	MIN		0.75	0.75	0.75	0.75	0.75	0.75	0.75	tCK (avg)	
		MAX		1.25	1.25	1.25	1.25	1.25	1.25	1.25		
DQS input high-level width	tDQSH	MIN	-	0.4	0.4	0.4	0.4	0.4	0.4	0.4	tCK (avg)	
DQS input low-level width	tDQSL	MIN	-	0.4	0.4	0.4	0.4	0.4	0.4	0.4	tCK (avg)	
DQS falling edge to CK setup time	tDSS	MIN	-	0.2	0.2	0.2	0.2	0.2	0.2	0.2	tCK (avg)	
DQS falling edge hold time from CK	tDSH	MIN	-	0.2	0.2	0.2	0.2	0.2	0.2	0.2	tCK (avg)	
Write postamble	tWPST	MIN	-	0.4	0.4	0.4	0.4	0.4	0.4	0.4	tCK (avg)	
Write preamble	tWPRE	MIN	-	0.35	0.35	0.35	0.35	0.35	0.35	0.35	tCK (avg)	
CKE Input Parameters												
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	MIN	3	3	3	3	3	3	3	3	tCK (avg)	
CKE input setup time	tISCKE	MIN	-	0.25	0.25	0.25	0.25	0.25	0.25	0.25	tCK (avg)	9
CKE input hold time	tIHCKE	MIN	-	0.25	0.25	0.25	0.25	0.25	0.25	0.25	tCK (avg)	10

Table 79: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions.

AC timing parameters must satisfy the tCK minimum conditions(in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min / Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Command Address Input Parameter												
Address and control input setup time	tIS	MIN	-	220	250	290	370	460	600	740	ps	11
Address and control input hold time	tIH	MIN	-	220	250	290	370	460	600	740	ps	11
Address and control input pulse width	tIPW	MIN	-	0.40	0.40	0.40	0.40	0.40	0.40	0.40	tCK (avg)	
Boot Parameters(max 55MHz)												
Clock cycle time	tCKb	MAX	-	-	-	-	-	-	-	-	ns	
		MIN		18	18	18	18	18	18	18		
CKE input setup time	tISCKEb	MIN	-	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
CKE input hold time	tIHCKEb	MIN	-	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
Address and control input setup time	tISb	MIN	-	1150	1150	1150	1150	1150	1150	1150	ps	
Address and control input hold time	tIHb	MIN	-	1150	1150	1150	1150	1150	1150	1150	ps	
DQS output data Access time from CK/CK#	tDQSCKb	MIN	-	2.0	2.0	2.0	2.0	2.0	2.0	2.0	ns	
		MAX	-	10.0	10.0	10.0	10.0	10.0	10.0	10.0		
Data strobe edge to output data edge	tDQSQb	MIN	-	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	
Data hold skew factor	tQHSb	MIN	-	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	
Mode Register Parameter												
MODE REGISTER WIRTE command period	tMRW	MIN	3	3	3	3	3	3	3	3	tCK (avg)	
MODE REGISTER READ command period	tMRR	MIN	2	2	2	2	2	2	2	2	tCK (avg)	
Core Parameter												
READ latency	RL	MIN	3	8	7	6	5	4	3	3	tCK (avg)	
WRITE latency	WL	MIN	1	4	4	3	2	2	1	1	tCK (avg)	
ACTIVATE-to-ACTIVATE command period	tRC	MIN	-	tRAS + tRPab (with all-bank precharge), tRAS + tRPpb (with per-bank precharge)							ns	17
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	tCKESR	MIN	3	15	15	15	15	15	15	15	ns	
SELF REFRESH exit to next valid command delay	tXSR	MIN	2	tRFCab + 10							ns	

Table 80: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions.

AC timing parameters must satisfy the tCK minimum conditions(in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min / Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Exit power-down to next valid	tXP	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
LPDDR2-S4 CAS-to-CAS delay	tCCD	MIN	-	2	2	2	2	2	2	2	tCK (avg)	
Internal READ to PRECHARGE	tRTP	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
RAS-to-CAS delay	tRCD	Fast	3	15	15	15	15	15	15	15	ns	
		Typ	3	18	18	18	18	18	18	18		
Row precharge time (single bank)	tRPpb	Fast	3	15	15	15	15	15	15	15	ns	
		Typ	3	18	18	18	18	18	18	18		
Row precharge time (all banks)	tRPpab 8-bank	Fast	3	18	18	18	18	18	18	18	ns	
		Typ	3	21	21	21	21	21	21	21		
Row active time	tRAS	MIN	3	42	42	42	42	42	42	42	ns	
		MAX	-	70	70	70	70	70	70	70	us	
WRITE recovery time	tWR	MIN	3	15	15	15	15	15	15	15	ns	
Internal WT-to-RD command delay	tWTR	MIN	2	7.5	7.5	7.5	7.5	7.5	10	10	ns	
Active bank *a* to active bank *b*	tRRD	MIN	2	10	10	10	10	10	10	10	ns	
Four-bank activate window	tFAW	MIN	8	50	50	50	50	50	50	60	ns	
Minimum deep power-down time	tDPD	MIN	-	500	500	500	500	500	500	500	us	
Temperature Derating												
tDQSCK derating	tDQSCK (derating)	MAX	-	5620	6000	6000	6000	6000	6000	6000	ps	

Table 81: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions.

AC timing parameters must satisfy the tCK minimum conditions(in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min / Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Core timing Temperature derating	tRCD (derated)	MIN	-	tRCD + 1.875							ns	
	tRC (derated)	MIN	-	tRC + 1.875							ns	
	tRAS (derated)	MIN	-	tRAS + 1.875							ns	
	tRP (derated)	MIN	-	tRP + 1.875							ns	
	tRRD (derated)	MIN	-	tRRD + 1.875							ns	

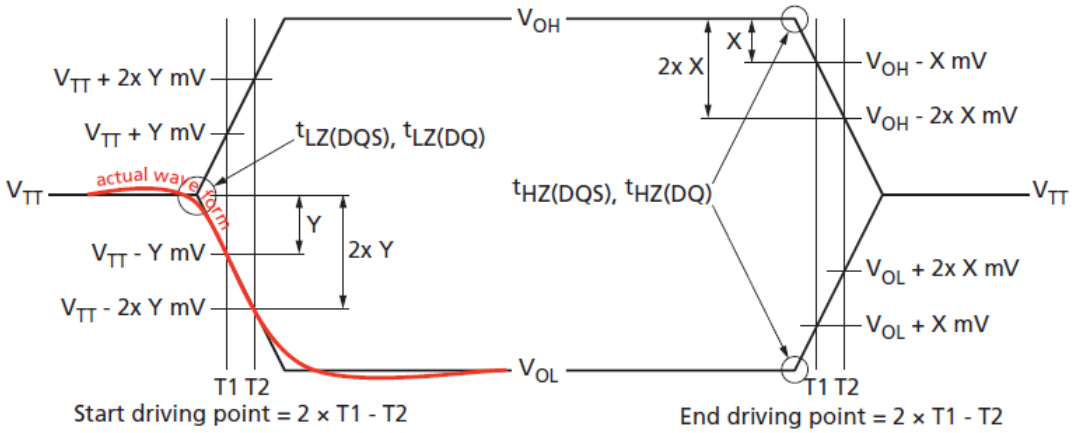
Notes : 1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.

2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to V_{REF}.
4. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
5. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
6. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions.

   These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ) or begins driving tLZ(DQS) and tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended.

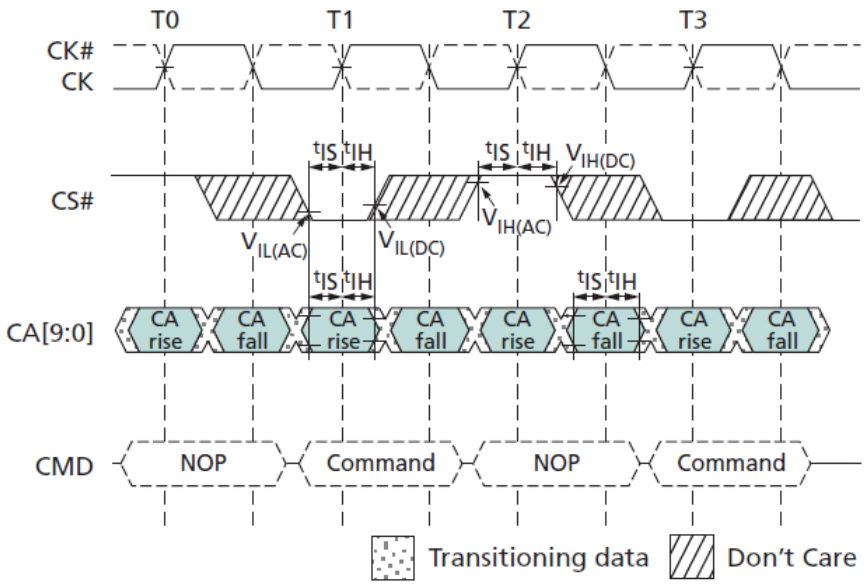
   The timing parameters tRPRE and tRPST are determined from the differential signal DQS/DQS#.

Output Transition Timing



7. Measured from the point when DQS/DQS# begins driving the signal, to the point when DQS/DQS# begins driving the first rising strobe edge.
8. Measured from the last falling strobe edge of DQS/DQS# to the point when DQS/DQS# finishes driving the signal.
9. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK/CK# crossing.
10. CKE input hold time is measured from CK/CK# crossing to CKE reaching a HIGH/LOW voltage level.
11. Input setup/hold time for signal (CA[9:0], CS#).
12. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. The letter b is appended to the boot parameter symbols (for example, tCK during boot is tCKb).
13. Mobile LPDDR2 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.
14. The output skew parameters are measured with default output impedance settings using the reference load.
15. The minimum tCK column applies only when tCK is greater than 6ns.
16. Timing derating applies for operation at 85˚C to 105˚C when the requirement to derate is indicated by mode register 4 op-code (see the MR4 Device Temperature (MA[7:0] =04h) table).
17. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

Figure 70: Command Input Setup and Hold Timing



Notes :1. The setup and hold timing shown applies to all commands.

2. Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see Power-Down.

CA and CS# Setup, Hold, and Derating

For all input signals (CA and CS#), the total required setup time (tIS) and hold time (tIH) is calculated by adding the data sheet tIS (base) and tIH (base) values to the ΔtIS and ΔtIH derating values, respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS. (See the series of tables following this section.)

The typical setup slew rate (tIS) for a rising signal is defined as the slew rate between the last crossing ofVREF(DC) and the first crossing of $V_{IH(AC)MIN}$. The typical setup slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)MAX}$. If the actual signal is consistently earlier than the typical slew rate line between the shaded $V_{REF(DC)}$-to-(AC) region, use the typical slew rate for the derating value (see Figure 71). If the actual signal is later than the typical slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see Figure 73).

The hold (tIH) typical slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)MAX}$ and the first crossing of $V_{REF(DC)}$. The hold (tIH) typical slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)MIN}$ and the first crossing of $V_{REF(DC)}$.

If the actual signal is consistently later than the typical slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the typical slew rate for the derating value (see Figure 72). If the actual signal is earlier than the typical slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see Figure 74).

For a valid transition, the input signal must remain above or below $V_{IH/VIL(AC)}$ for a specified time, tVAC (see Table 86).

For slow slew rates the total setup time could be a negative value (that is, a valid input signal will not have reached $V_{IH/VIL(AC)}$ at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach $V_{IH/VIL(AC)}$. For slew rates between the values listed in Table 84, the derating values are obtained using linear interpolation.

Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Table 82: CA and CS# Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
tIS(base)	0	30	70	150	240	300	$V_{IH/VIL(AC)} = V_{REF(DC)}$ ±220mV
tIH(base)	90	120	160	240	330	390	$V_{IH/VIL(DC)} = V_{REF(DC)}$ ±130mV

Note : 1. AC/DC referenced for 1 V/ns CA and CS# slew rate, and 2 V/ns differential CK/CK# slew rate

Table 83: CA and CS# Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate				Reference
	400	333	255	200	
tIS(base)	300	440	600	850	$V_{IH/VIL(AC)} = V_{REF(DC)}$ ±300mV
tIH(base)	400	540	700	950	$V_{IH/VIL(DC)} = V_{REF(DC)}$ ±200mV

Note : 1. AC/DC referenced for 1 V/ns CA and CS# slew rate, and 2 V/ns differential CK/CK# slew rate

Table 84: Derating Values for AC/DC-Based tIS/tIH (AC220)

ΔtIS, ΔtIH derating in ps

		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS# slew rare V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note : 1. Shaded cells are not supported.

Table 85: Derating Values for AC/DC-Based tIS/tIH (AC300)

ΔtIS, ΔtIH derating in ps

		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS# slew rare V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note : 1. Shaded cells are not supported.

Table 86: Required Time for Valid Transition – tVAC > $V_{IH(AC)}$ and < $V_{IL(AC)}$

Slew Rate (V/ns)	tVAC at 300mV(ps)		tVAC at 220mV(ps)	
	Min	Max	Min	Max
>2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-

Figure 71: Typical Slew Rate and tVAC – tIS for CA and CS# Relative to Clock

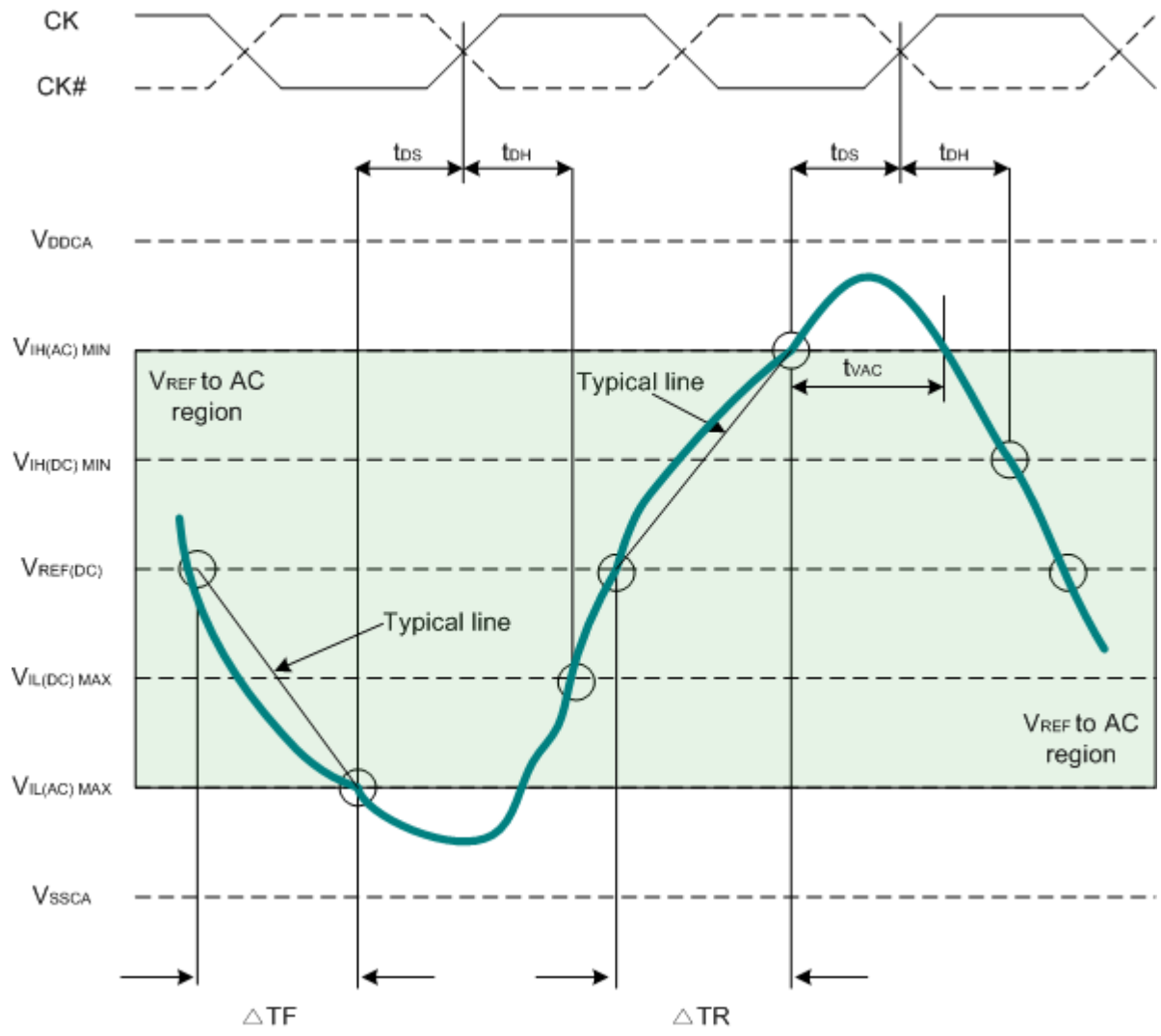


Figure 72: Typical Slew Rate – tIH for CA and CS# Relative to Clock

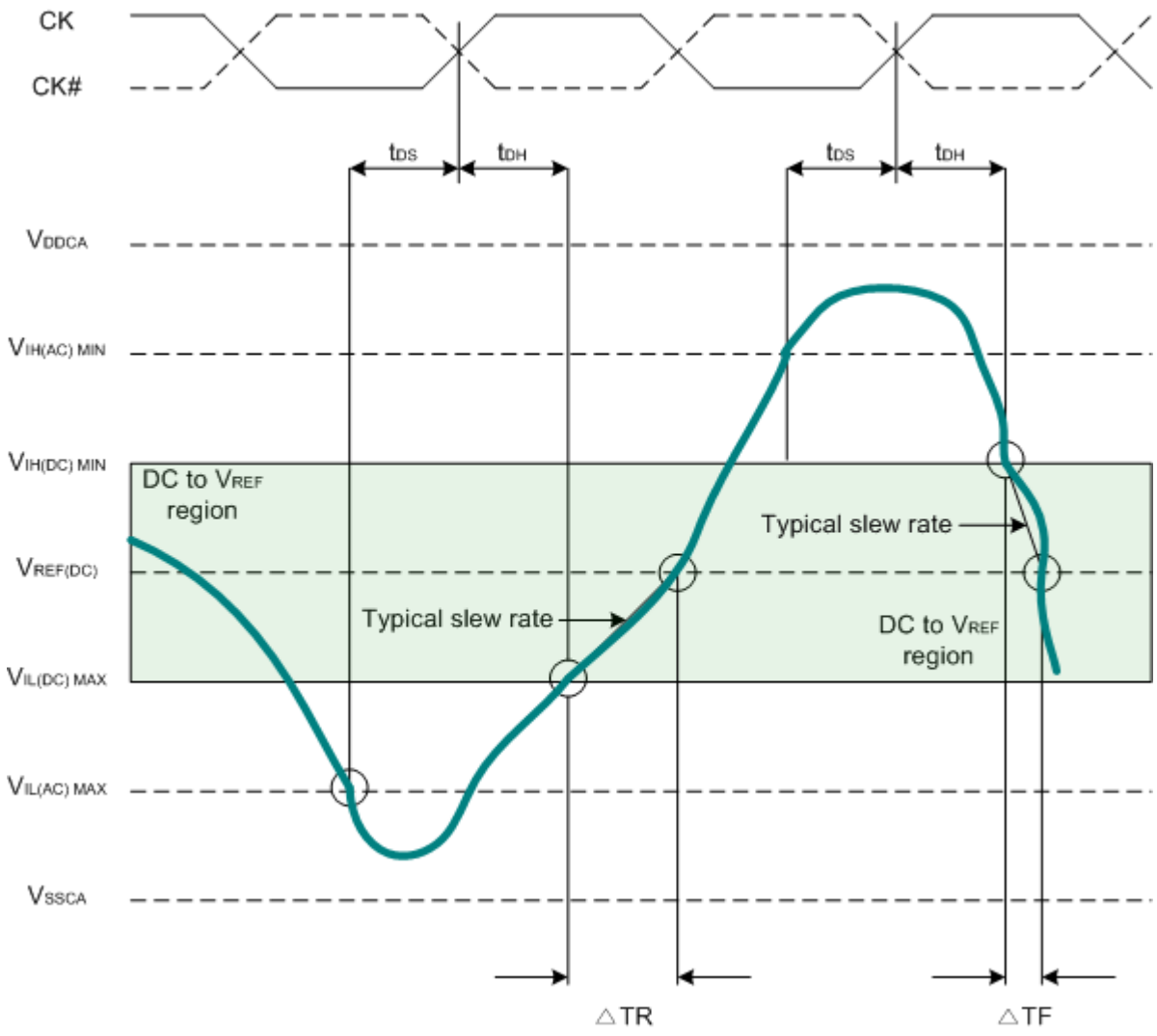


Figure 73: Tangent Line – tIS for CA and CS# Relative to Clock

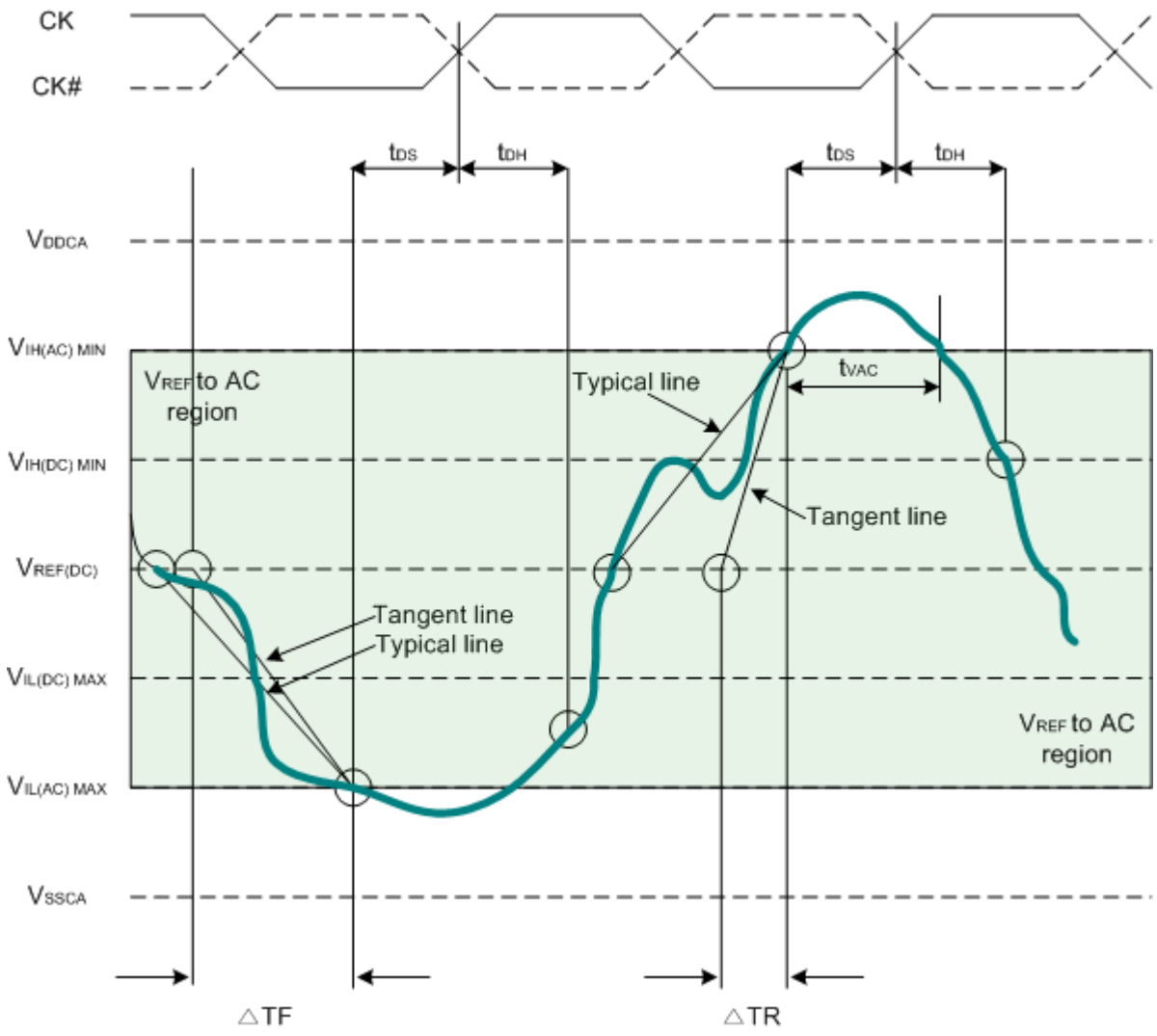
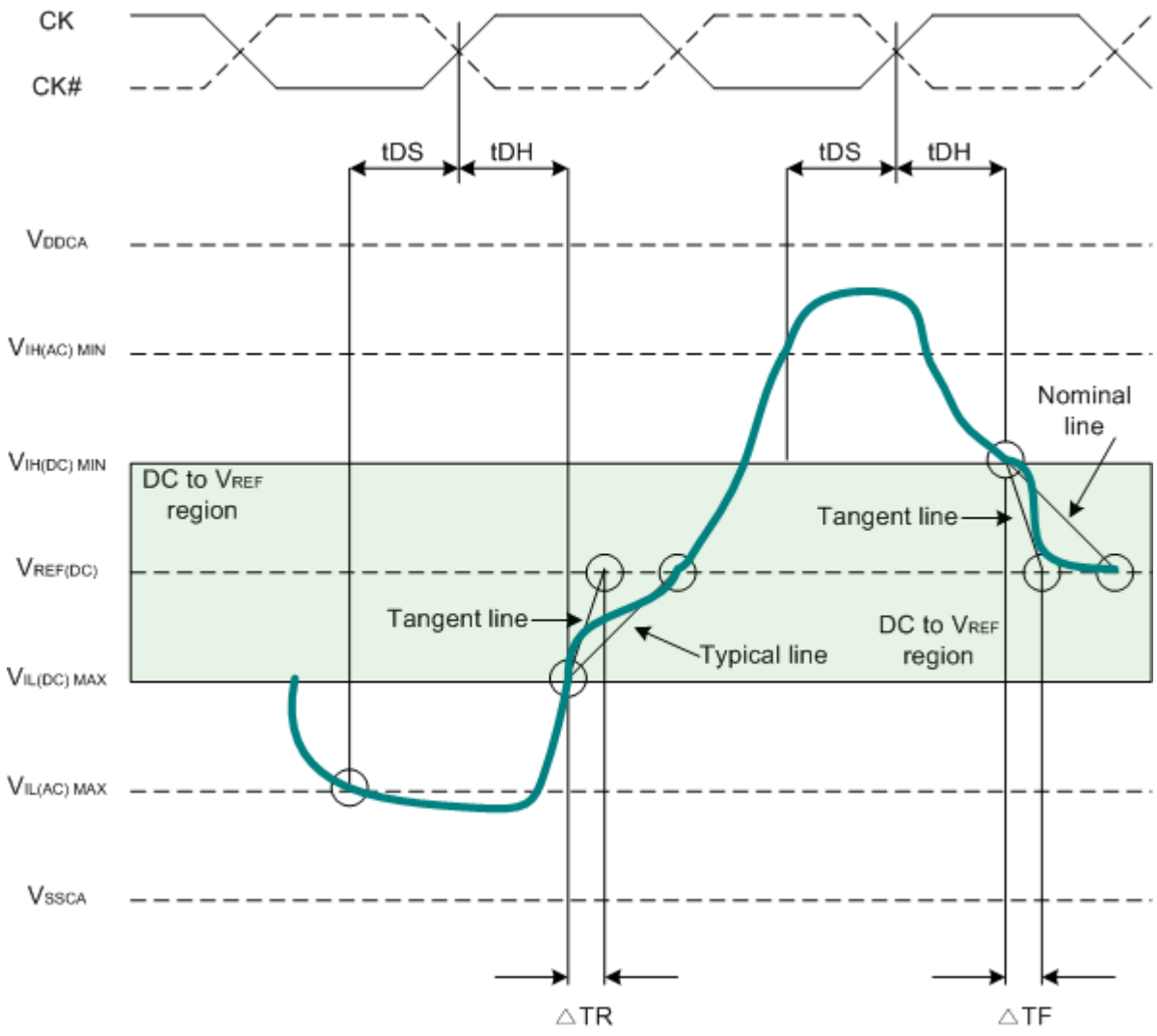


Figure 74: Tangent Line – tIH for CA and CS# Relative to Clock



Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) calculate the total required setup time (tDS) and hold time (tDH) by adding the data sheet tDS(base) and tDH(base) values (see Table 87) to the ΔtDS and ΔtDH derating values, respectively (see Table 89 and Table 90).

Example: tDS = tDS(base) + ΔtDS. The typical tDS slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)MIN}$. The typical tDS slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)MAX}$ (see Figure 75).

If the actual signal is consistently earlier than the typical slew rate line in Figure 71) the area shaded gray between the $V_{REF(DC)}$ region and the AC region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded $V_{REF(DC)}$ region and the AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see Figure 73).

The typical tDH slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)MAX}$ and the first crossing of $V_{REF(DC)}$. The typical tDH slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)MIN}$ and the first crossing of $V_{REF(DC)}$ (see Figure 76).

If the actual signal is consistently later than the typical slew rate line between the shaded DC-level-to-$V_{REF(DC)}$ region, use the typical slew rate for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between shaded DC-to -$V_{REF\ (DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for the derating value (see Figure 78).

For a valid transition, the input signal must remain above or below $V_{IH/VIL(AC)}$ for the specified time, tVAC(see Table 91).

The total setup time for slow slew rates could be negative (that is, a valid input signal may not have reached $V_{IH/VIL(AC)}$ at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach $V_{IH/VIL(AC)}$.

For slew rates between the values listed in Table 87 and Table 88, the derating values can be obtained using linear interpolation.

Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Table 87: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
tDS(base)	-10	15	50	130	210	230	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±220mV
tDH(base)	80	105	140	220	300	320	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±130mV

Table 88: Data Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate				Reference
	400	333	255	200	
tDS(base)	180	300	450	700	VIH/VIL(AC) = VREF(DC) ±300mV
tDH(base)	280	400	550	800	VIH/VIL(DC) = VREF(DC) ±200mV

Note : 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS/DQS# slew rate

Table 89: Derating Values for AC/DC-Based tDS/tDH (AC220)

ΔtDS, ΔtDH derating in ps

		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note : 1. Shaded cells are not supported.

Table 90: Derating Values for AC/DC-Based tDS/tDH (AC300)

ΔtDS, ΔtDH derating in ps

		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4												4	-35	-40	-11	-8

Note : 1. Shaded cells are not supported.

Table 91: Required Time for Valid Transition – tVAC > $V_{IH(AC)}$ or < $V_{IL(AC)}$

Slew Rate (V/ns)	tVAC at 300mV(ps)		tVAC at 220mV(ps)	
	Min	Max	Min	Max
>2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-

Table 90: Derating Values for AC/DC-Based tDS/tDH (AC300)

ΔtDS, ΔtDH derating in ps

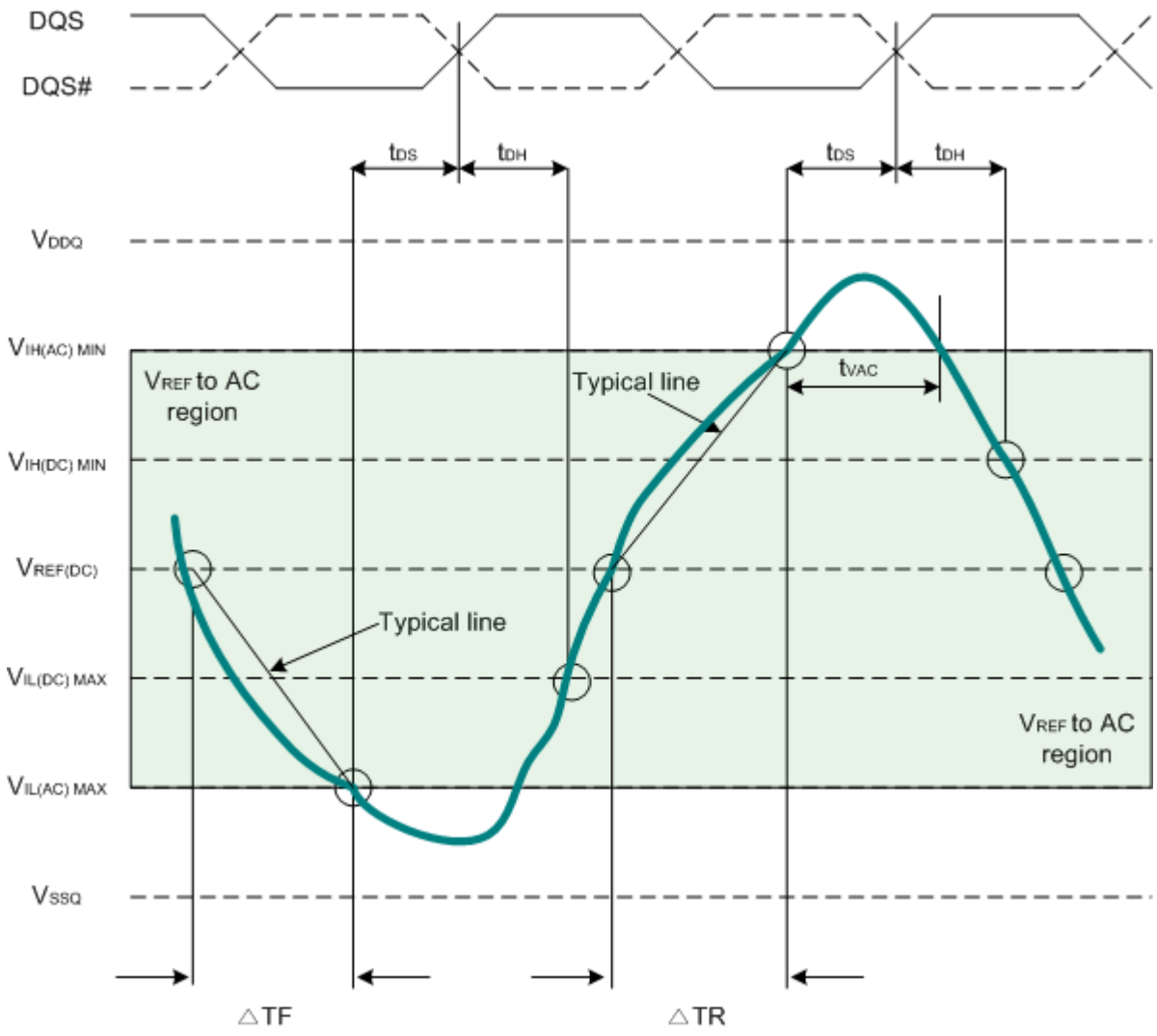
		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4												4	-35	-40	-11	-8

Note : 1. Shaded cells are not supported.

Table 91: Required Time for Valid Transition – tVAC > $V_{IH(AC)}$ or < $V_{IL(AC)}$

Slew Rate (V/ns)	tVAC at 300mV(ps)		tVAC at 220mV(ps)	
	Min	Max	Min	Max
>2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-

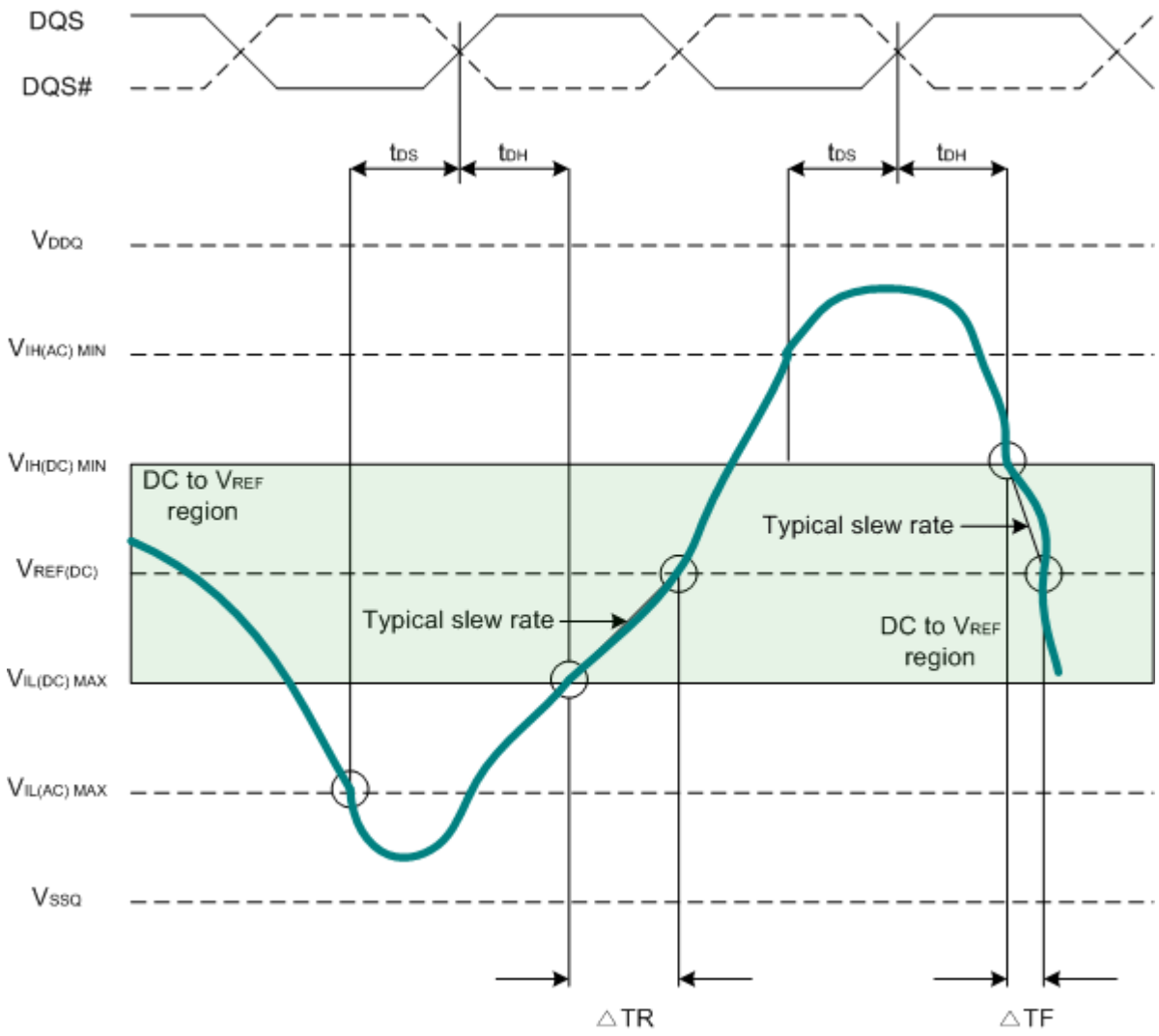
Figure 75: Typical Slew Rate and tVAC – tDS for DQ Relative to Strobe



$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$$

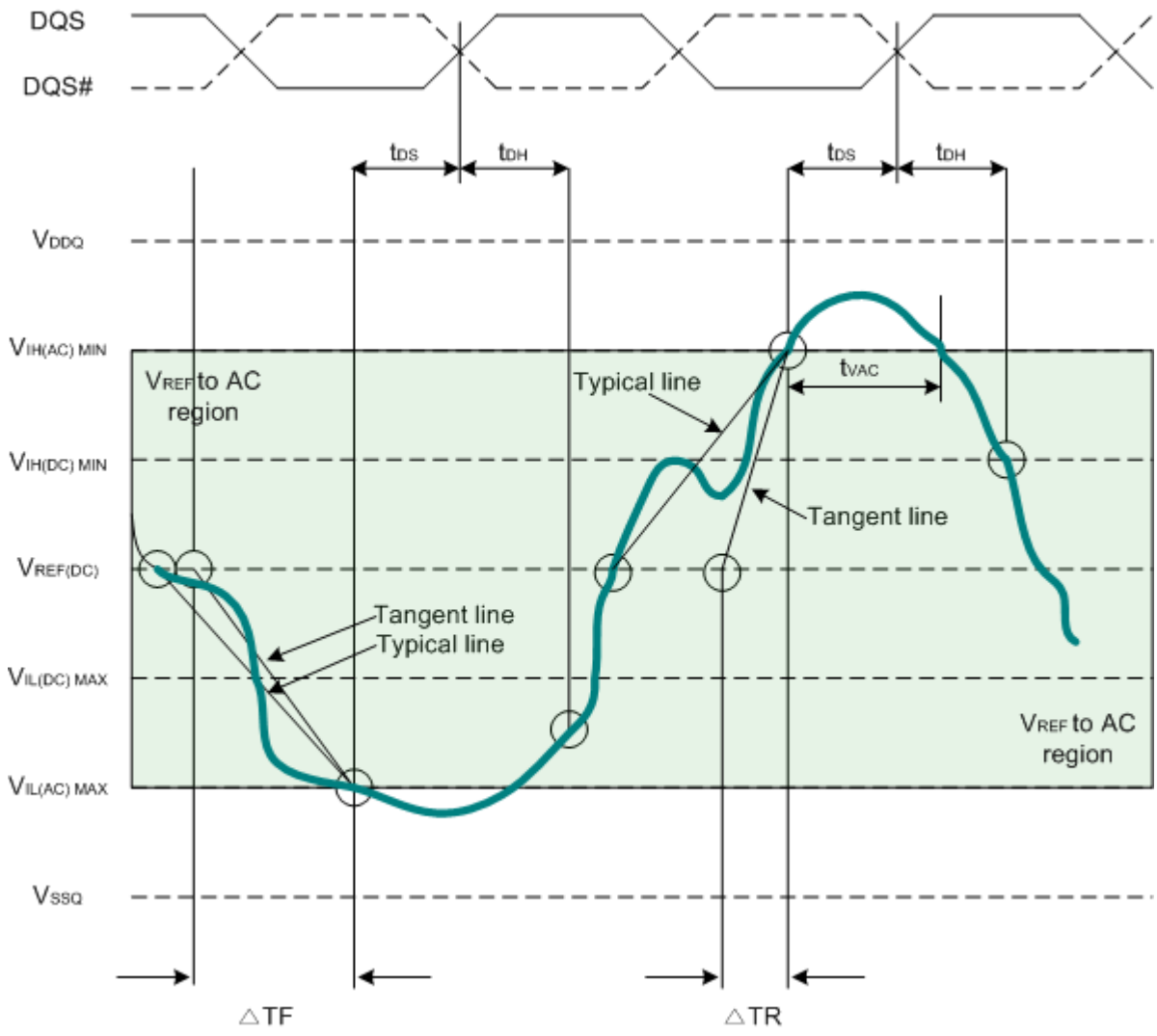
Figure 76: Typical Slew Rate – tDH for DQ Relative to Strobe



$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

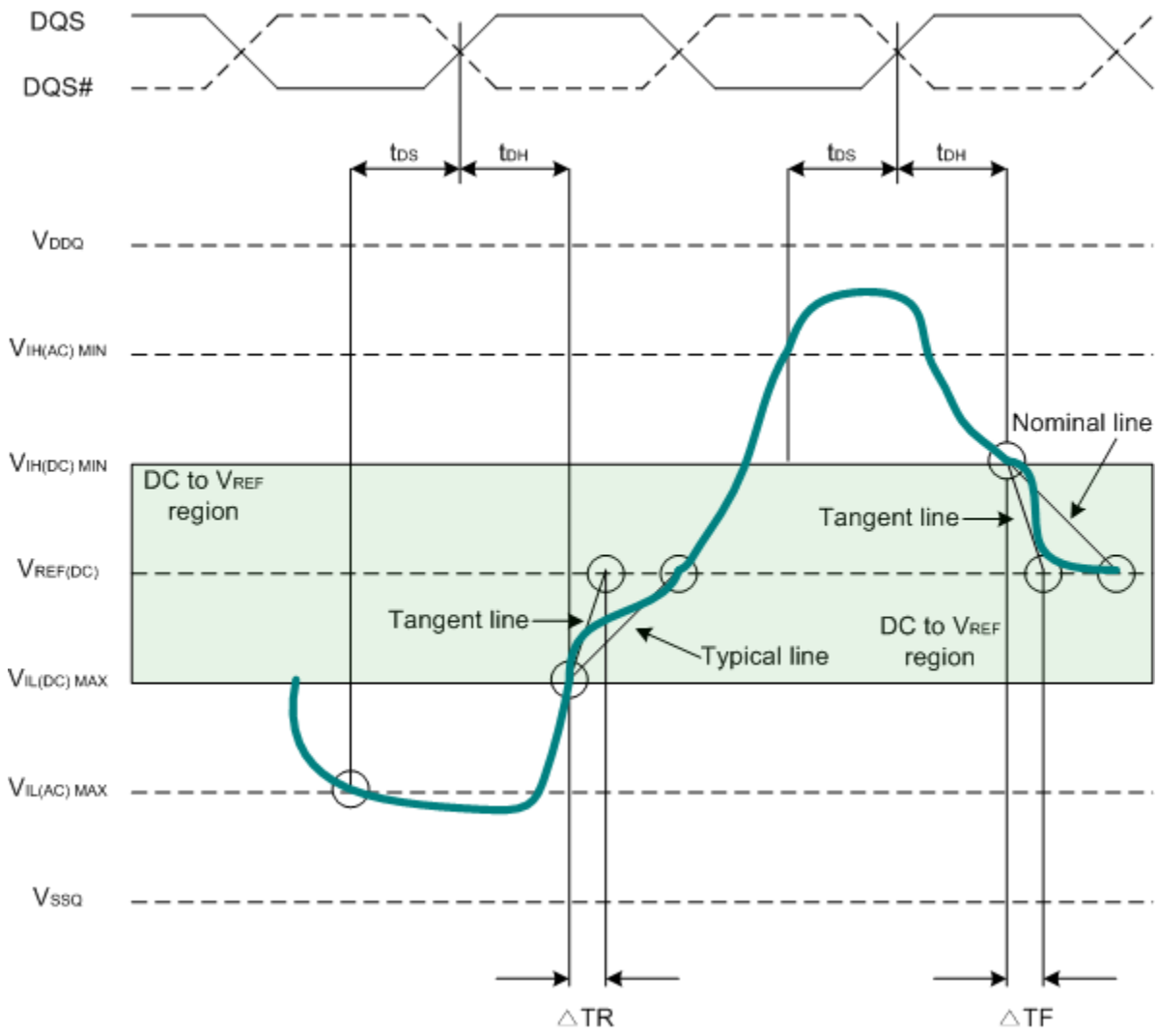
Figure 77: Tangent Line – tDS for DQ with Respect to Strobe



$$\text{Setup slew rate falling signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(AC)max}]}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{\text{tangent line } [V_{IH(AC)min} - V_{REF(DC)}]}{\Delta TR}$$

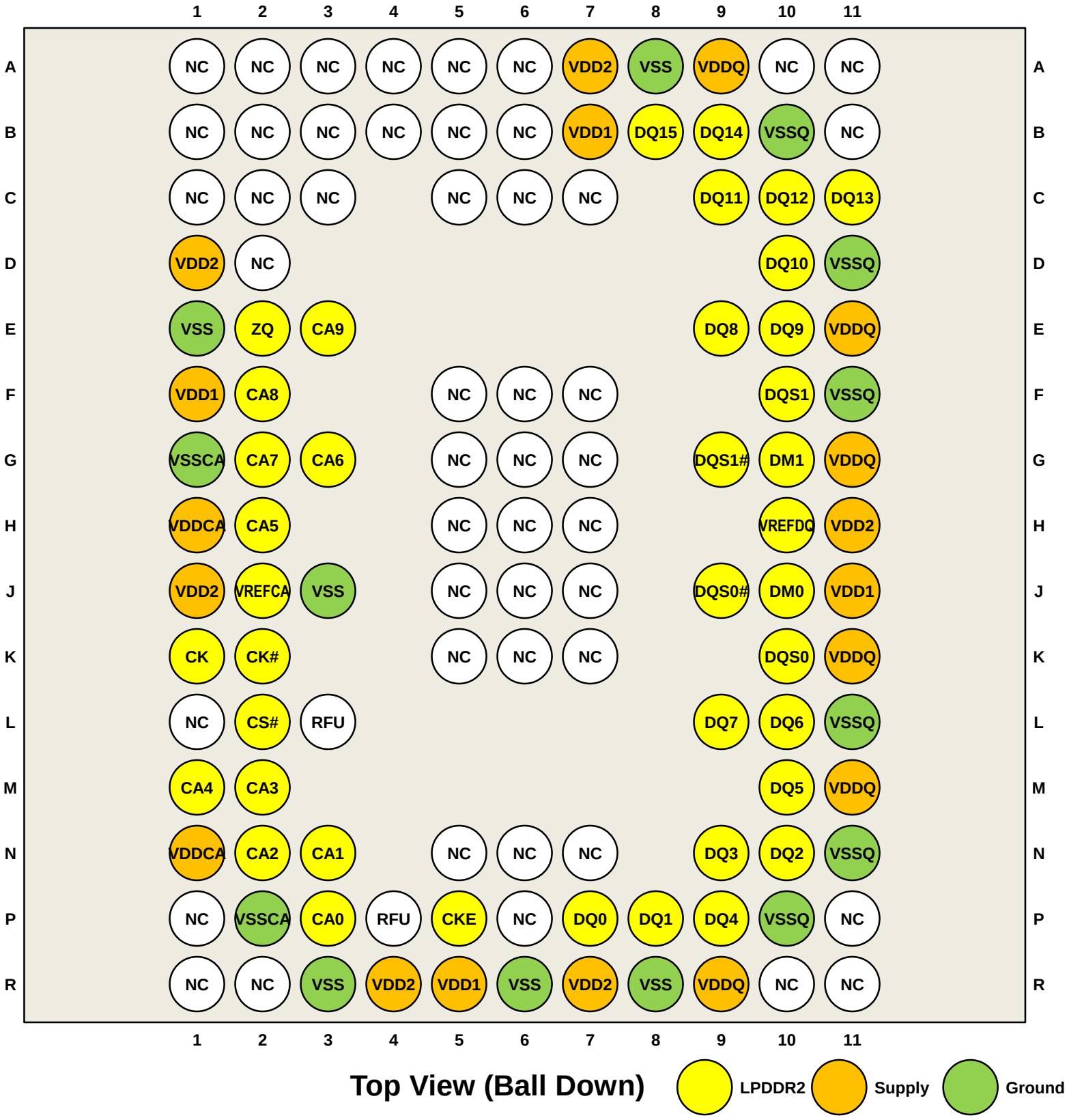
Figure 78: Tangent Line – tDH for DQ with Respect to Strobe



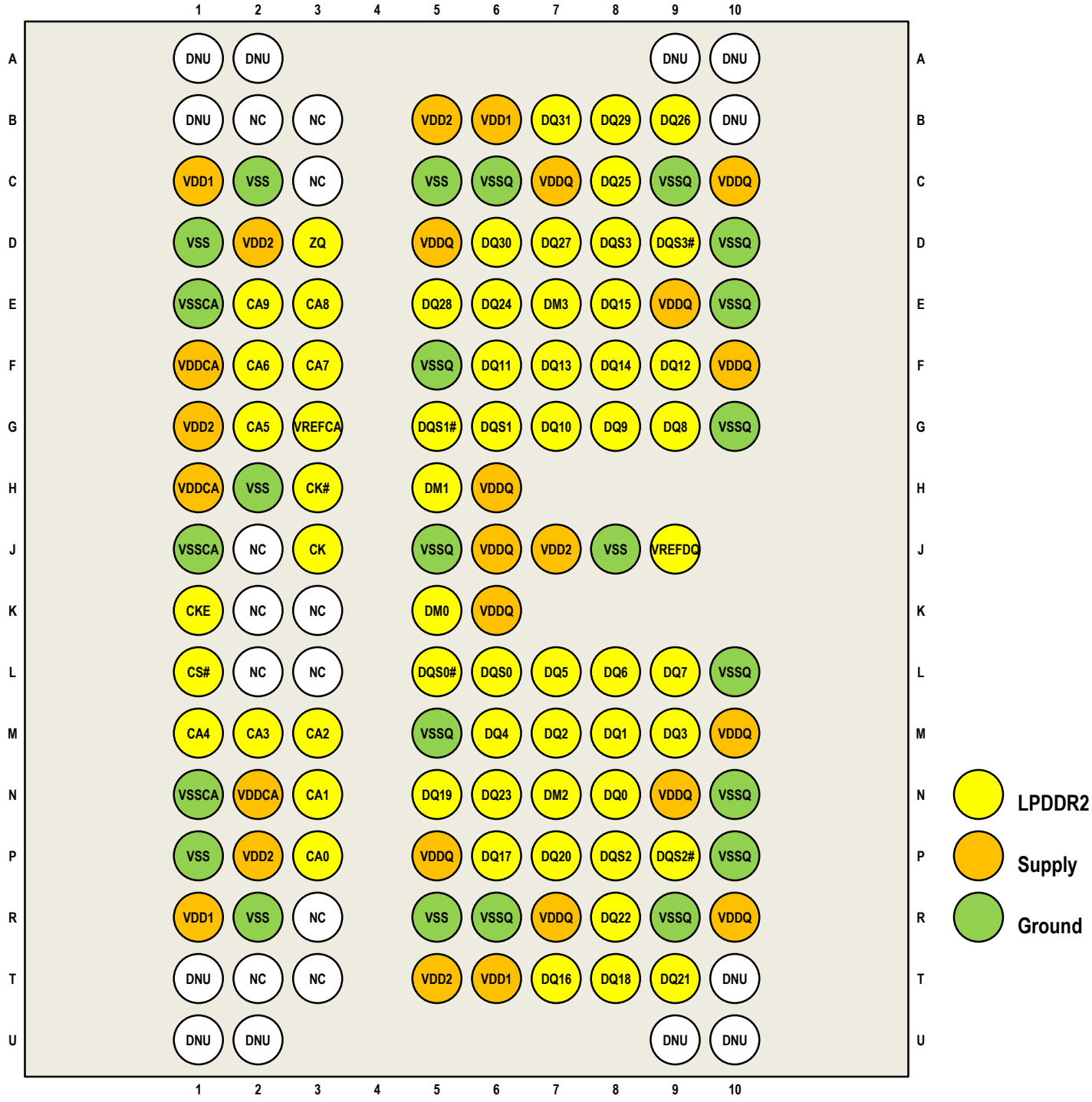
$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } [V_{IH(DC)min} - V_{REF(DC)}]}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)max}]}{\Delta TR}$$

Pin Configuration – 121Ball FBGA(X16)

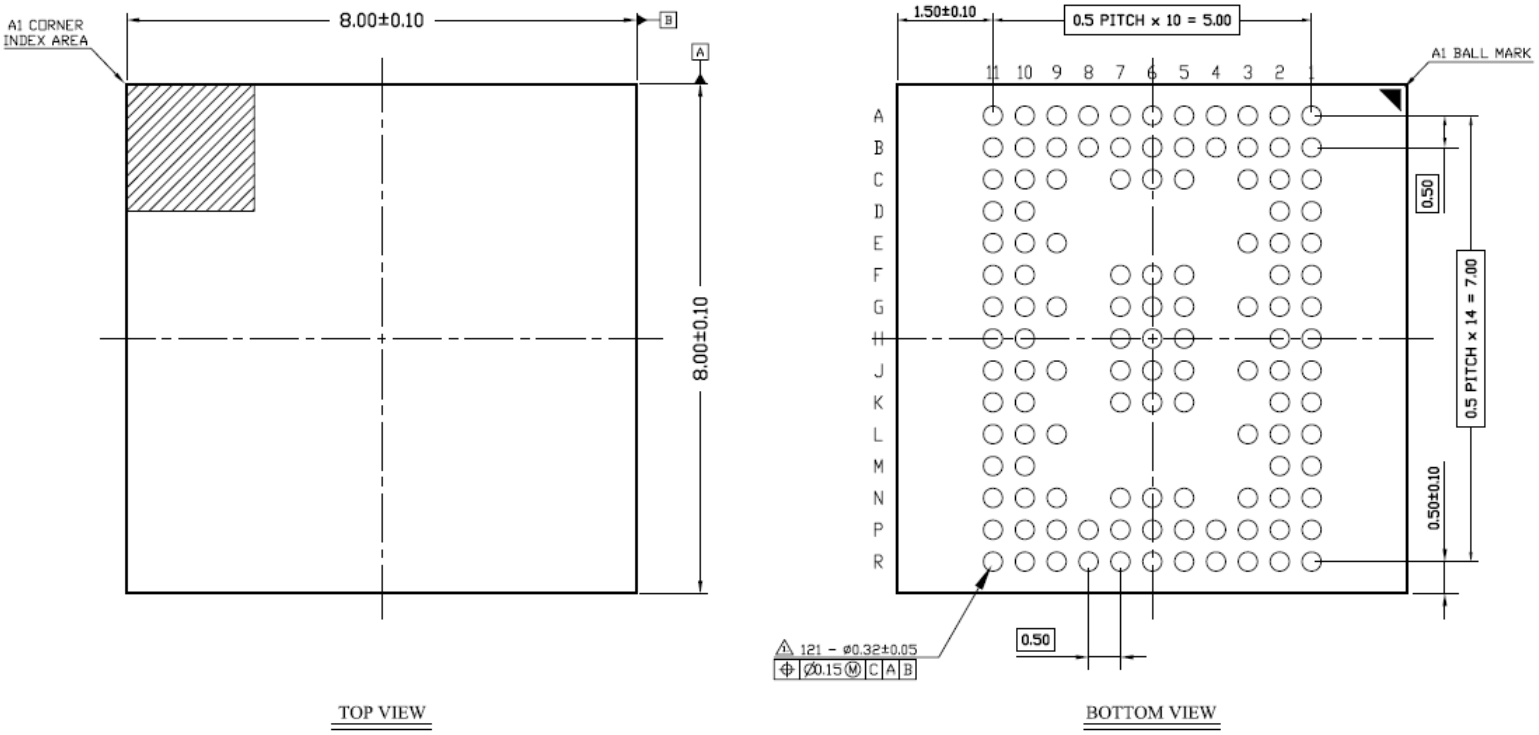


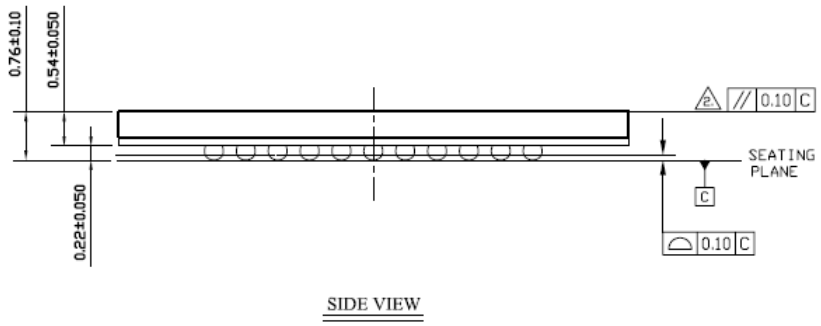
Pin Configuration – 134Ball FBGA(X32)



Top View (Ball Down)

Package Dimension – 121Ball FBGA(X16)

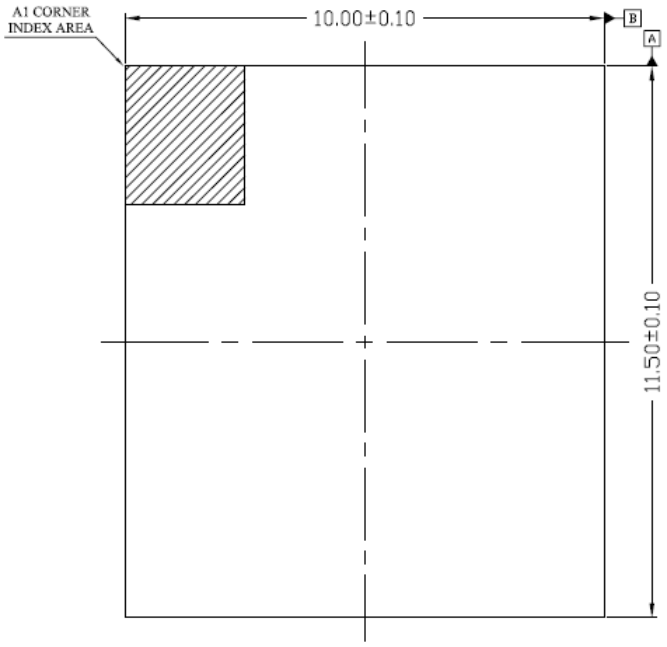




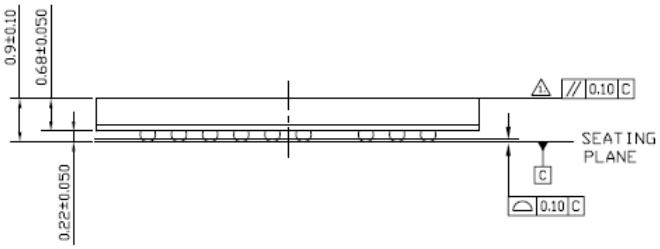
NOTE :

1. ALL DIMENSION ARE IN MILLIMETERS.
2. ⚠ POST REFLOW SOLDER BALL DIAMETER. (Pre Reflow Diameter : 0.30±0.02)
3. ⚠ TOLERANCE INCLUDES WARPAGE.

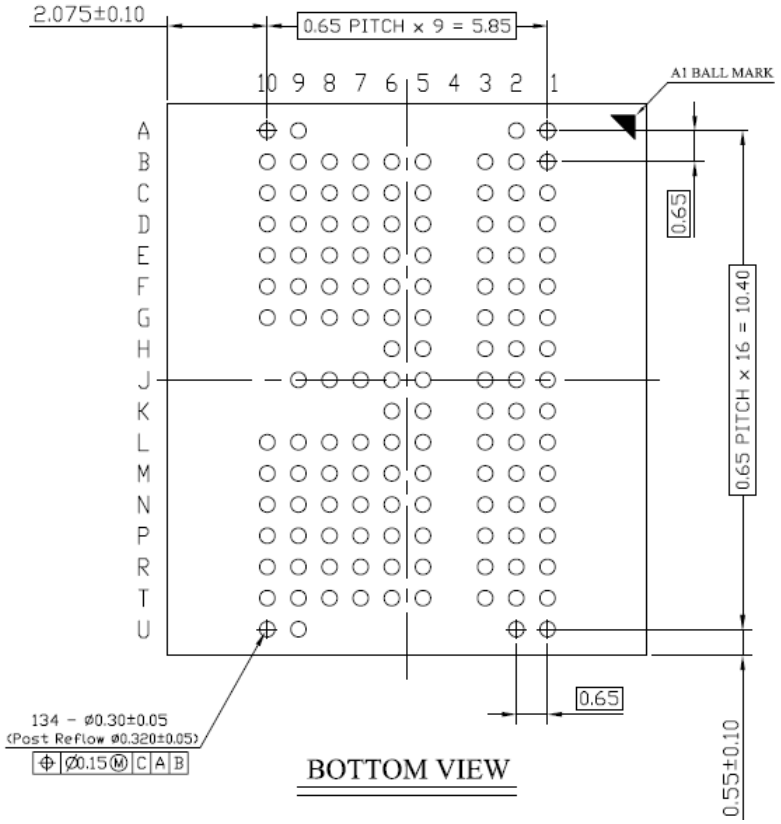
Package Dimension – 134Ball FBGA(X32)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTE :
1. ALL DIMENSION ARE IN MILLIMETERS.
2. ⚠ TOLERANCE INCLUDES WARPAGE.