FAIRCHILD
A Schlumberger Company

FMP20N05/FMP18N05 T-39-11
N-Channel Power MOSFETs, 18-20 A, 50 V

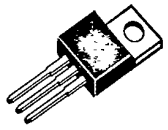
Power And Discrete Division

Description

These devices are very low $R_{DS(on)}$, 50 V, n-channel, enhancement mode, power MOSFETs especially designed to serve the low voltage, high speed, switching markets. Typical applications are SMPS for telecommunication and instrumentation, DC motor controls, emitter switching, synchronous rectification, and systems that are operated from low voltage batteries, such as automotive and portable equipment, etc.

- **Extremely low $R_{DS(on)}$**
- **V_{GS} Rated at ±30 V**
- **Silicon Gate for Fast Switching Speeds**
- **Rugged**
- **Low Drive Requirements**
- **Ease of Paralleling**

TO-220AB



IS00060F

FMP18N05
FMP20N05

Maximum Ratings

Symbol	Characteristic	Rating FMP20N05	Rating FMP18N05	Unit
V_{DSS}	Drain to Source Voltage[1]	50	50	V
V_{DGR}	Drain to Gate Voltage[1] R_{GS} = 20 kΩ	50	50	V
V_{GS}	Gate to Source Voltage	±30	±30	V
T_J, T_{stg}	Operating Junction and Storage Temperatures	−55 to +150	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8″ From Case for 5 s	300	300	°C

Maximum On-State Characteristics

		FMP20N05	FMP18N05	
$R_{DS(on)}$	Static Drain-to-Source On Resistance	0.085	0.10	Ω
I_D	Drain Current Continuous at T_C = 25°C Continuous at T_C = 100°C Pulsed	 20 14 60	 18 13 50	A

Maximum Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.67	1.67	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	80	80	°C/W
P_D	Total Power Dissipation at T_C = 25°C	75	75	W

Notes
For information concerning connection diagram and package outline, refer to Section 7.

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit	Test Conditions
Off Characteristics					
$V_{(BR)DSS}$	Drain Source Breakdown Voltage[1]	50		V	V_{GS} = 0 V, I_D = 250 μA
I_{DSS}	Zero Gate Voltage Drain Current		250	μA	V_{DS} = Rated V_{DSS}, V_{GS} = 0 V
			1000	μA	V_{DS} = 0.8 x Rated V_{DSS}, V_{GS} = 0 V, T_C = 125°C
I_{GSS}	Gate-Body Leakage Current		±500	nA	V_{GS} = ±20 V, V_{DS} = 0 V
On Characteristics					
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	I_D = 250 μA, V_{DS} = V_{GS}
$R_{DS(on)}$	Static Drain-Source On-Resistance[2]			Ω	V_{GS} = 10 V, I_D = 10 A
	FMP20N05		0.085		
	FMP18N05		0.10		
$V_{DS(on)}$	Drain-Source On-Voltage[2] FMP20N05		2.0	V	V_{GS} = 10 V; I_D = 20 A;
	FMP18N05		2.25		
	FMP20N05 FMP18N05		1.40	V	V_{GS} = 10 V; I_D = 10 A; T_C = 100°C
g_{fs}	Forward Transconductance	5		S (℧)	V_{DS} = 10 V, I_D = 10 A
Dynamic Characteristics					
C_{iss}	Input Capacitance		850	pF	V_{DS} = 25 V, V_{GS} = 0 V f = 1.0 MHz
C_{oss}	Output Capacitance		400	pF	
C_{rss}	Reverse Transfer Capacitance		150	pF	
Switching Characteristics (T_C = 25°C, *Figures 9, 10*)					
$t_{d(on)}$	Turn-On Delay Time		50	ns	V_{DD} = 40 V, I_D = 10 A V_{GS} = 10 V, R_{GEN} = 50 Ω R_{GS} = 50 Ω
t_r	Rise Time		90	ns	
$t_{d(off)}$	Turn-Off Delay Time		60	ns	
t_f	Fall Time		75	ns	
Q_g	Total Gate Charge		20	nC	V_{GS} = 10 V, I_D = 25 A V_{DD} = 40 V

Symbol	Characteristic	Typ	Max	Unit	Test Conditions
Source-Drain Diode Characteristics					
V_{SD}	Diode Forward Voltage		1.5	V	I_S = 20 A; V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	60		ns	I_S = 20 A; dI_S/dt = 50 A/μS

Notes
1. T_J = +25°C to +150°C
2. Pulse test: Pulse width ≤ 80 μs, Duty cycle ≤ 1%

Typical Performance Curves

Figure 1 Output Characteristics

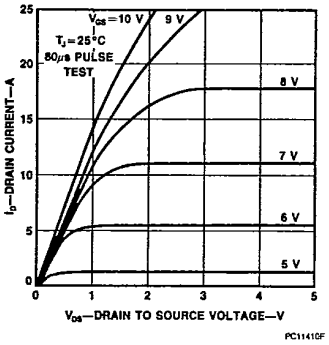


Figure 2 Static Drain to Source Resistance vs Drain Current

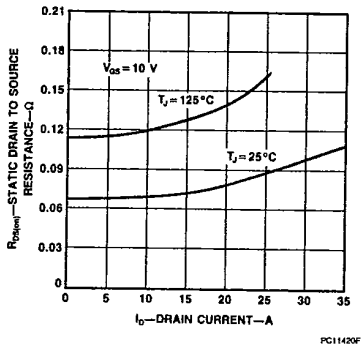


Figure 3 Transfer Characteristics

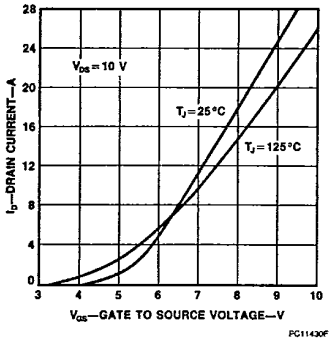


Figure 4 Temperature Variation of Gate to Source Threshold Voltage

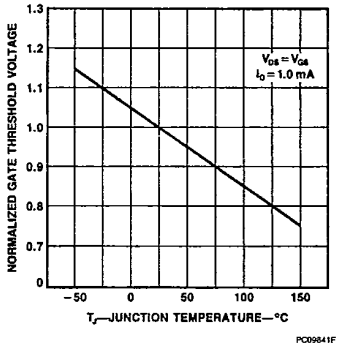


Figure 5 Capacitance vs Drain to Source Voltage

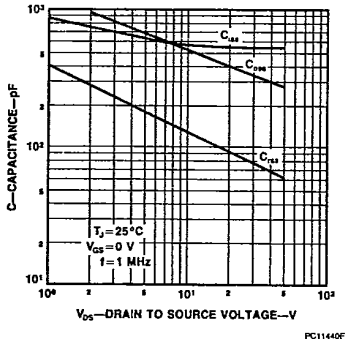
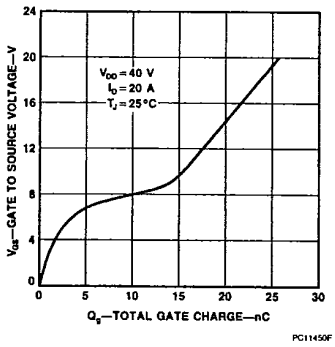


Figure 6 Gate to Source Voltage vs Total Gate Charge



Typical Performance Curves (Cont.)

Figure 7 Forward Biased Safe Operating Area

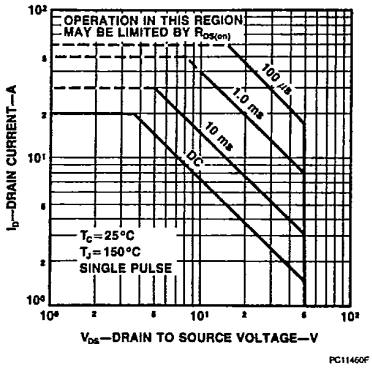
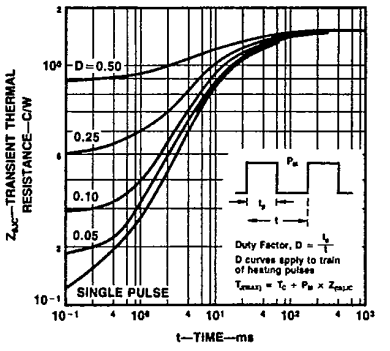


Figure 8 Transient Thermal Resistance vs Time



Typical Electrical Characteristics

Figure 9 Switching Test Circuit

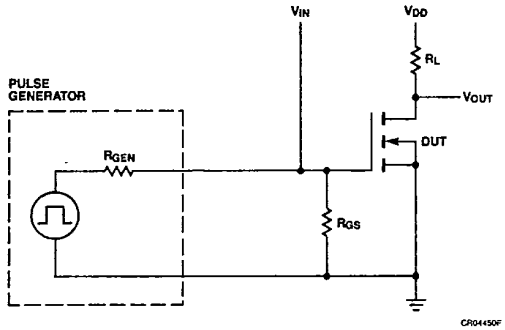


Figure 10 Switching Waveforms