

FMPA2300

2.3–2.4GHz WiMax/WiBro Linear Power Amplifier

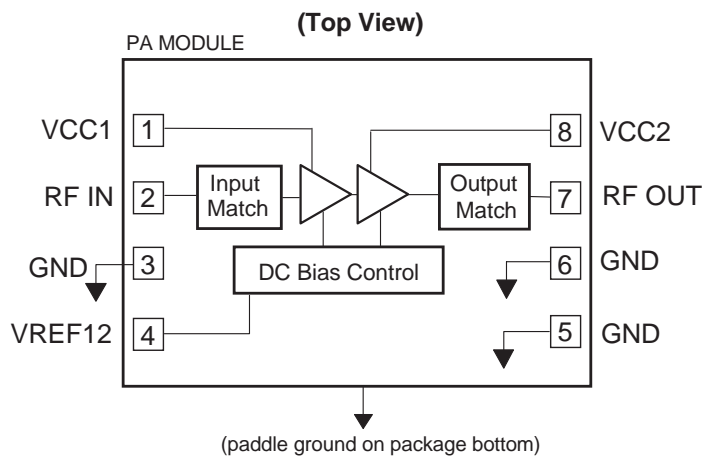
Features

- 25dB small signal gain
- 30dBm output power @ 1dB compression
- 16.5% PAE at 22dBm modulated power out
- 2% EVM at 22dBm modulated power out
- 3.4V collector supply operation
- 2.85V reference supply operation
- Lead-free RoHS compliant 3 x 3 x 1mm leadless package
- Internally matched to 50Ω and DC blocked RF input/output
- Optimized for use in 802.16e applications

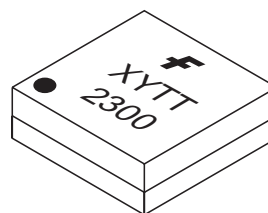
General Description

The FMPA2300 power amplifier is designed for high performance WiMax and WiBro applications in the 2.3–2.4GHz frequency band. The low profile 8 pin 3 x 3 x 1mm package with internal matching on both input and output to 50Ω minimizes next level PCB space and allows for simplified integration. The PA's low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

Functional Block Diagram



Device (3.0 x 3.0 x 1.0mm)



Pin Description

| Pin # | Signal Name | Description |
|-------|-------------|--------------------------------|
| 1 | VCC1 | Supply Voltage to Input Stage |
| 2 | RF In | RF Input Signal |
| 3 | GND | Ground |
| 4 | VREF12 | Reference Voltage |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 | RF Out | RF Output Signal |
| 8 | VCC2 | Supply Voltage to Output Stage |
| 9 | GND | Ground |

Electrical Characteristics⁽¹⁾ OFDM Modulation

(176μs burst time, 100μs idle time) 54Mbps Data Rate, 16.7MHz Bandwidth

| Parameter | Min. | Typ. | Max. | Units |
|---------------------------------------|------|------|------|-------|
| Frequency | 2.3 | | 2.4 | GHz |
| Collector Supply Voltage (VCC1, VCC2) | 3.0 | 3.4 | 4.2 | V |
| Reference Supply Voltage (VREF12) | | 2.85 | | V |
| Reference Supply Current (VREF12) | | 8 | | mA |
| Gain | | 25.5 | | dB |
| Total Measured Current @ 22dBm Pout | | 225 | | mA |
| EVM @ 22dBm Pout ⁽²⁾ | | 2 | | % |
| PAE @ 22dBm Modulated Pout | | 16.5 | | % |

Electrical Characteristics⁽¹⁾ Single Tone

| Parameter | Min. | Typ. | Max. | Units |
|---------------------------------------|------|------|------|-------|
| Frequency | 2.3 | | 2.4 | GHz |
| Collector Supply Voltage (VCC1, VCC2) | 3.0 | 3.4 | 4.2 | V |
| Reference Supply Voltage (VREF12) | 2.7 | 2.85 | 3.1 | V |
| Gain | | 25.5 | | dB |
| Total Quiescent Collector Current | | 130 | | mA |
| Reference Current at pin (VREF12) | | 8 | | mA |
| P1dB Compression | | 30 | | dBm |
| Collector Current @ P1dB Compression | | 580 | | mA |
| Shutdown Current (VREF12 = 0V) | | ≤5 | | μA |
| Input Return Loss | | 20 | | dB |
| Output Return Loss | | 7 | | dB |
| Turn-On Time | | <1 | | μS |

Absolute Maximum Ratings⁽³⁾

| Symbol | Parameter | Ratings | Units |
|------------|----------------------------|-------------|-------|
| VCC1, VCC2 | Positive Supply Voltage | 5 | V |
| IC1, IC2 | Supply Current | | |
| | IC1 | 100 | mA |
| | IC2 | 900 | mA |
| VREF12 | Positive Reference Voltage | 3.1 | V |
| Pin | RF Input Power | +10 | dBm |
| Tcase | Case Operating Temperature | -40 to +85 | °C |
| Tstg | Storage Temperature | -55 to +150 | °C |

Notes:

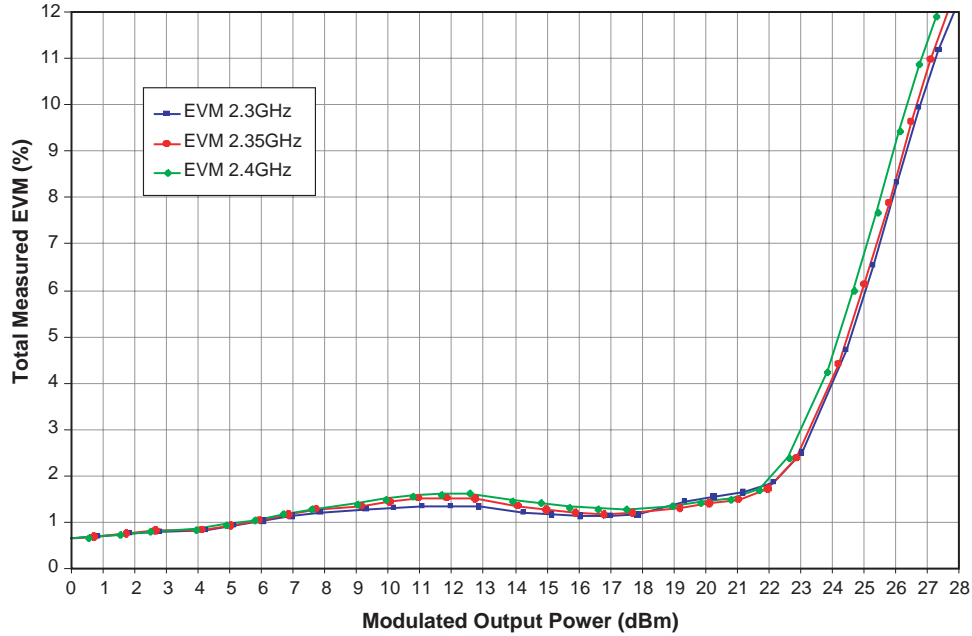
1. VCC1, VCC2 = 3.4V, VREF12 = 2.85V, T_A=25°C, PA is constantly biased, 50Ω system.
2. Percentage includes system noise floor of EVM = 0.8%.
3. No permanent damage with one parameter set at extreme limit. Other parameters set to typical values.

Performance Data OFDM Modulation

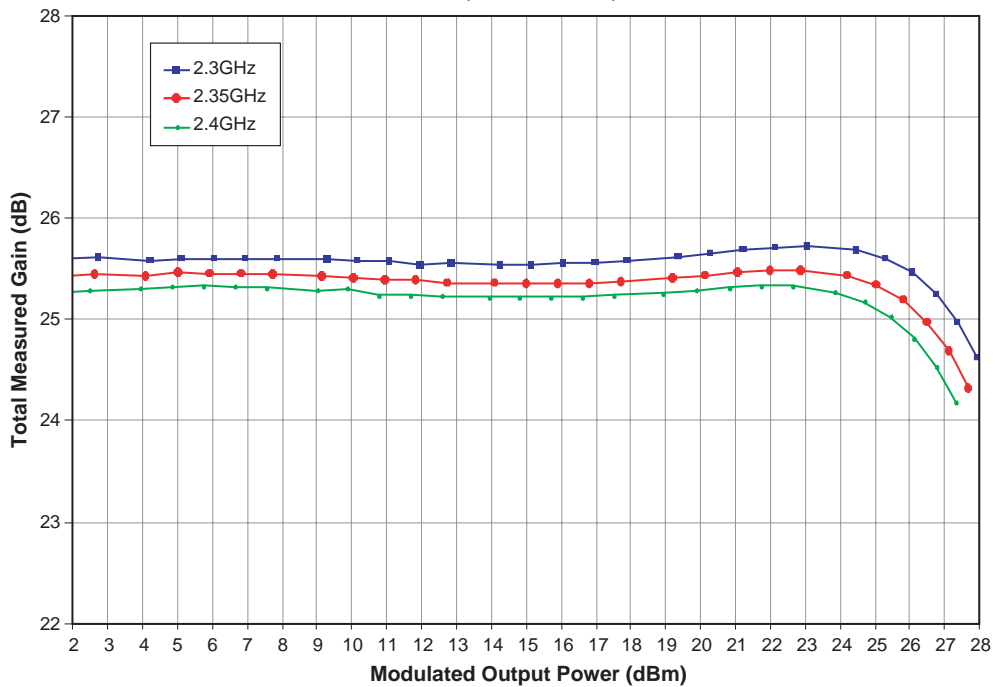
(with 176ms burst time, 100ms idle time) 54Mbps Data Rate, 16.7MHz Bandwidth

Note: Uncorrected EVM. Source EVM is approximately 0.8%.

Total Measured EVM vs. Modulated Output Power
 Vref = 2.85V, Vc12 = 3.4V, T = 25°C

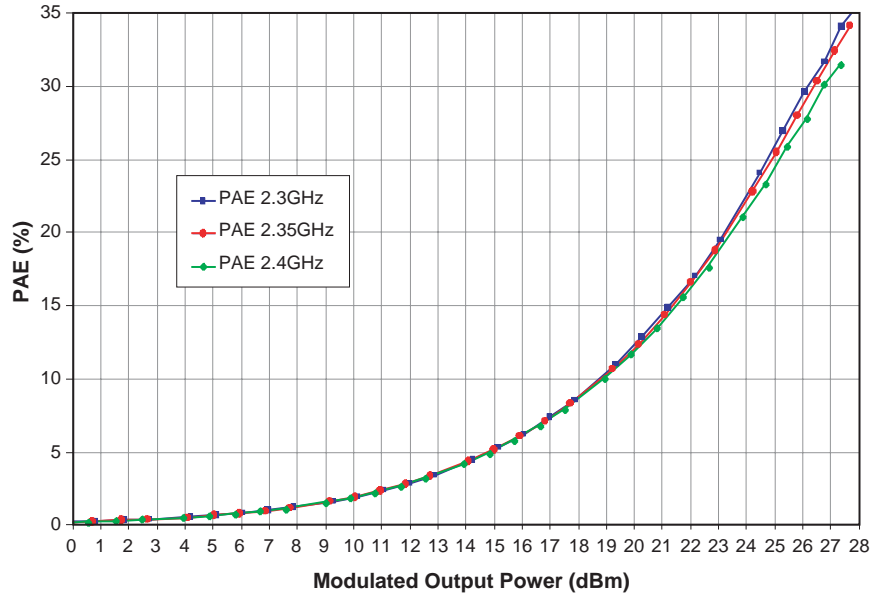


Total Measured Gain vs. Modulated Output Power
 Vref = 2.85V, Vc12 = 3.4V, T = 25°C

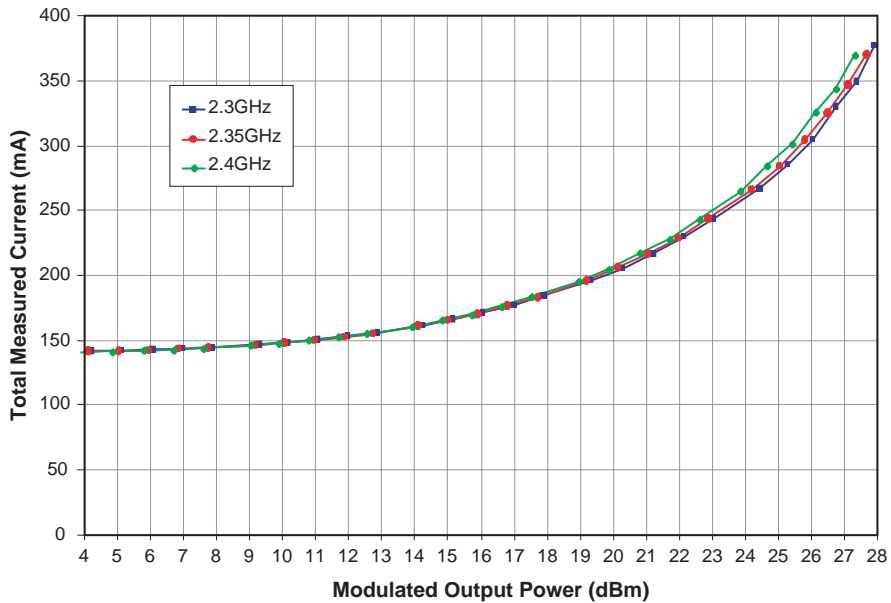


Performance Data OFDM Modulation (Continued)
 (with 176ms burst time, 100ms idle time) 54Mbps Data Rate, 16.7MHz Bandwidth
Note: Uncorrected EVM. Source EVM is approximately 0.8%.

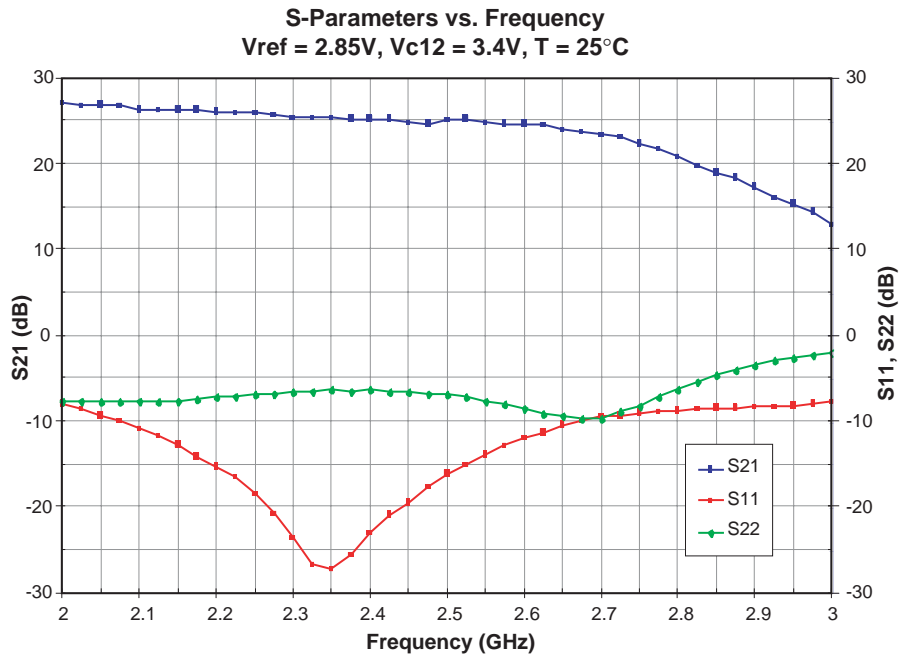
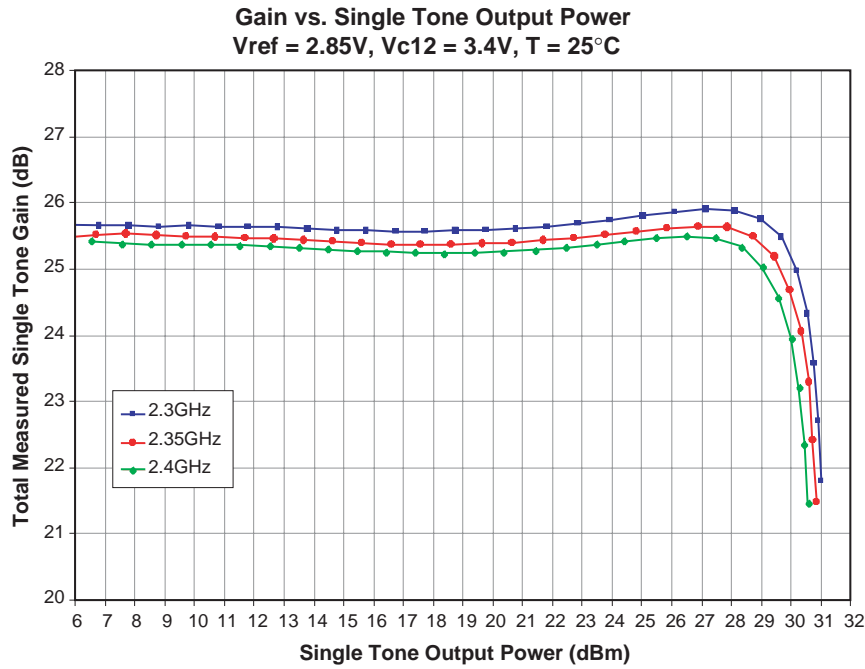
PAE vs. Modulated Output Power
 Vref = 2.85V, Vc12 = 3.4V, T = 25°C



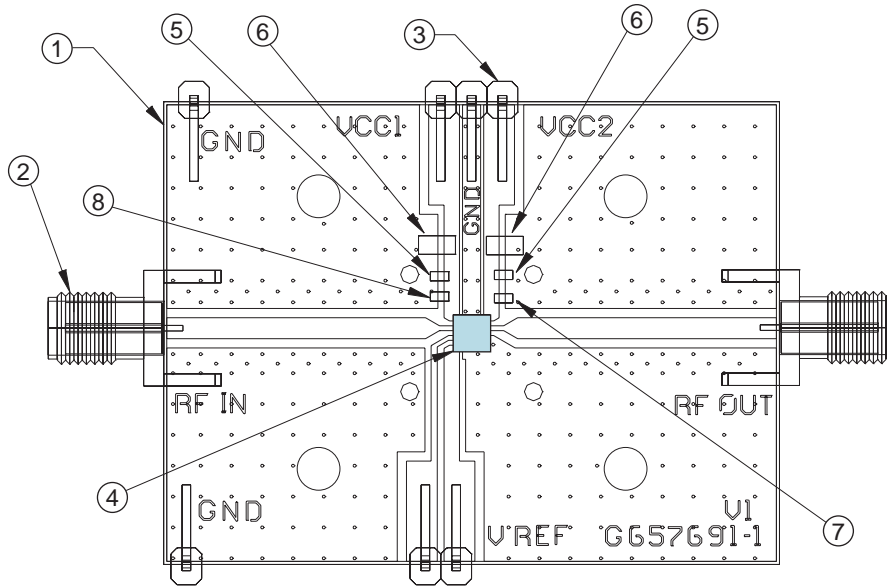
Total Measured Current vs. Modulated Output Power
 Vref = 2.85V, Vc12 = 3.4V, T = 25°C



Performance Data Single Tone



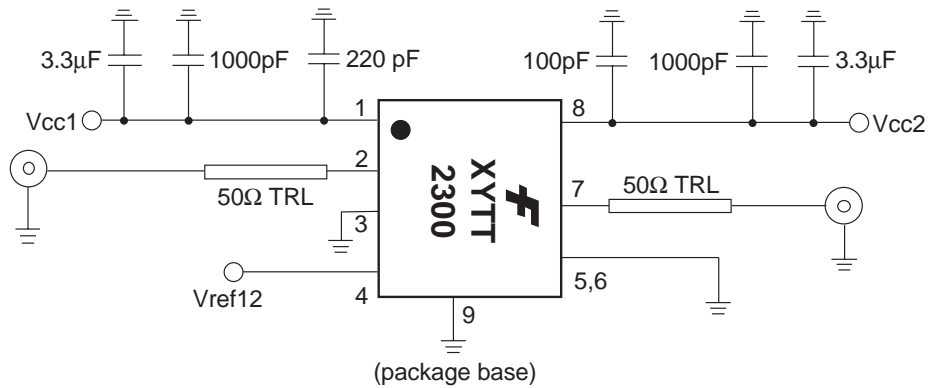
Evaluation Board Layout



MATERIALS LIST

| QTY | ITEM NO. | PART NUMBER | DESCRIPTION | VENDOR |
|-----|----------|--------------------|--------------------------|-----------|
| 1 | 1 | G657691-1 VI | PC, BOARD | FAIRCHILD |
| 2 | 2 | #142-0701-841 | SMA CONNECTOR | JOHNSON |
| 7 | 3 | #2340-5211TN | TERMINALS | 3M |
| REF | 4 | | ASSEMBLY, FMPA2300 | FAIRCHILD |
| 3 | 5 | GRM39X7R102K50V | 1000 pF CAPACITOR (0603) | MURATA |
| 3 | 5 (ALT) | ECJ-1VB1H102K | 1000 pF CAPACITOR (0603) | PANASONIC |
| 2 | 6 | C3216X5R1A335M | 3.3 uF CAPACITOR (1206) | TDK |
| 1 | 7 | GRM36C0G101J50Z500 | 100pF CAPACITOR (0402) | MURATA |
| 1 | 8 | GRM36C0G221J50D500 | 220pF CAPACITOR (0402) | MURATA |

Evaluation Board Schematic



Evaluation Board Turn-On Sequence⁽⁴⁾

Recommended turn-on sequence:

1. Connect common ground terminal to the Ground (GND) pin on the board.
2. Apply positive supply voltage VC1 (=3.4V) to pin VCC1 (first stage collector).
3. Apply positive supply voltage VC2 (=3.4V) to pin VCC2 (second stage collector).
4. Apply positive bias voltage VREF12 (=2.85V) to pin VREF (bias networks).
5. At this point, you should expect to observe the following positive currents flowing into the pins:

| Pin | Current |
|--------|-------------|
| VREF12 | 7.0–9.0mA |
| VCC1 | 50.0–60.0mA |
| VCC2 | 70.0–80.0mA |

6. Apply input RF power to SMA connector pin RFIN. Currents in pins VC1 and VC2 will vary depending on the input drive level.
7. Vary positive voltage on pin VREF12 from +2.85 V to +0 V to shut down the amplifier or alter the power level.

Shut down current flow into the pins:

| Pin | Current |
|------|---------|
| VCC1 | <1nA |
| VCC2 | <1nA |

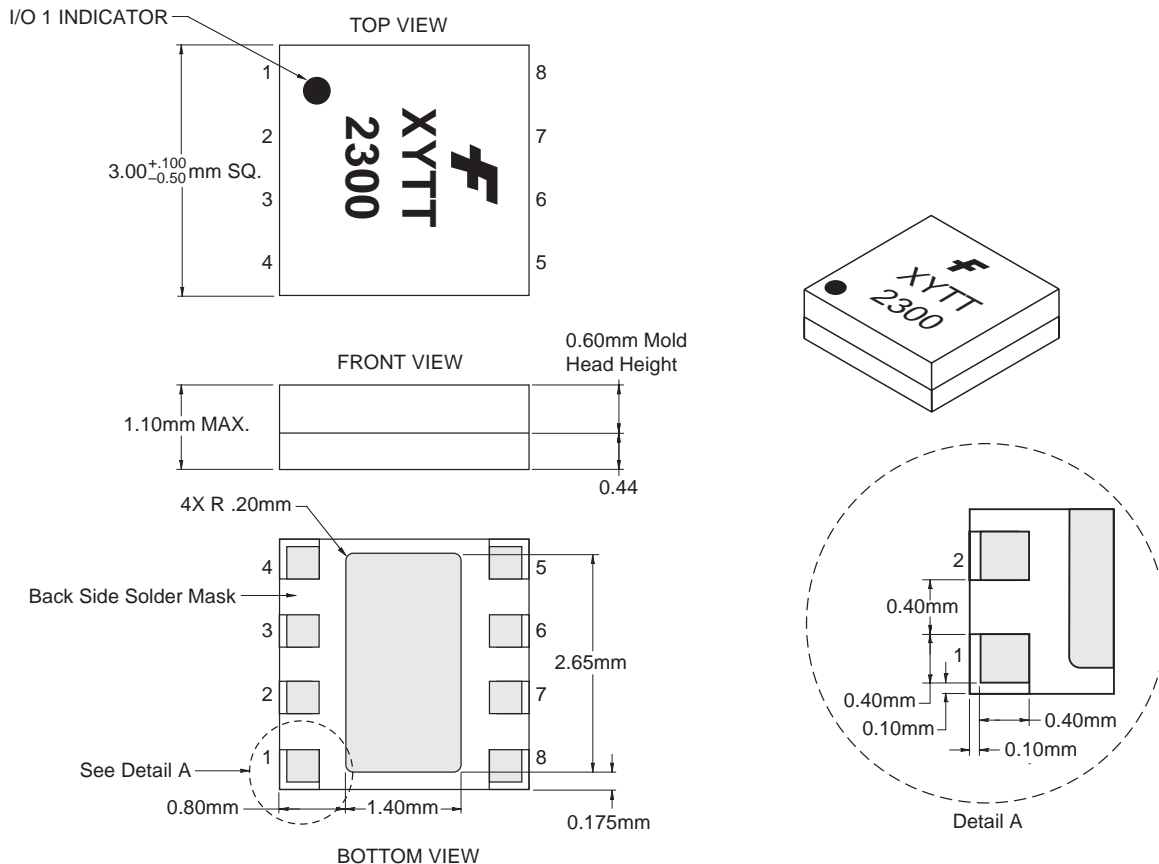
Recommended turn-off sequence:

Use reverse order described in the turn-on sequence above.

Note:

4. Turn on sequence is not critical and it is not necessary to sequence power supplies in actual system level design.

Package Outline



Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
 - A properly grounded static-dissipative surface on which to place devices.
 - Static-dissipative floor or mat.
 - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:

Fairchild recommends the following procedures prior to assembly.

- Assemble the devices within 7 days of removal from the dry pack.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure, at 125°C for 24 hours minimum, must be performed.

Solder Materials & Temperature Profile:

Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

Reflow Profile

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A maximum heating rate is 3°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 60-180 seconds at 150-200°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 20 seconds. Soldering temperatures should be in the range 255–260°C, with a maximum limit of 260°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

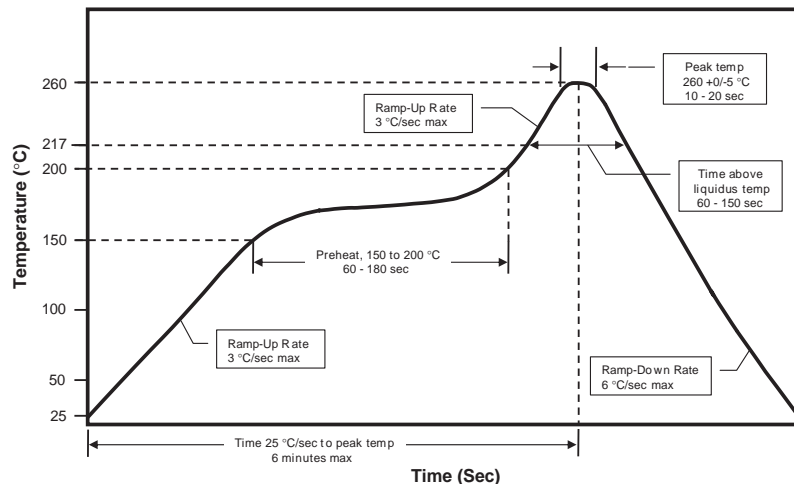
Solder Joint Characteristics:

Proper operation of this device depends on a reliable void-free attachment of the heat sink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:

Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should be subjected to no more than 15°C above the solder melting temperature for no more than 5 seconds. No more than 2 rework operations should be performed.

Recommended Solder Reflow Profile



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