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FMS6363A
Three-Channel 7th-Order High-Definition VoltagePlus™ Video Filter Driver

Features

- Three 7th-Order 32MHz (HD) Filters
- Drives Single AC-or DC-Coupled Video Loads (150Ω)
- Drives Dual AC-or DC-Coupled Video Loads (75Ω)
- Transparent Input Clamping
- Single Supply: 3.3V – 5V
- AC-or DC-Coupled Inputs and Outputs
- DC-Coupled Output Eliminates AC-Coupling Capacitor
- Robust 9kV ESD Protection
- Lead-Free SOIC-8 Package

Applications

- Cable Set-Top Boxes
- Satellite Set-Top Boxes
- DVD Players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6363A VoltagePlus™ video filter is intended to replace passive LC filters and drivers with a cost-effective integrated device. The three 7th-order filters provide improved frequency response performance over the FMS6363 and other 3-channel HD VFD devices.

The FMS6363A may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC coupled inputs are required *(see Applications section for details).*

The outputs can drive AC-or DC-coupled single (150Ω) or dual (75Ω) video loads. DC coupling the outputs removes the need for large output coupling capacitors. The input DC levels are offset approximately +280mV at the output *(see Applications section for details).*

Related Resources

AN-6024 – FMS6xxx Product Series Understanding Analog Video Signal Clamps, Bias, DC Restore, and AC or DC coupling Methods

AN-6041 – PCB Layout Considerations for Video Filter/Drivers

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method	Quantity
FMS6363ACSX	-40°C to +85°C	8-Lead SOIC	Reel	2500

Block Diagram

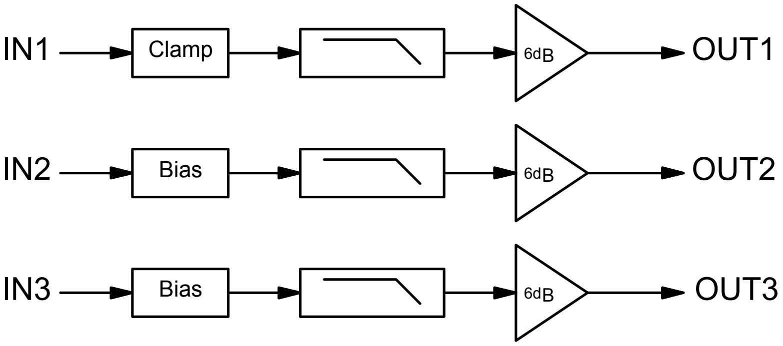


Figure 1. 7th-Order 30MHz Filter

Pin Configuration

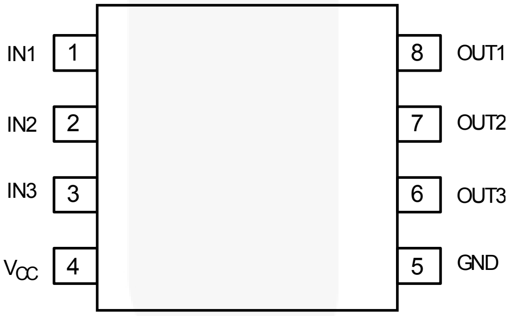


Figure 2. Pin Configuration

Pin Definitions

Pin#	Name	Type	Description
1	IN1	Input	Video Input Channel 1
2	IN2	Input	Video Input Channel 2
3	IN3	Input	Video Input Channel 2
4	V_{CC}	Input	Positive Power Supply
5	GND	Input	Device Ground Connection
6	OUT3	Output	Filtered Output Channel 3
7	OUT2	Output	Filtered Output Channel 2
8	OUT1	Output	Filtered Output Channel 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_S	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
V_{OUT}	Maximum Output Current, Do Not Exceed		50	mA

ESD Information

Symbol	Parameter	Min	Unit
ESD	Human Body Model, JESD22-A114	9	kV
	Charged Device Model, JESD22-C101	2	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature (Soldering, 10s)			+300	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air	115			°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	Supply Voltage Range	3.14	3.30	5.25	V

DC Electrical Characteristics

Unless otherwise noted T_A=25°C, V_{CC}=3.3V, R_S=37.5Ω; all inputs are AC-coupled with 0.1μF; all output AC-coupled with 220μF into 150Ω load.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Supply						
V_S	Supply Voltage Range	V_S Range	3.14	3.30	5.25	V
I_{CC}	Quiescent Supply Current(1)	V_S=+3.3V, No Load		22	35	mA
		V_S=+5V, No Load		34	40	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC Coupled	1.4			V_{PP}
PSRR	Power Supply Rejection Ratio	DC (All Channels)		-60		dB

AC Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{CC}=3.3V, R_S=37.5Ω; all inputs are AC-coupled with 0.1μF; all outputs AC-coupled with 220μF into 150Ω load.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV	Channel Gain	Active Video Input Range = 1V_{PP}	5.8	6.0	6.2	dB
$BW_{0.5dB}$	±0.5dB Bandwidth	R_{SOURCE}=75Ω, R_L=150Ω	28			MHz
$BW_{-1.0dB}$	-1.0 dB Bandwidth		26	30		MHz
$BW_{3.0dB}$	-3.0 dB Bandwidth		30	34		MHz
$Att_{37.125M}$	Normalized Stopband Attenuation	R_{SOURCE}=75Ω, f=37.325MHz		6.5		dB
$Att_{44.25M}$		R_{SOURCE}=75Ω, f=44.25MHz		14.5		
$Att_{74.25M}$		R_{SOURCE}=75Ω, f=74.25MHz	40	44		
Att_{78M}		R_{SOURCE}=75Ω, f=78MHz		46		
THD1	Output Distortion (All Channels)	f=10 MHz; V_{OUT}=1.4V_{PP}		-49		dBC
THD2		f=15 MHz; V_{OUT}=1.4V_{PP}		-48		
THD3		f=22 MHz; V_{OUT}=1.4V_{PP}		-45		
X_{talk}	Crosstalk (Channel-to-Channel)	f=1.00 MHz; V_{OUT}=1.4V_{PP}		-65		dB
SNR	Peak Signal to RMS Noise	Unweighted: 30MHz Lowpass, 100kHz to 30MHz	65			dB
t_{pd}	Propagation Delay	Delay from Input to Output; 100KHz to 28MHz	12			ns

Typical Application

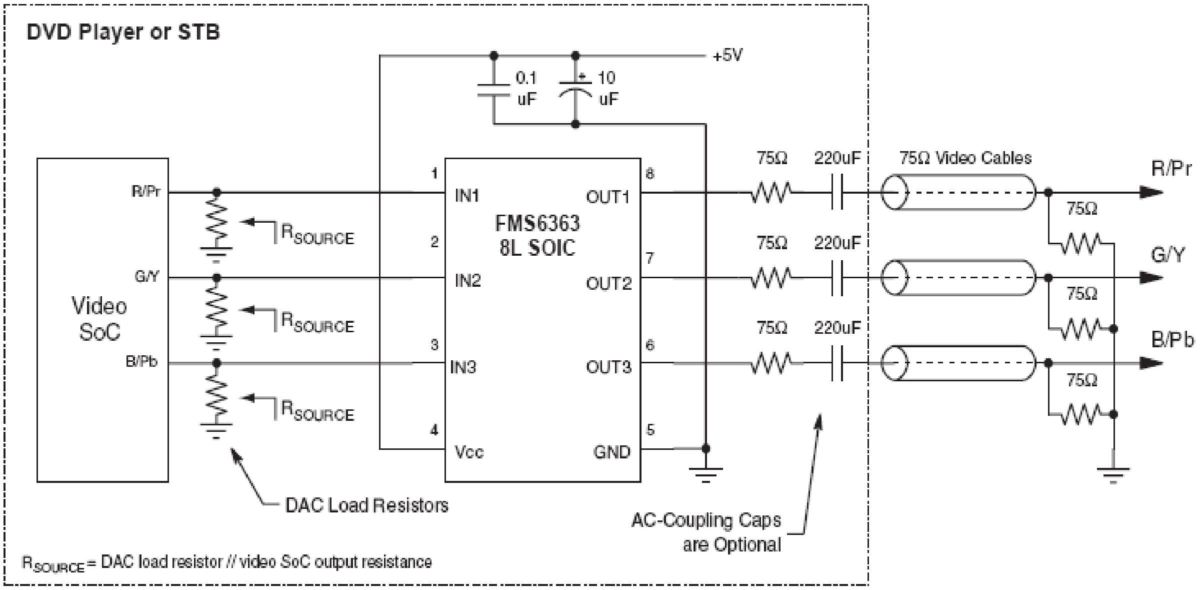
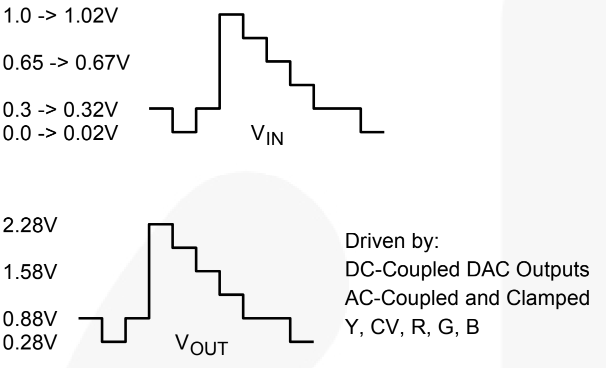


Figure 3. Typical Application

Application Information

Application Circuits

The FMS6363A VoltagePlus™ video filter provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 4:



There is a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$.

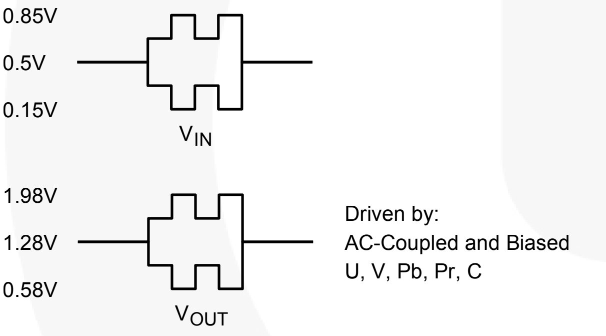


Figure 4. Typical Voltage Levels

The FMS6363A provides an internal diode clamp to support AC coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6363A without an AC coupling capacitor. When the input is AC coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp can not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb, and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 5.

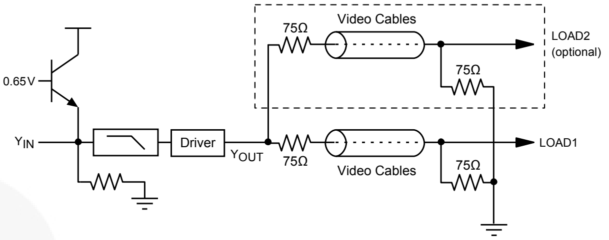


Figure 5. Input Clamp Circuit

I/O Configurations

For a DC-coupled DAC drive with DC-coupled outputs, use this configuration:

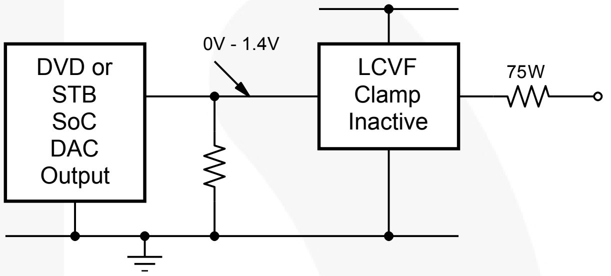


Figure 6. DC-Coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC coupled as follows:

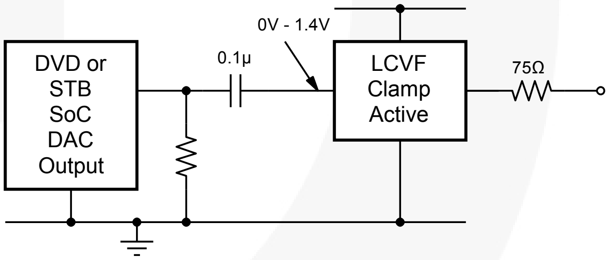


Figure 7. AC-Coupled Inputs, DC-Coupled Outputs

When the FMS6363A is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC-coupled like this:

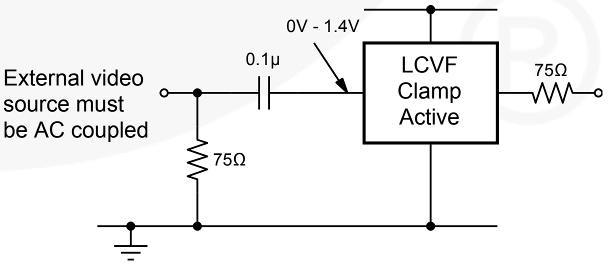


Figure 8. SCART with DC-Coupled Outputs

The same method can be used for biased signals. The Pb and Pr channels are baised to set the DC level to 500mV.

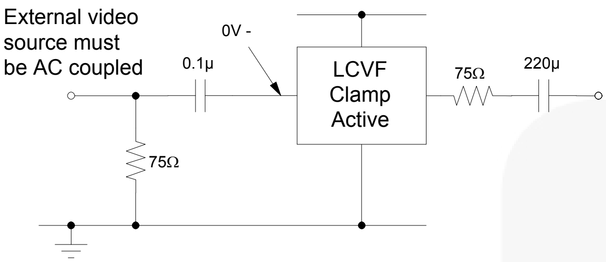


Figure 9. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

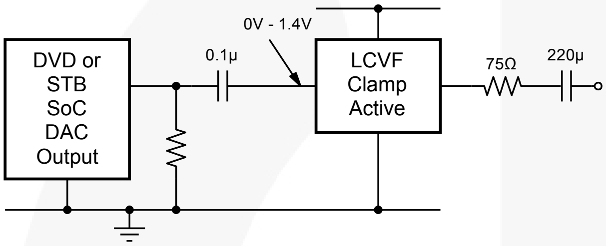


Figure 10. DC-Coupled Inputs, AC-Coupled Outputs

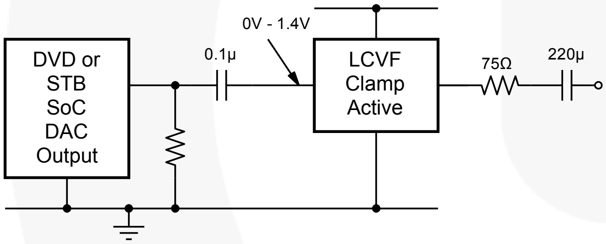


Figure 11. AC-Coupled Inputs and Outputs

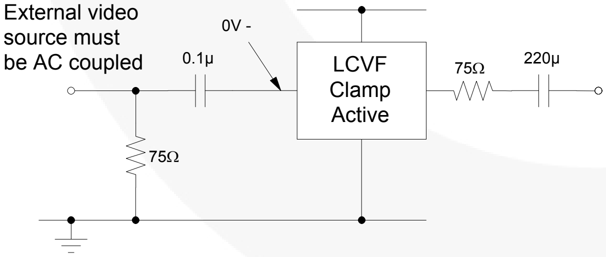


Figure 12. Biased SCART with AC-Coupled Outputs

Note:

1. The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6363A output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the power dissipation and internal temperature rise:

$$T_J = T_A + P_d \cdot \theta_{JA} \quad (1)$$

where:

$$P_d = P_{CH1} + P_{CH2} + P_{CH3} \quad (2)$$

$$P_{CHx} = V_{CC} \cdot I_{CH} - (V_O^2/R_L) \quad (3)$$

where:

$$V_O = 2V_{IN} + 0.280V \quad (4)$$

$$I_{CH} = (I_{CC}/3) + (V_O/R_L) \quad (5)$$

V_{IN} = RMS value of input signal

I_{CC} = 22mA

V_{CC} = 3.3V

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations* section for details.

The FMS6363A is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75 Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief-duration short-circuit conditions. This capability is not guaranteed.

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a evaluation board to guide layout and aid device evaluation. The evaluation board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing / Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90° angles.
- Minimize clock and video data trace length differences.
- Include 10µF and 0.1µF ceramic power supply bypass capacitors.
- Place the 0.1µF capacitor within 2.54mm (0.1in) of the device power pin.
- Place the 10µF capacitor within 19.05mm (0.75in) of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 12.7mm (0.5in) on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Output Considerations

The FMS6363A outputs are DC offset from the input by 150mV; therefore, $V_{OUT} = 2 \cdot V_{IN}$ DC+150mV. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6363A has a 2x (6dB) gain, the output is typically connected via a 75Ω-series back-matching resistor followed by the 75Ω video cable. Due to the inherent divide-by-two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC-coupling the output, ensure that the coupling capacitor of choice passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. Distance from the device pin to the series termination resistor should be no greater than 2.54mm (0.1in).

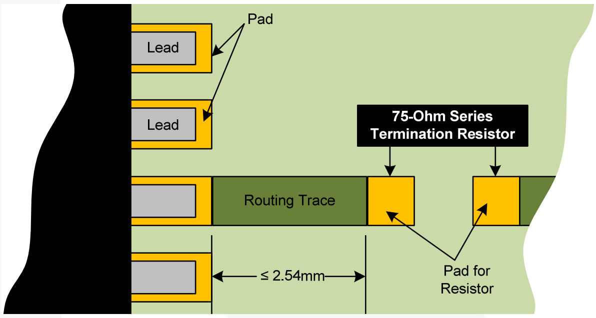


Figure 13. Termination Resistor

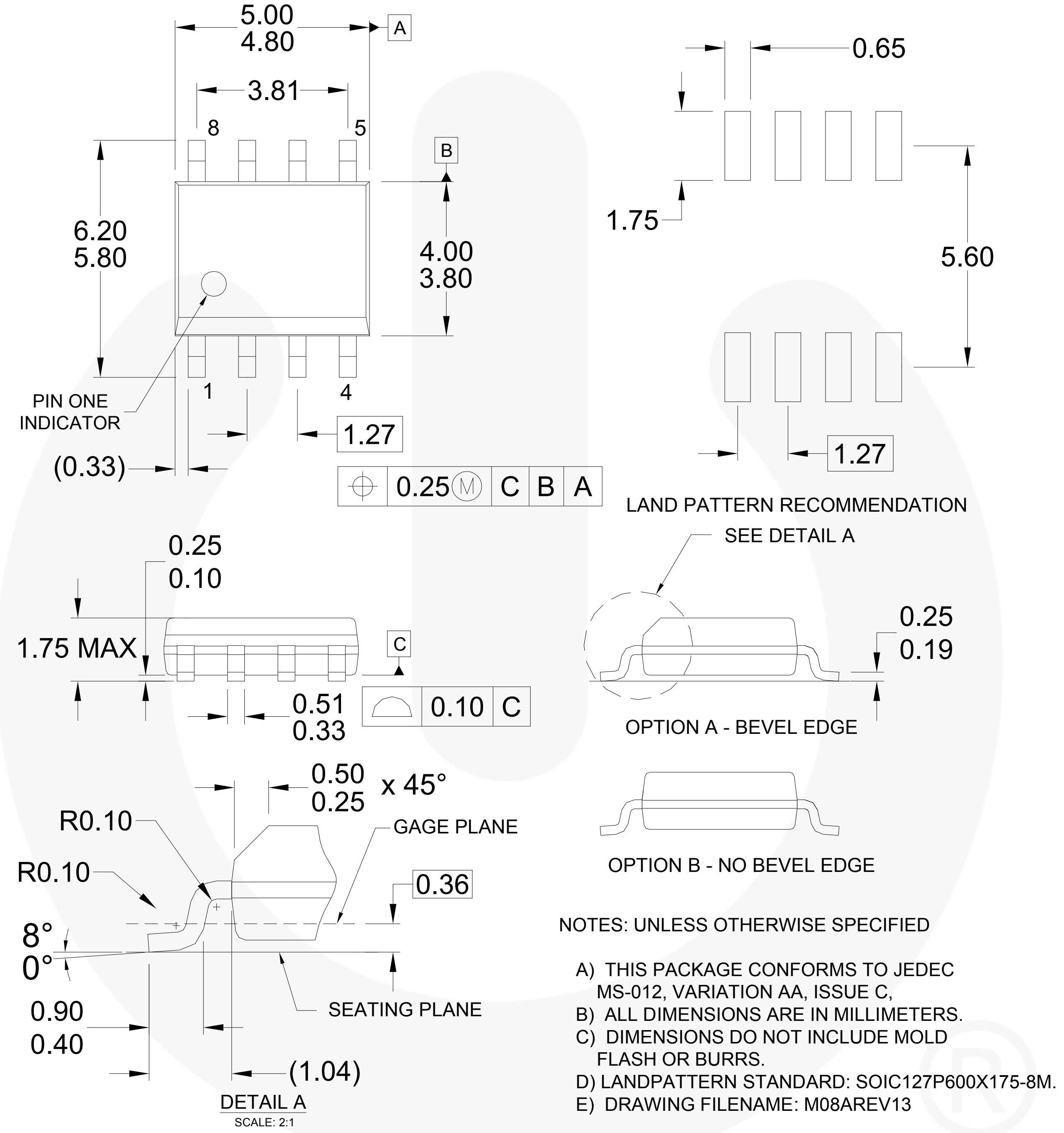
Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players, are at +70ºC; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane), each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70µm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in the power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Use modeling techniques to provide a first-order approximation.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 14. 8-Lead Small Outline Integrated Circuit (SOIC)

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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