

FMW20N60S1HF

FUJI POWER MOSFET

Super J-MOS series

N-Channel enhancement mode power MOSFET

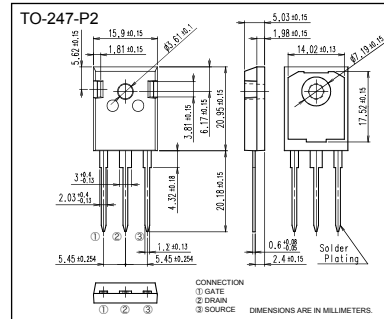
Features

- Low on-state resistance
- Low switching loss
- easy to use (more controllable switching dV/dt by R_g)

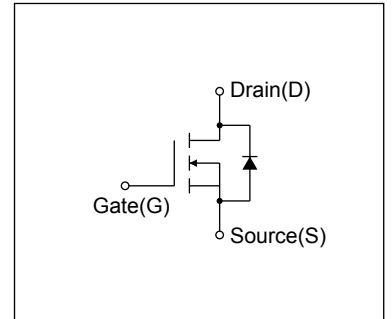
Applications

- UPS
- Server
- Telecom
- Power conditioner system
- Power supply

Outline Drawings [mm]



Equivalent circuit schematic



Maximum Ratings and Characteristics

Absolute Maximum Ratings at $T_c=25^\circ\text{C}$ (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	$V_{GS}=-30\text{V}$
Continuous Drain Current	I_D	± 20	A	$T_c=25^\circ\text{C}$ Note*1
		± 12.6	A	$T_c=100^\circ\text{C}$ Note*1
Pulsed Drain Current	I_{DP}	± 60	A	
Gate-Source Voltage	V_{GS}	± 30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AR}	6.6	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E_{AS}	472.2	mJ	Note *3
Maximum Drain-Source dV/dt	dV_{DS}/dt	50	kV/ μs	$V_{DS} \leq 600\text{V}$
Peak Diode Recovery dV/dt	dV/dt	15	kV/ μs	Note *4
Peak Diode Recovery $-di/dt$	$-di/dt$	100	A/ μs	Note *5
Maximum Power Dissipation	P_D	2.5	W	$T_a=25^\circ\text{C}$
		140		$T_c=25^\circ\text{C}$
Operating and Storage Temperature range	T_{ch}	150	$^\circ\text{C}$	
	T_{stg}	-55 to +150	$^\circ\text{C}$	

Note *1 : Limited by maximum channel temperature.

Note *2 : $T_{ch} \leq 150^\circ\text{C}$, See Fig.1 and Fig.2

Note *3 : Starting $T_{ch}=25^\circ\text{C}$, $I_{AS}=2\text{A}$, $L=216\text{mH}$, $V_{DD}=60\text{V}$, $R_G=50\Omega$, See Fig.1 and Fig.2

E_{AS} limited by maximum channel temperature and avalanche current.

Note *4 : $I_F \leq I_D$, $-di/dt=100\text{A}/\mu\text{s}$, $V_{DD} \leq 400\text{V}$, $T_{ch} \leq 150^\circ\text{C}$.

Note *5 : $I_F \leq I_D$, $dV/dt=15\text{kV}/\mu\text{s}$, $V_{DD} \leq 400\text{V}$, $T_{ch} \leq 150^\circ\text{C}$.

● Electrical Characteristics at T_c=25°C (unless otherwise specified)
Static Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA V _{GS} =0V	600	-	-	V
Gate Threshold Voltage	V _{GS(th)}	I _D =250μA V _{DS} =V _{GS}	2.5	3	3.5	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =600V V _{GS} =0V T _{ch} =25°C	-	-	25	μA
		V _{DS} =480V V _{GS} =0V T _{ch} =125°C	-	-	250	
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ± 30V V _{DS} =0V	-	10	100	nA
Drain-Source On-State Resistance	R _{DS(on)}	I _D =10A V _{GS} =10V	-	0.161	0.19	Ω
Gate resistance	R _G	f=1MHz, open drain	-	3.7	-	Ω
Forward Transconductance	g _{fs}	I _D =10A V _{DS} =25V	8.5	17.5	-	S
Input Capacitance	C _{iss}	V _{DS} =10V	-	1470	-	pF
Output Capacitance	C _{oss}	V _{GS} =0V	-	3120	-	
Reverse Transfer Capacitance	C _{rss}	f=1MHz	-	280	-	
Effective output capacitance, energy related (Note *6)	C _{o(er)}	V _{GS} =0V V _{DS} =0...480V	-	90	-	
Effective output capacitance, time related (Note *7)	C _{o(tr)}	V _{GS} =0V V _{DS} =0...480V I _D =constant	-	305	-	
Turn-On Time	t _{d(on)}	V _{DD} =400V, V _{GS} =10V I _D =10A, R _G =27Ω See Fig.3 and Fig.4	-	22	-	ns
	t _r		-	40	-	
Turn-Off Time	t _{d(off)}		-	162	-	
	t _f		-	22	-	
Total Gate Charge	Q _G	V _{DD} =480V, I _D =20A V _{GS} =10V See Fig.5	-	48	-	nC
Gate-Source Charge	Q _{GS}		-	12.5	-	
Gate-Drain Charge	Q _{GD}		-	15	-	
Drain-Source crossover Charge	Q _{SW}		-	8	-	
Avalanche Capability	I _{AV}	L=6.02mH, T _{ch} =25°C See Fig.1 and Fig.2	6.6	-	-	A
Diode Forward On-Voltage	V _{SD}	I _F =20A, V _{GS} =0V T _{ch} =25°C	-	0.9	1.35	V
Reverse Recovery Time	t _{rr}	I _F =20A, V _{GS} =0V V _{DD} =400V -di/dt=100A/μs T _{ch} =25°C		370	-	ns
Reverse Recovery Charge	Q _{rr}		-	6.2	-	μC
Peak Reverse Recovery Current	I _{rp}		See Fig.6	-	32	-

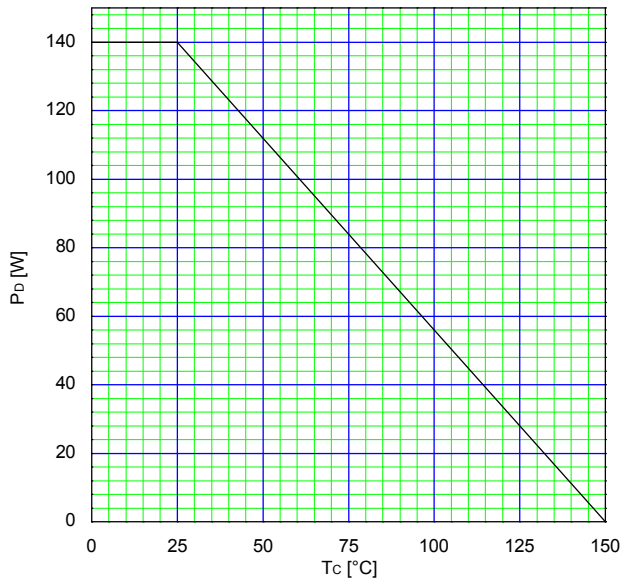
Note *6 : C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}.

Note *7 : C_{o(tr)} is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}.

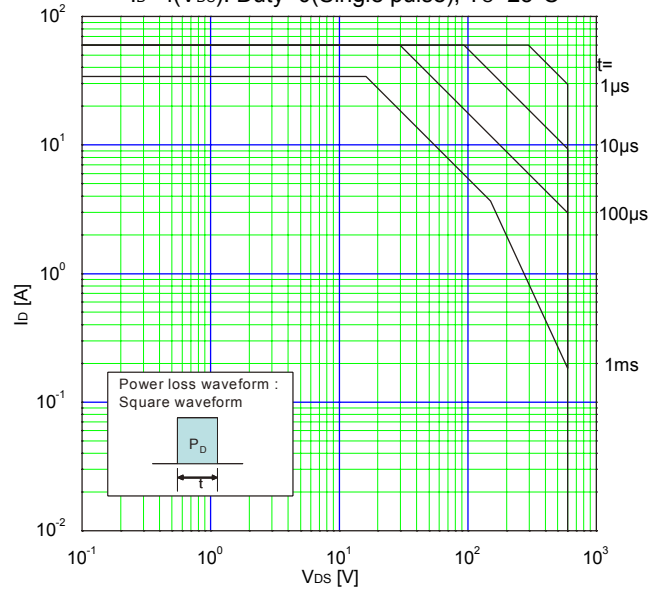
● Thermal Characteristics

Description	Symbol	min.	typ.	max.	Unit
Channel to Case	R _{th(ch-c)}			0.89	°C/W
Channel to Ambient	R _{th(ch-a)}			50	°C/W

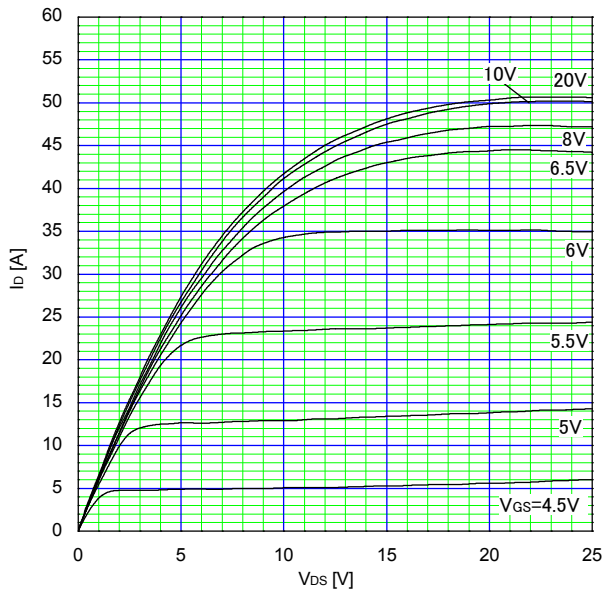
Allowable Power Dissipation
 $P_D = f(T_C)$



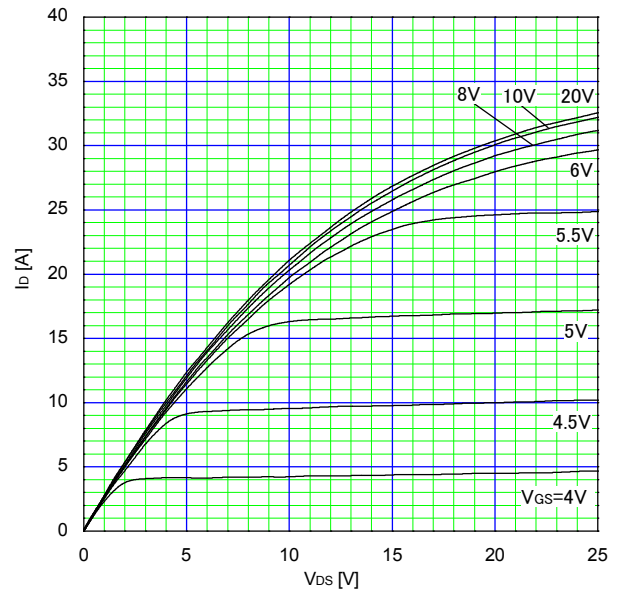
Safe Operating Area
 $I_D = f(V_{DS})$: Duty=0 (Single pulse), $T_C=25^\circ\text{C}$



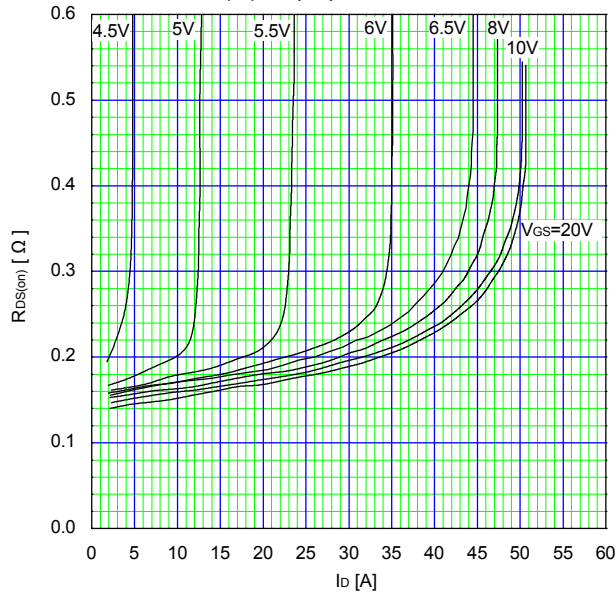
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80 μs pulse test, $T_{ch}=25^\circ\text{C}$



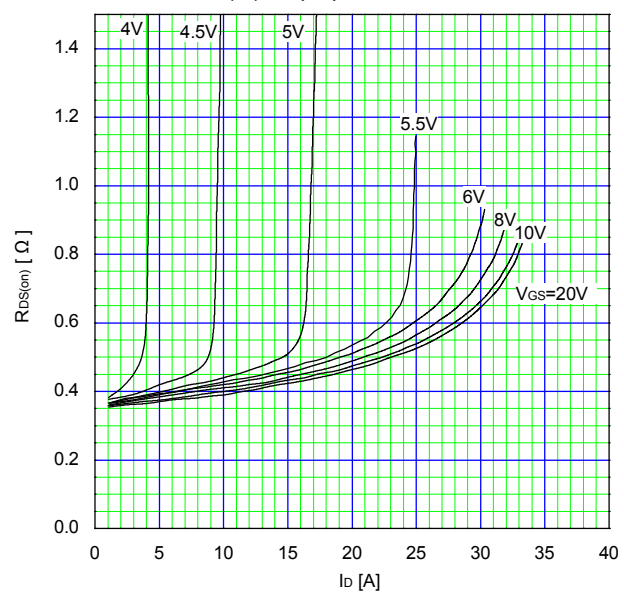
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80 μs pulse test, $T_{ch}=150^\circ\text{C}$



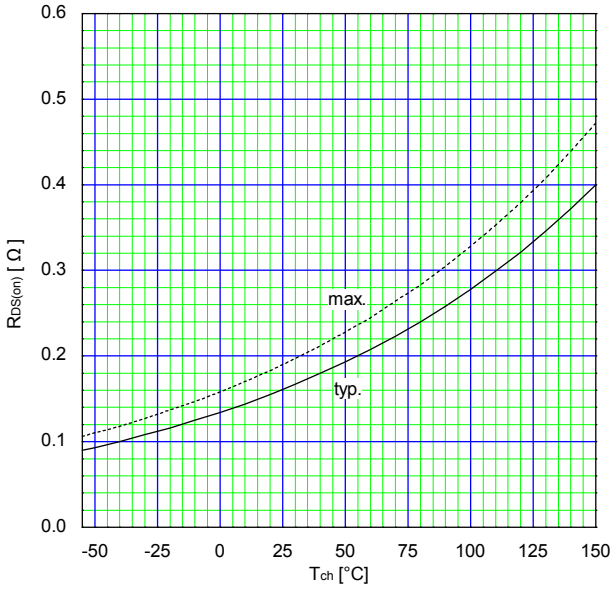
Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80 μs pulse test, $T_{ch}=25^\circ\text{C}$



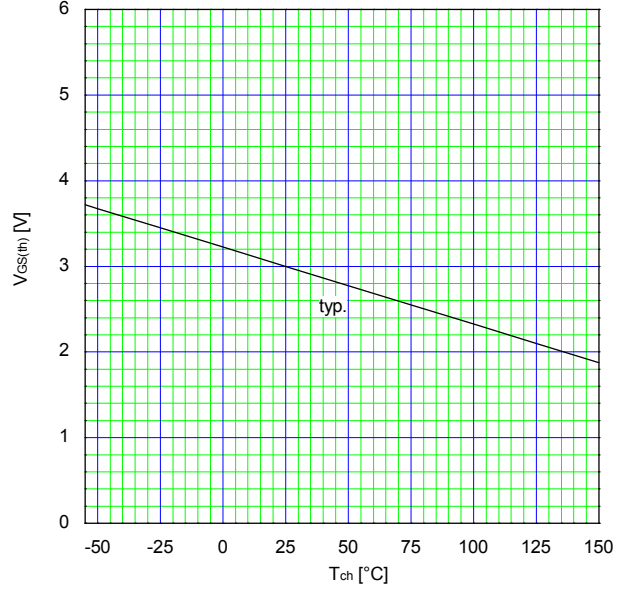
Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80 μs pulse test, $T_{ch}=150^\circ\text{C}$



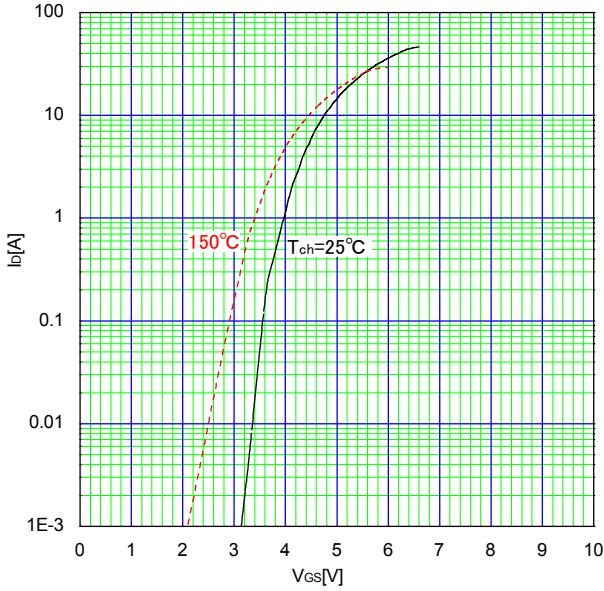
Drain-Source On-state Resistance
 $R_{DS(on)} = f(T_{ch})$: $I_D = 10A$, $V_{GS} = 10V$



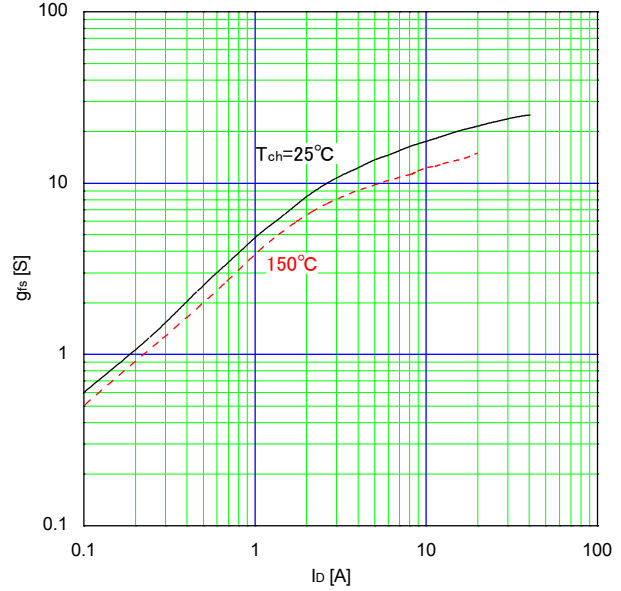
Gate Threshold Voltage vs. T_{ch}
 $V_{GS(th)} = f(T_{ch})$: $V_{DS} = V_{GS}$, $I_D = 250\mu A$



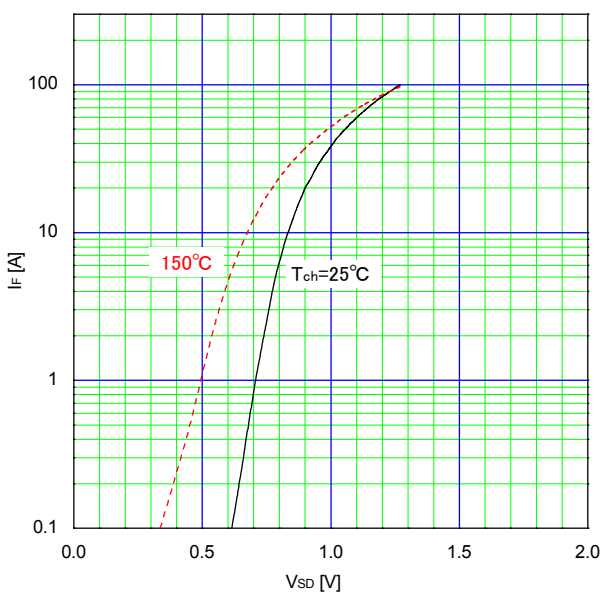
Typical Transfer Characteristic
 $I_D = f(V_{GS})$: $80\mu s$ pulse test, $V_{DS} = 25V$



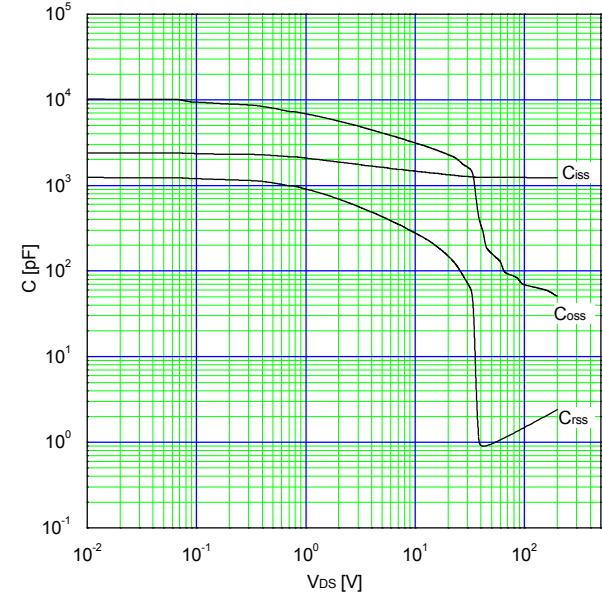
Typical Transconductance
 $g_{fs} = f(I_D)$: $80\mu s$ pulse test, $V_{DS} = 25V$



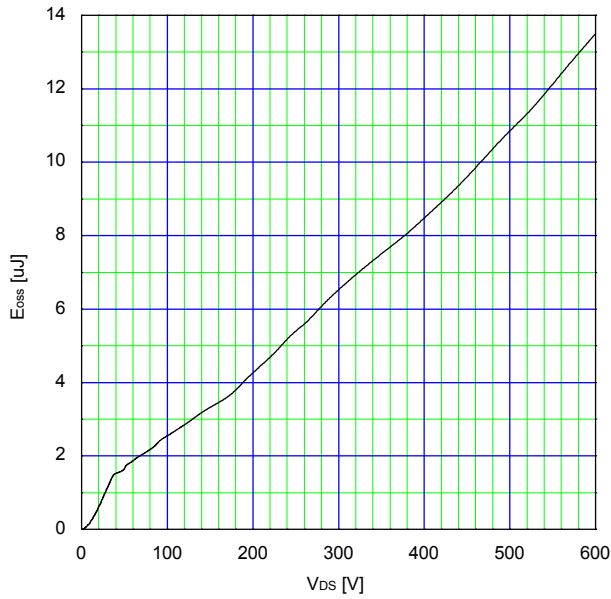
Typical Forward Characteristics of Reverse Diode
 $I_F = f(V_{SD})$: $80\mu s$ pulse test



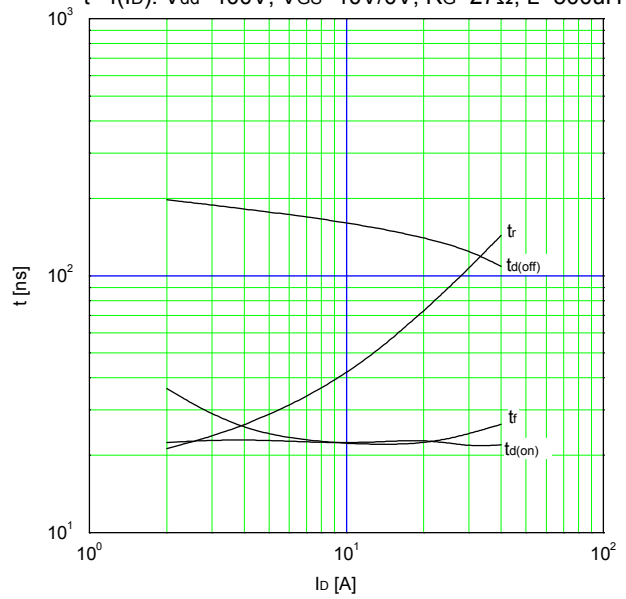
Typical Capacitance
 $C = f(V_{DS})$: $V_{GS} = 0V$, $f = 1MHz$



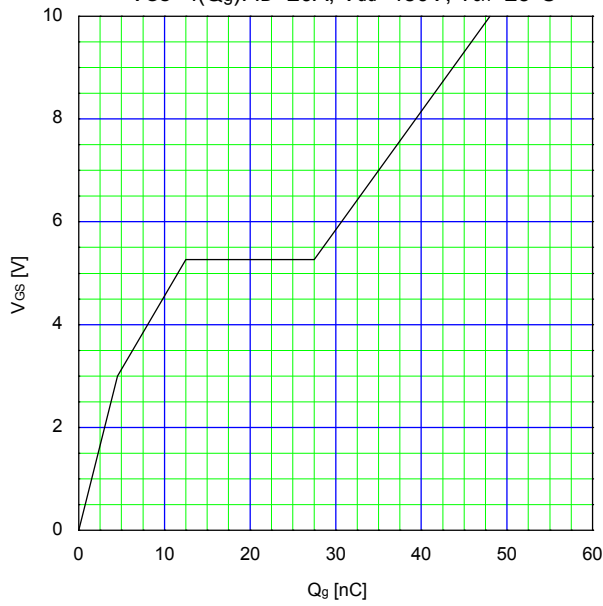
Typical Coss stored energy



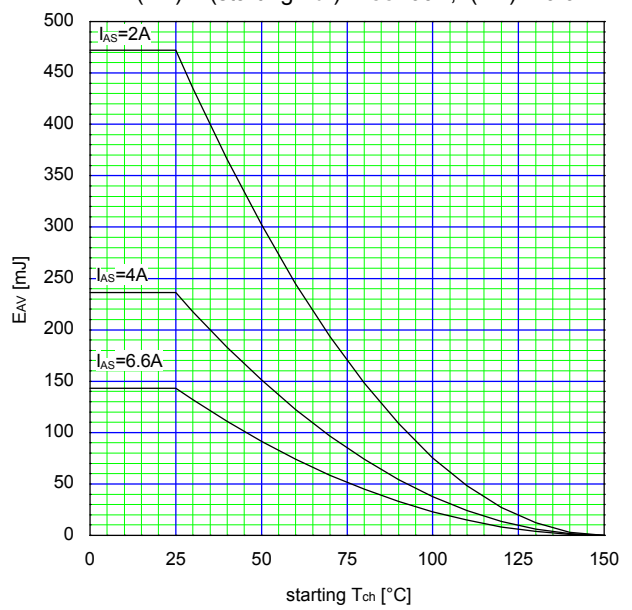
Typical Switching Characteristics vs. I_D T_{ch}=25°C
t = f(I_D): V_{dd}=400V, V_{GS}=10V/0V, R_G=27Ω, L=500uH



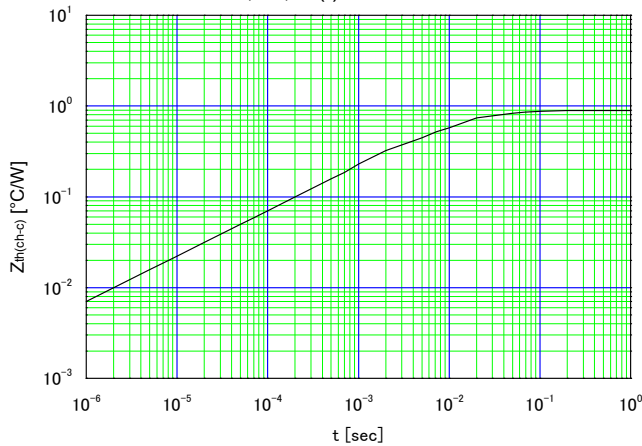
Typical Gate Charge Characteristics
V_{GS} = f(Q_g): I_D=20A, V_{dd}=480V, T_{ch}=25°C



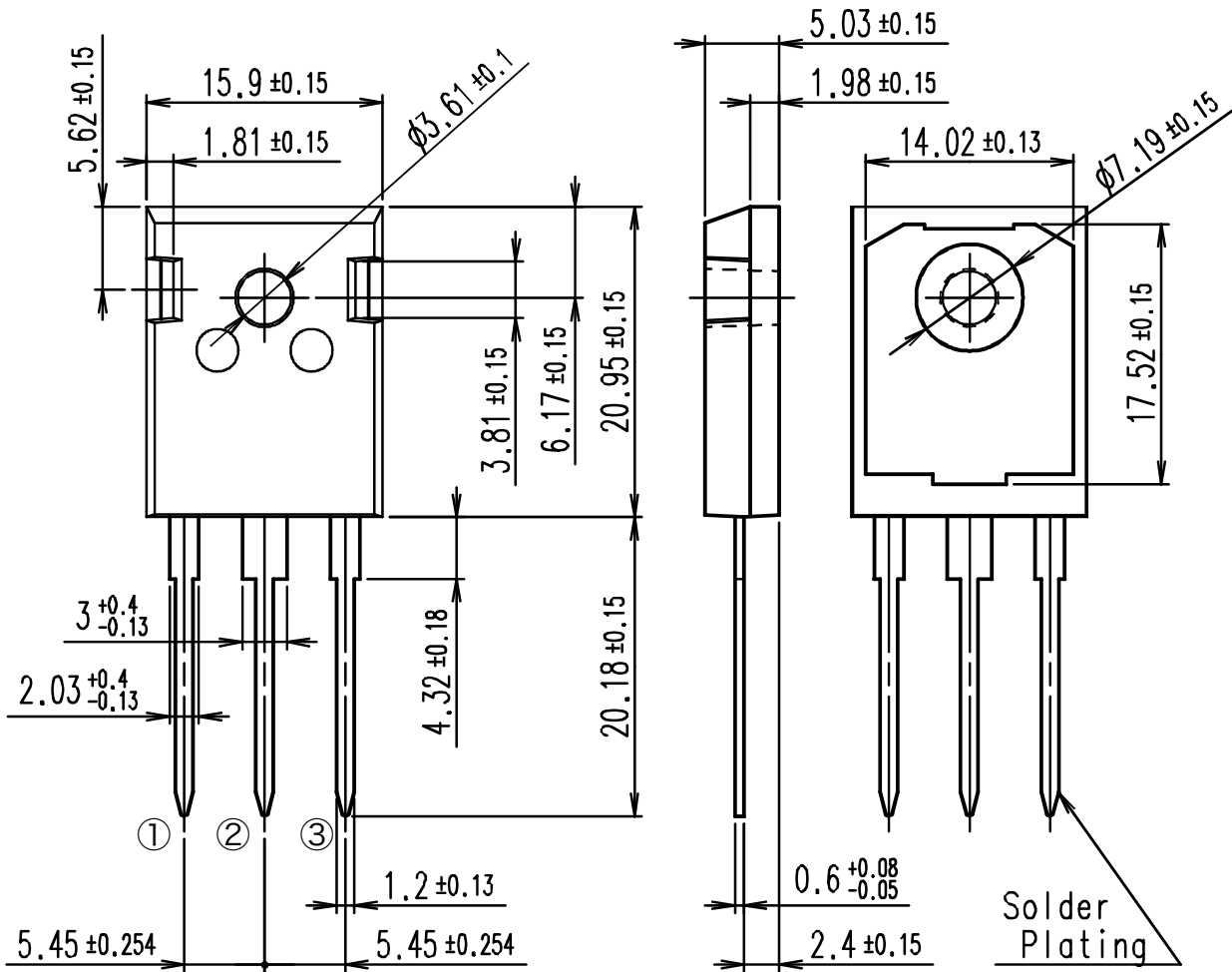
Maximum Avalanche Energy vs. starting T_{ch}
E(AV) = f(starting T_{ch}): V_{CC}=60V, I(AV) <= 6.6A



Transient Thermal Impedance
Z_{th(ch-c)} = f(t): D=0



■ Outview: TO-247-P2 Package

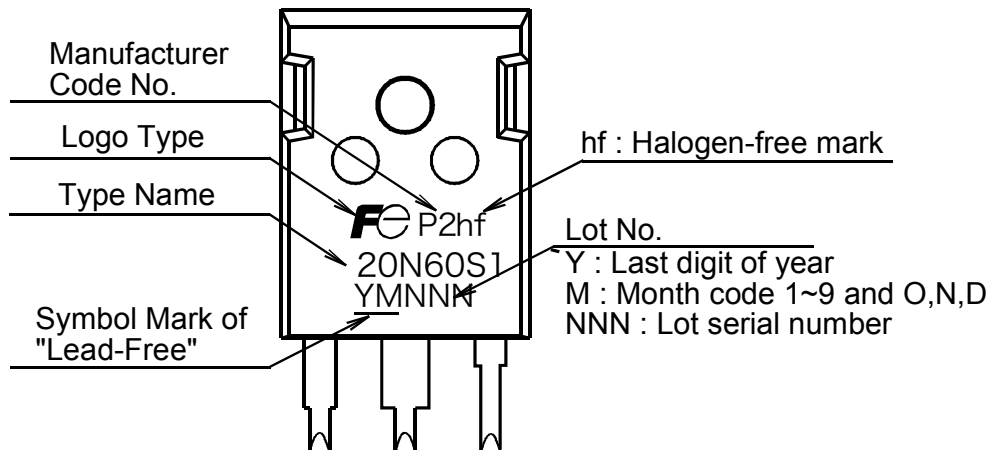


CONNECTION

- ① GATE
- ② DRAIN
- ③ SOURCE

DIMENSIONS ARE IN MILLIMETERS.

■ Marking



* The font (font type,size) and the logo type size might be actually different.

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