

## FNK P-Channel Enhancement Mode Power MOSFET

### Description

The FNK03P05E uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

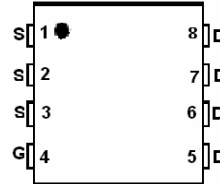
### General Features

- $V_{DS} = -30V, I_D = -50A$   
 $R_{DS(ON)} < 9m\Omega @ V_{GS} = -10V$

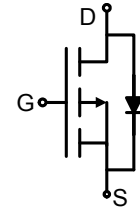
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

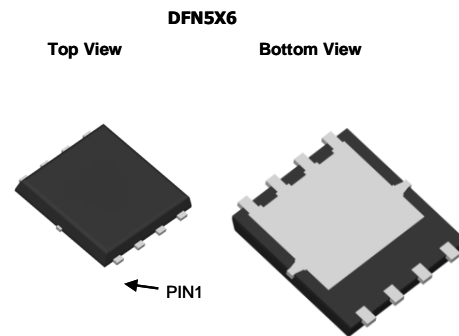
- Battery and loading switching



Marking and pin assignment



Schematic diagram



### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FNK03P05E	FNK03P05E	DFN 5x6 8L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-50	A
Pulsed Drain Current	$I_{DM}$	-200	A
Maximum Power Dissipation	$P_D$	35	W
Derating factor		0.28	$W/^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	300	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

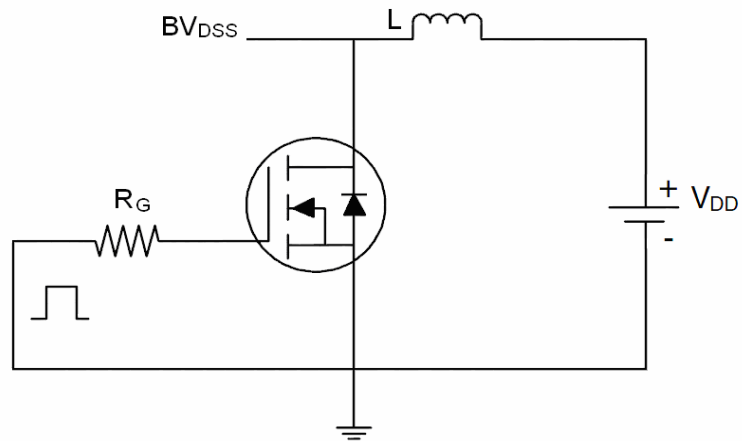
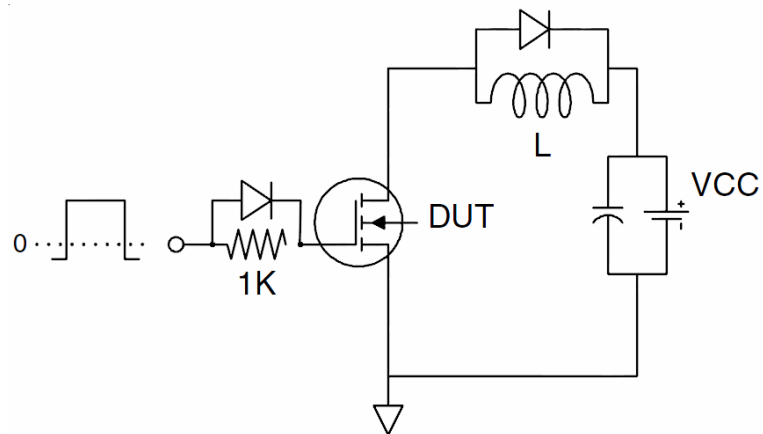
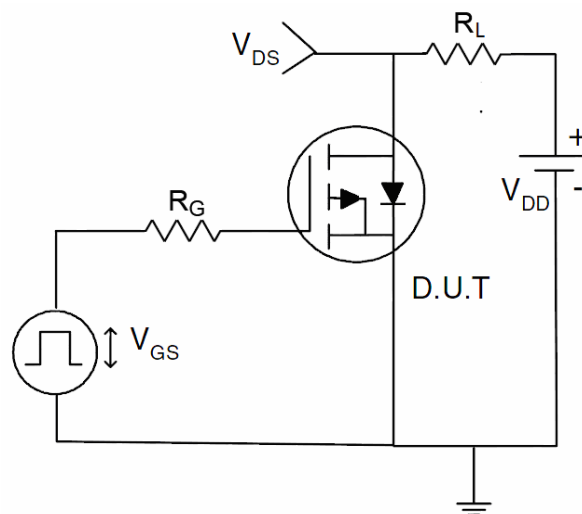
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3.6	$^\circ C/W$
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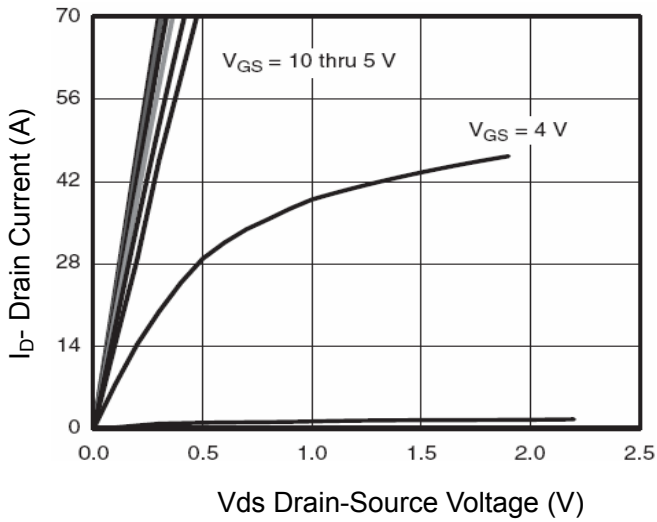
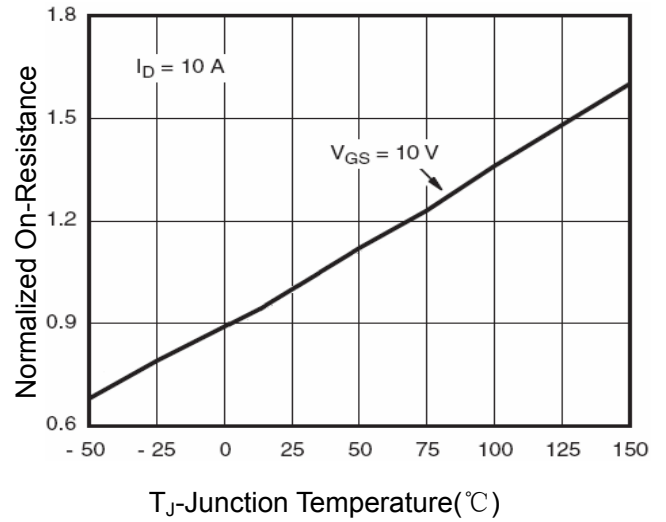
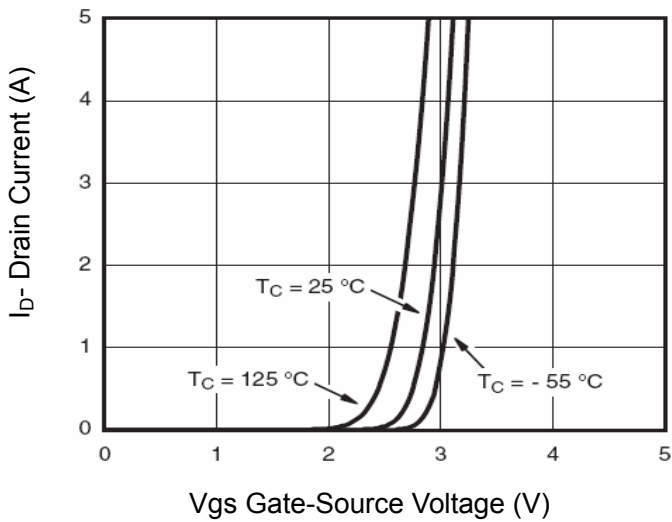
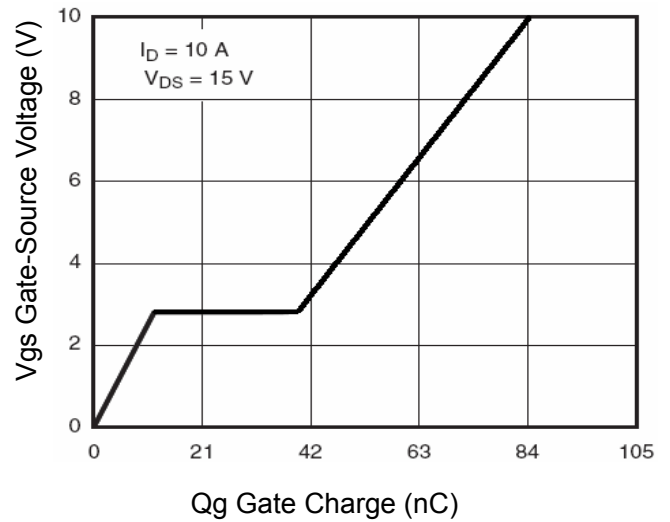
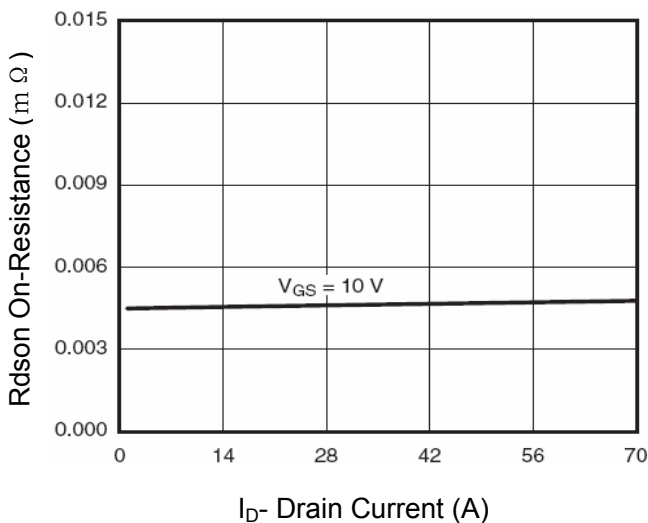
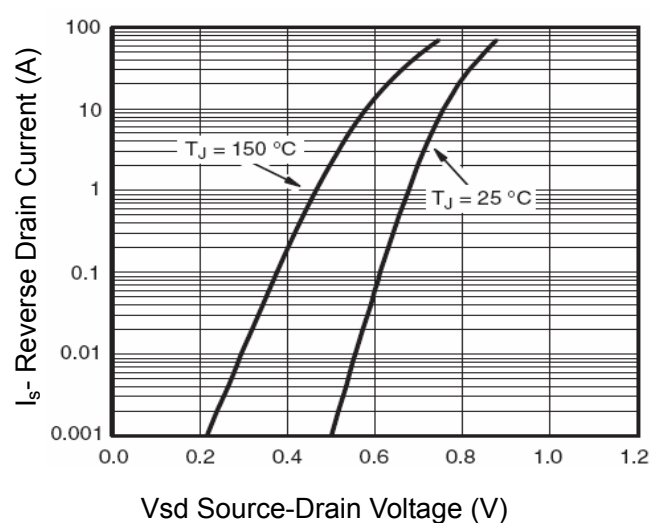
## Electrical Characteristics (TC=25°C unless otherwise noted)

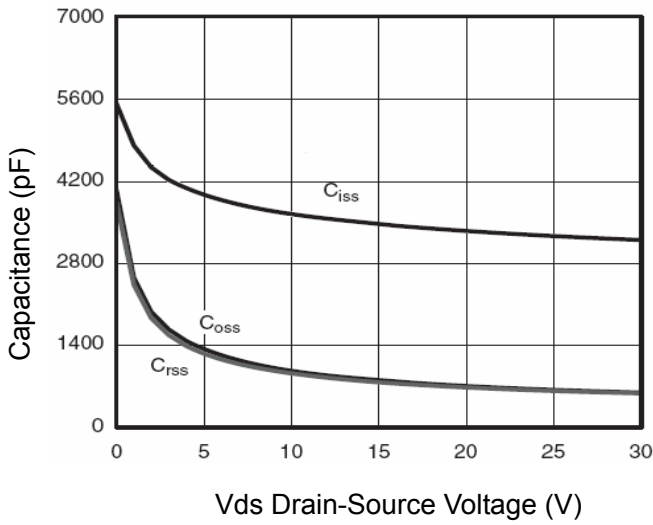
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-30V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-10A$	-	4.6	9	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-10V, I_D=-15A$	-	20	-	S
<b>Dynamic Characteristics (Note 4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	6425	-	PF
Output Capacitance	$C_{oss}$		-	885	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	675	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-10A$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	13	-	nS
Turn-on Rise Time	$t_r$		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	$t_f$		-	14	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-15V, I_D=-10A,$ $V_{GS}=-10V$	-	84	-	nC
Gate-Source Charge	$Q_{gs}$		-	11.7	-	nC
Gate-Drain Charge	$Q_{gd}$		-	25	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=-10A$	-	-0.85	-1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	-50	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ C, I_F = -10A$ $di/dt = 100A/\mu s$ (Note3)	-	-	45	nS
Reverse Recovery Charge	$Q_{rr}$		-	-	43	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

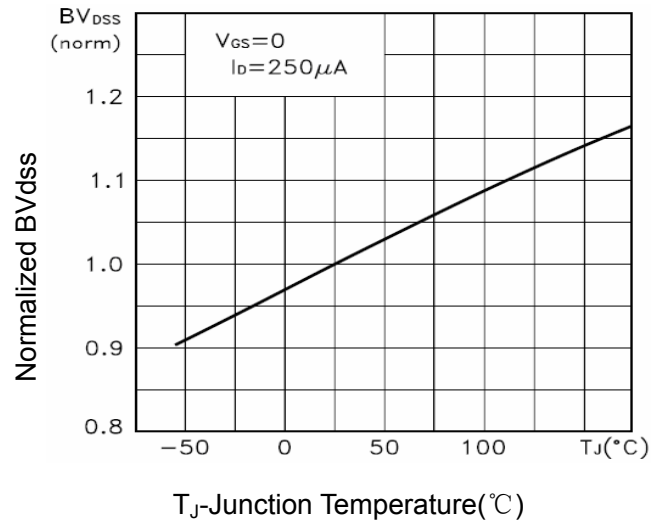
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ C, V_{DB}=-15V, V_G=-10V, L=0.5mH, R_g=25\Omega$

**Test Circuit**
**1) E<sub>AS</sub> Test Circuits**

**2) Gate Charge Test Circuit**

**3) Switch Time Test Circuit**


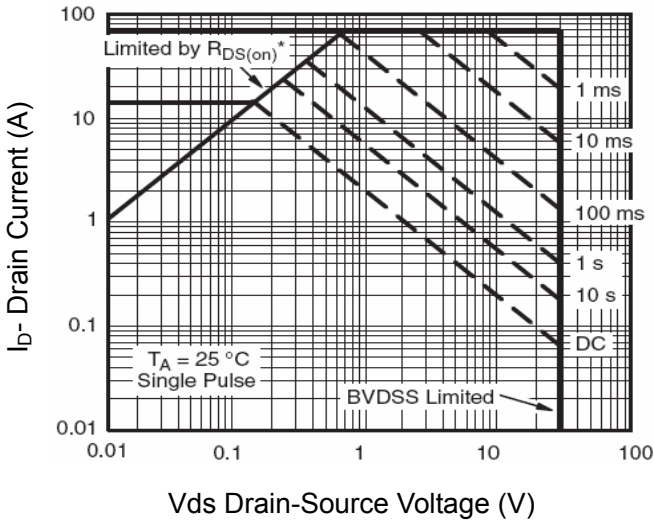
**Typical Electrical and Thermal Characteristics (Curves)**

**Figure 1 Output Characteristics**

**Figure 4 Rdson-Junction Temperature**

**Figure 2 Transfer Characteristics**

**Figure 5 Gate Charge**

**Figure 3 Rdson- Drain Current**

**Figure 6 Source- Drain Diode Forward**



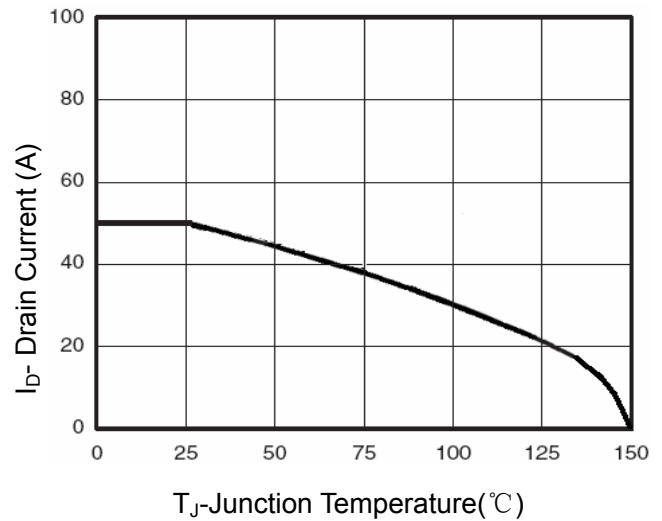
**Figure 7 Capacitance vs Vds**



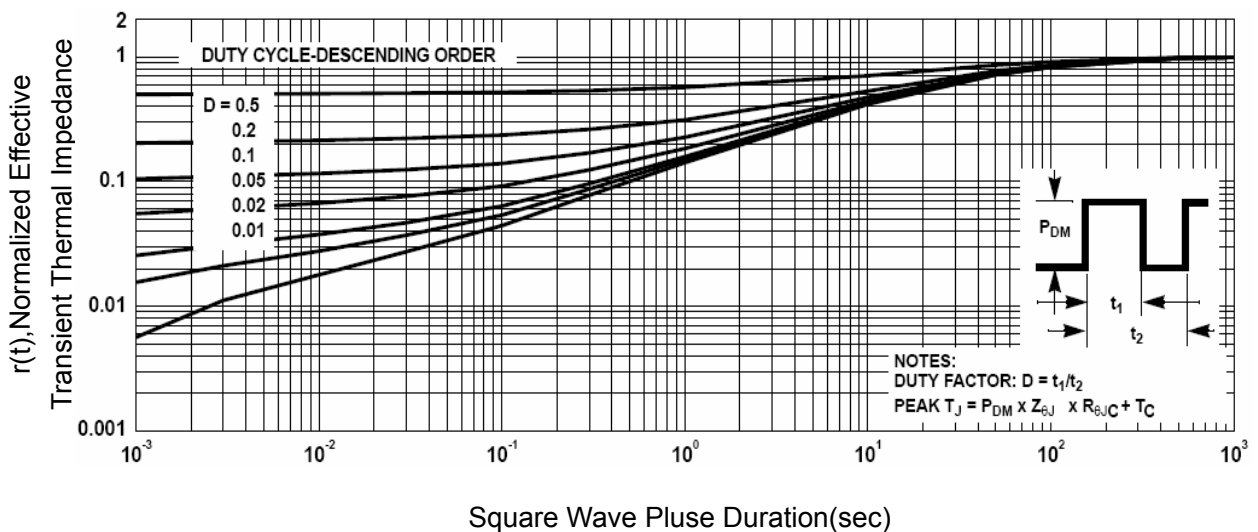
**Figure 9 BV<sub>DSS</sub> vs Junction Temperature**



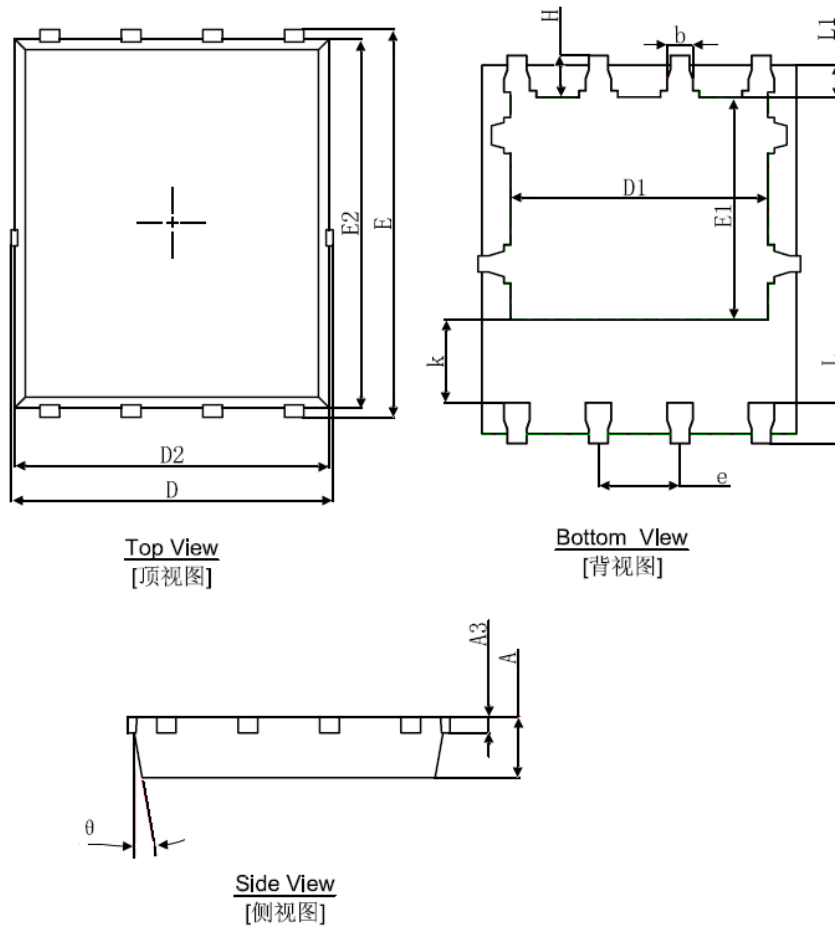
**Figure 8 Safe Operation Area**



**Figure 10 ID Current Derating vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

**DFN5X6-8L Package Information**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
K	1.190	1.390	0.047	0.055
b	0.035	0.450	0.014	0.018
e	1.270(TYP.)		0.050(TYP.)	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	8°	12°	8°	12°

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