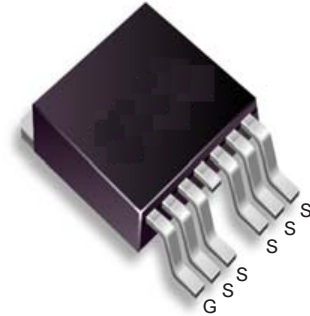


## Applications

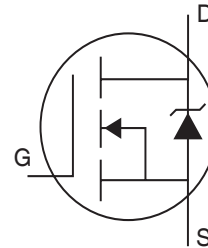
- DC Motor Drive
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

## General Features

- $V_{DS} = 40V, I_D = 330A$   
 $R_{DS(ON)} < 1.6m\Omega @ V_{GS} = 10V$



D<sup>2</sup>Pak 7 Pin



## Benefits

- Optimized for Logic Level Drive
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability
- Lead-Free

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	330	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	240	
$I_{DM}$	Pulsed Drain Current	1320	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	355	W
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$dv/dt$	Peak Diode Recovery	1.3	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

## Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy	912	mJ
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## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.42	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	40	

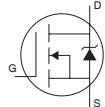
### Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

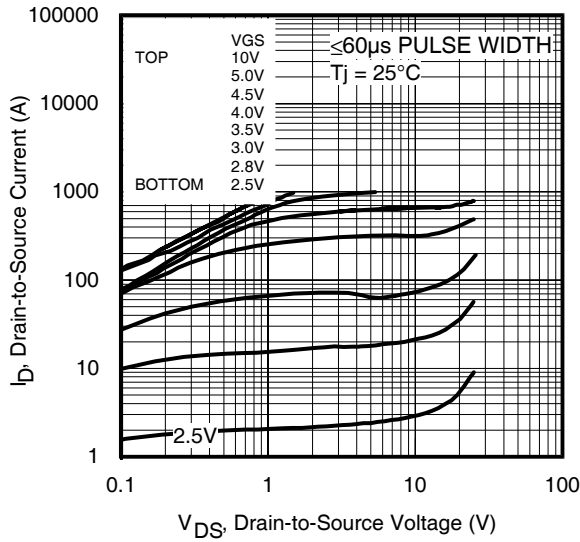
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.2	1.6	m $\Omega$	$V_{GS} = 10V, I_D = 30A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.9	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_G$	Internal Gate Resistance	—	1	—	$\Omega$	

### Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

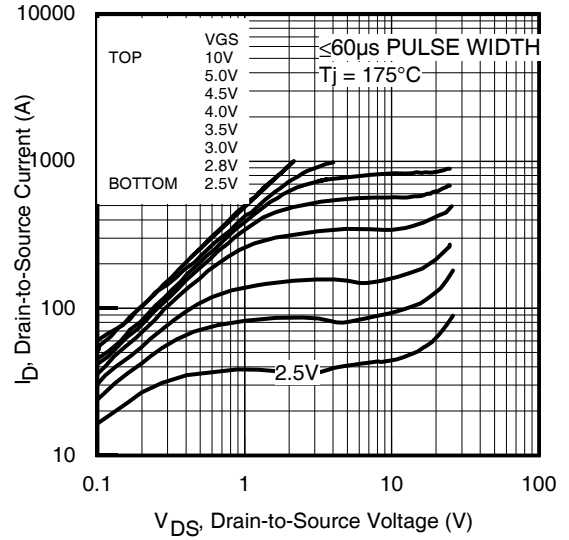
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	—	80	—	S	$V_{DS} = 10V, I_D = 15A$
$Q_g$	Total Gate Charge	—	120	180	nC	$I_D = 20A$ $V_{DS} = 20V$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source Charge	—	25	50		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	75	90		
$t_{d(on)}$	Turn-On Delay Time	—	40	—	ns	$V_{DD} = 15V$ $I_D = 10A$ $R_G = 2.5\Omega$ $V_{GS} = 10V$
$t_r$	Rise Time	—	20	—		
$t_{d(off)}$	Turn-Off Delay Time	—	116	—		
$t_f$	Fall Time	—	68	—		
$C_{iss}$	Input Capacitance	—	11480	—	pF	$V_{GS} = 0V$ $V_{DS} = 20V$ $f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1380	—		
$C_{rss}$	Reverse Transfer Capacitance	—	1050	—		

### Diode Characteristics

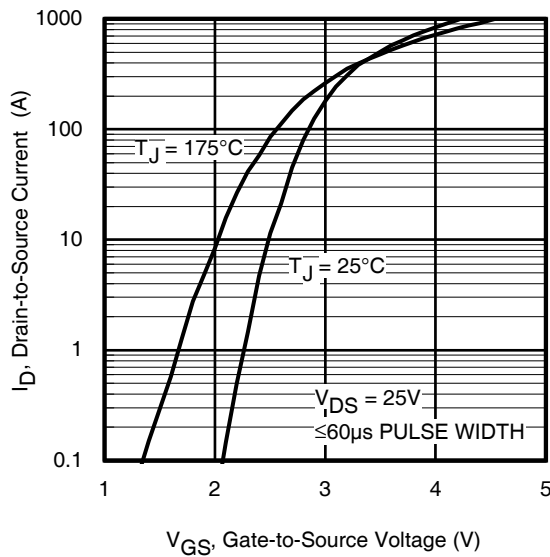
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	330	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	1320	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 30A, V_{GS} = 0V$
$t_{rr}$	Reverse Recovery Time	—	62	—	ns	$T_J = 25^\circ\text{C}, I_F = 20A, V_R = 30V,$ $di/dt = 100A/\mu s$
$Q_{rr}$	Reverse Recovery Charge	—	52	—	nC	
$I_{RRM}$	Reverse Recovery Current	—	3.7	—	A	



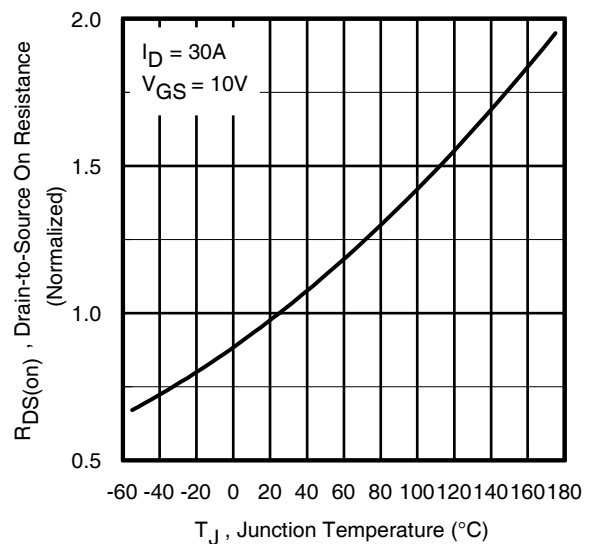
**Fig 1.** Typical Output Characteristics



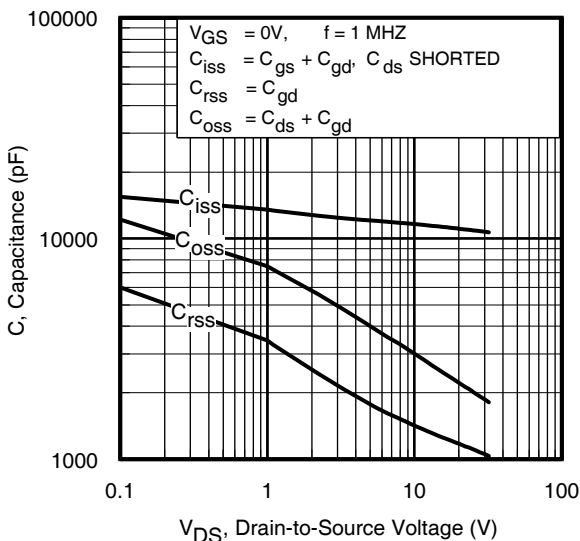
**Fig 2.** Typical Output Characteristics



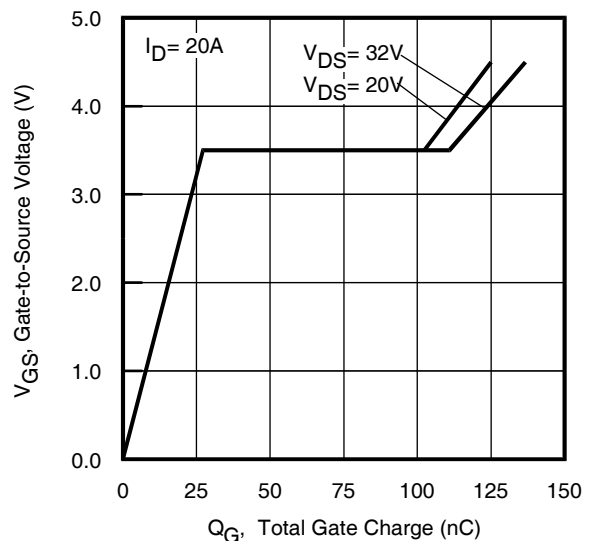
**Fig 3.** Typical Transfer Characteristics



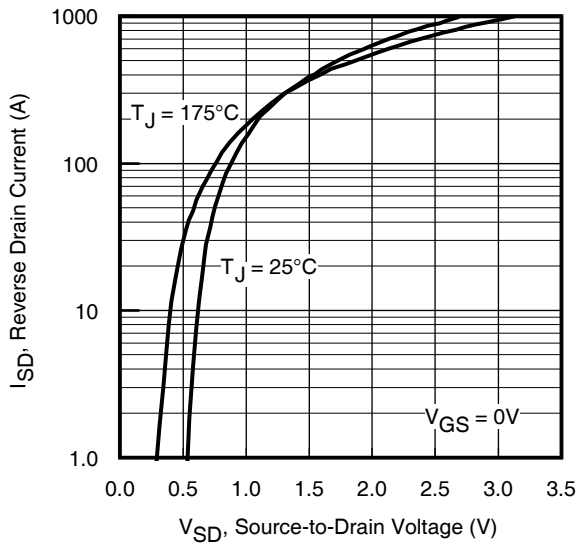
**Fig 4.** Normalized On-Resistance vs. Temperature



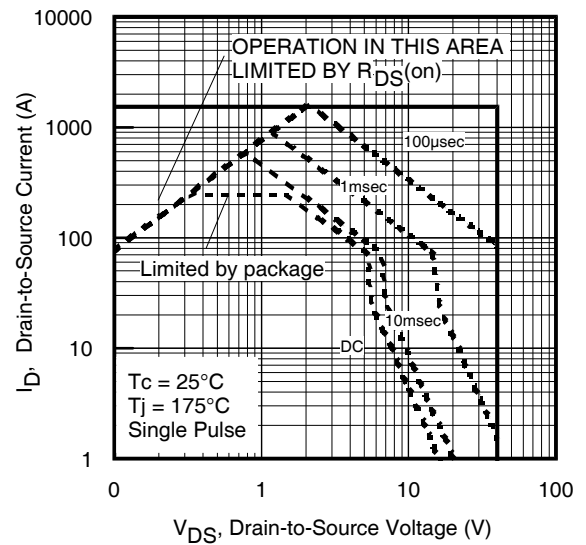
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



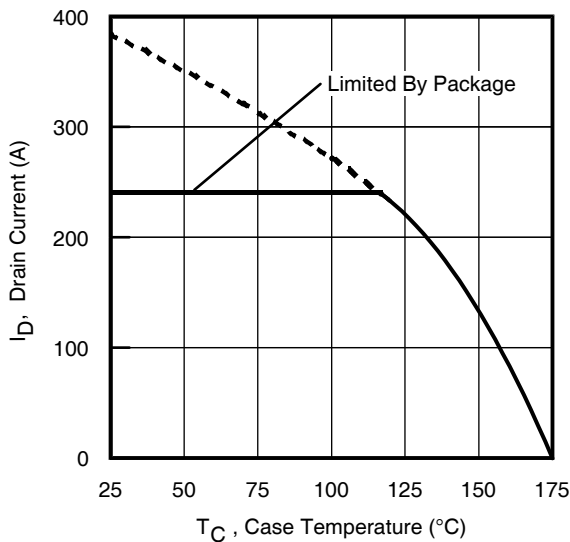
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



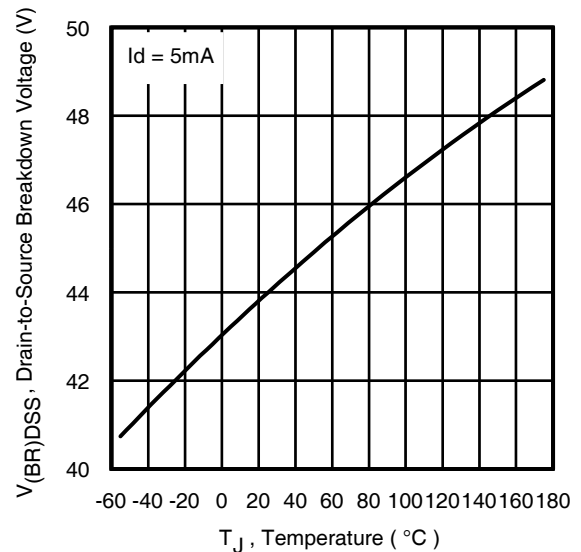
**Fig 7.** Typical Source-Drain Diode Forward Voltage



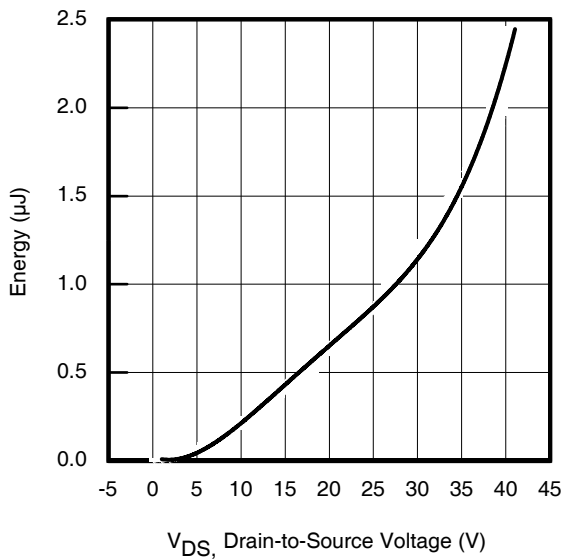
**Fig 8.** Maximum Safe Operating Area



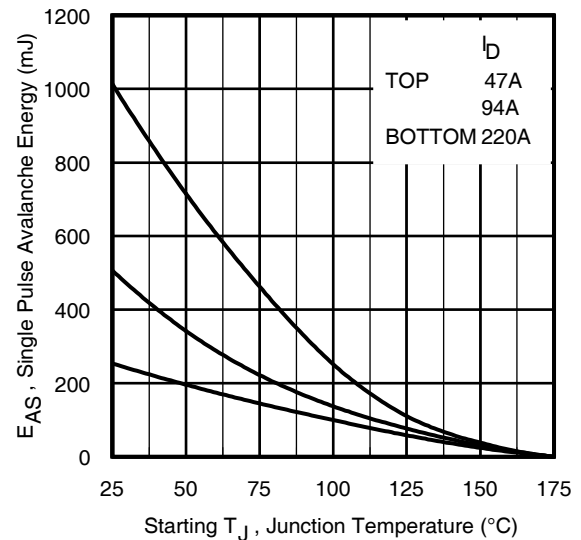
**Fig 9.** Maximum Drain Current vs. Case Temperature



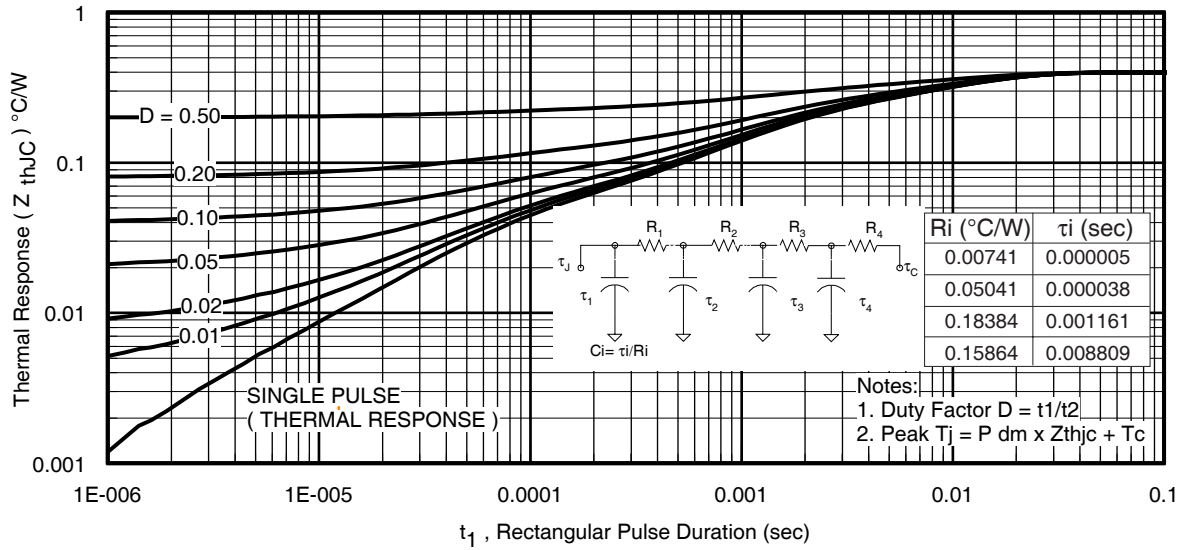
**Fig 10.** Drain-to-Source Breakdown Voltage



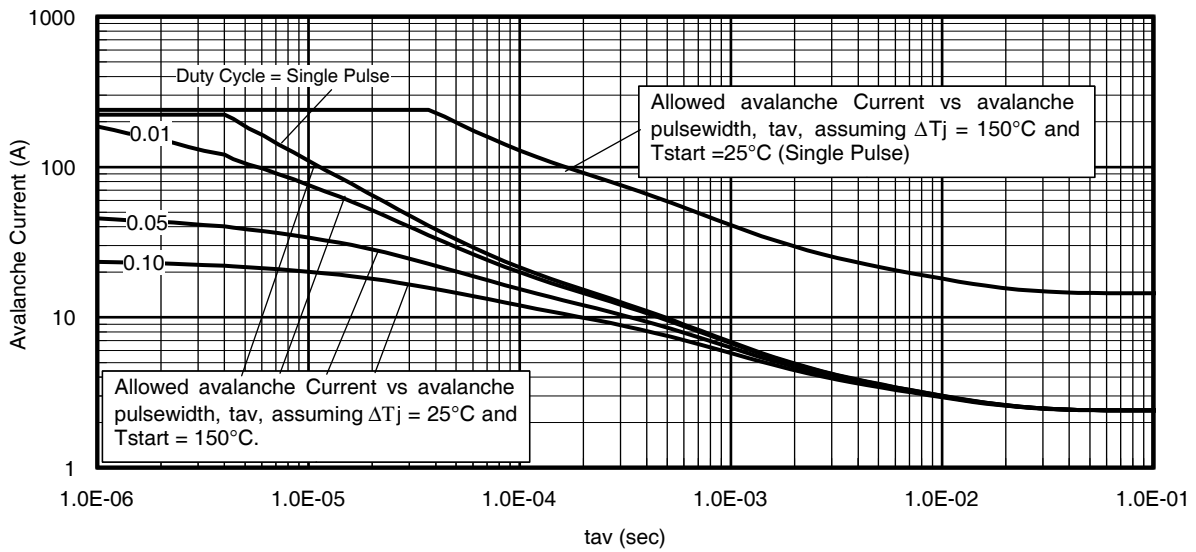
**Fig 11.** Typical  $C_{OSS}$  Stored Energy



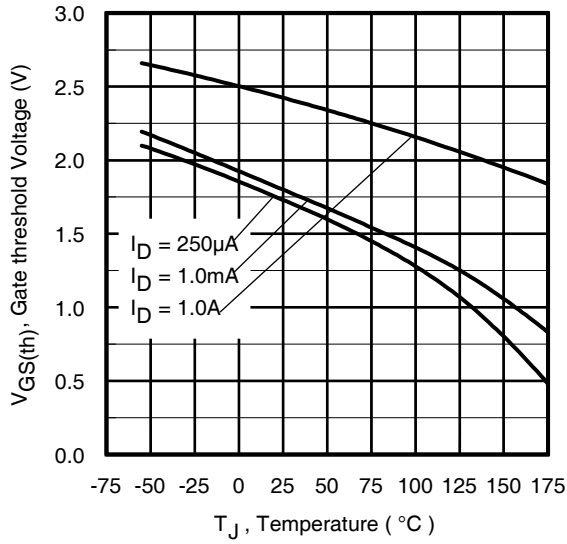
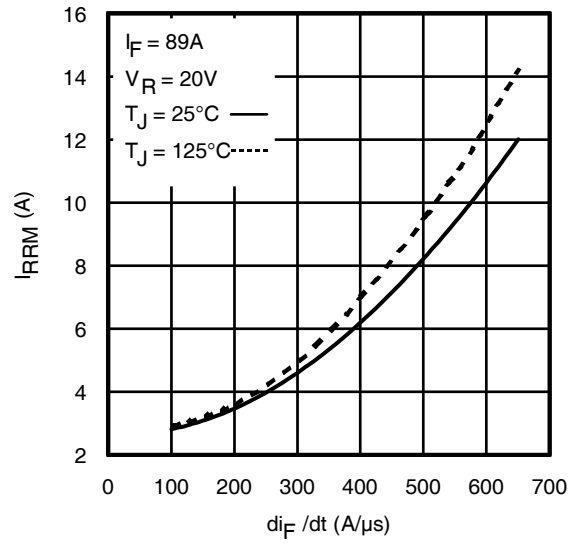
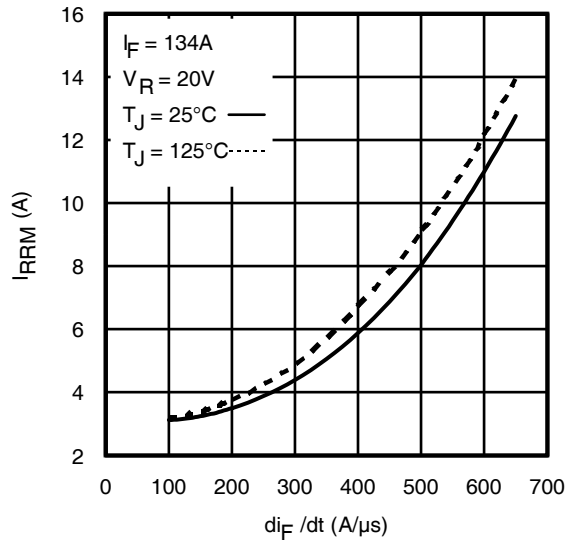
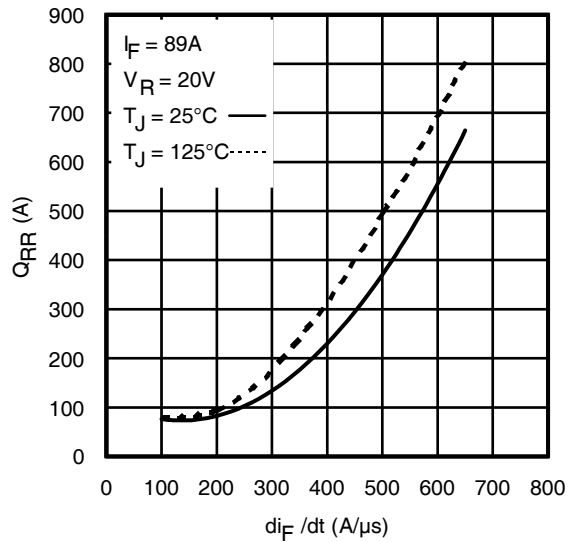
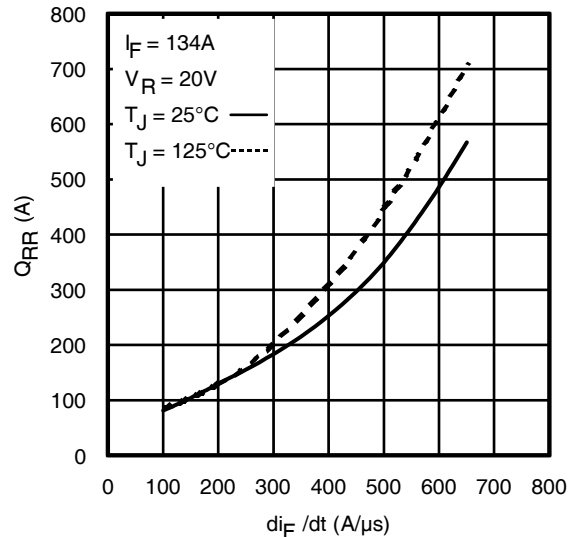
**Fig 12.** Maximum Avalanche Energy Vs. Drain Current

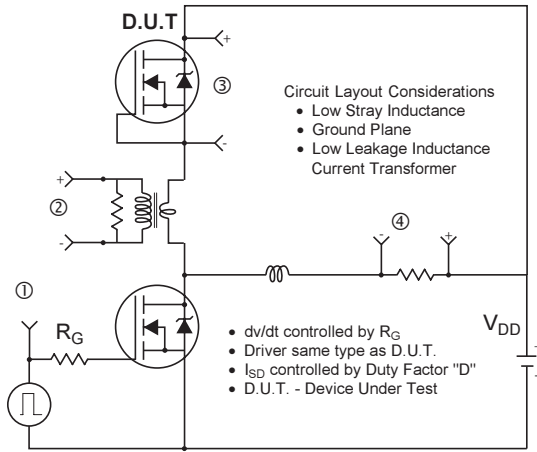


**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Fig 14.** Typical Avalanche Current vs.Pulsewidth


**Fig. 16.** Threshold Voltage vs. Temperature

**Fig. 17 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 18 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 19 -** Typical Stored Charge vs.  $di_F/dt$ 

**Fig. 20 -** Typical Stored Charge vs.  $di_F/dt$

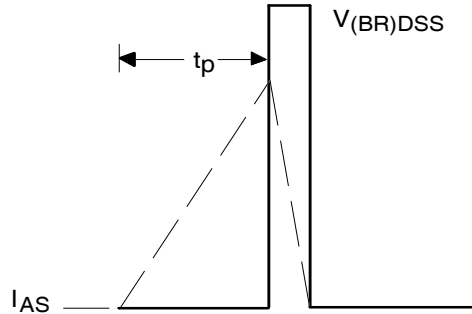


\*  $V_{GS} = 5V$  for Logic Level Devices

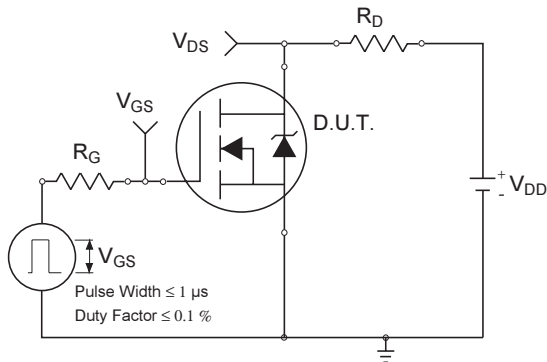
**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel**



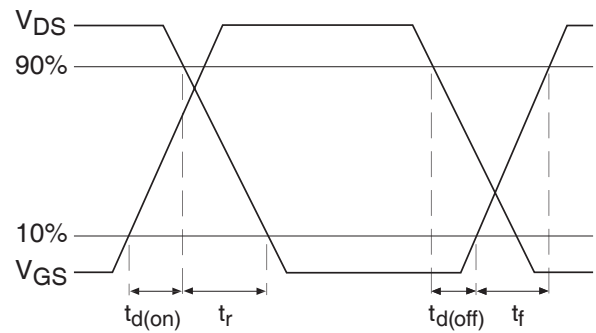
**Fig 22a. Unclamped Inductive Test Circuit**



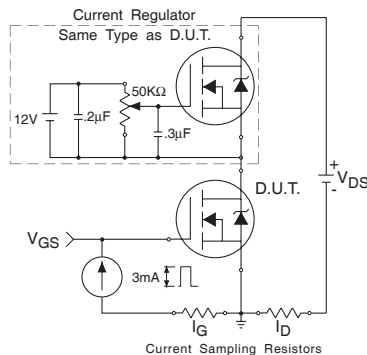
**Fig 22b. Unclamped Inductive Waveforms**



**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



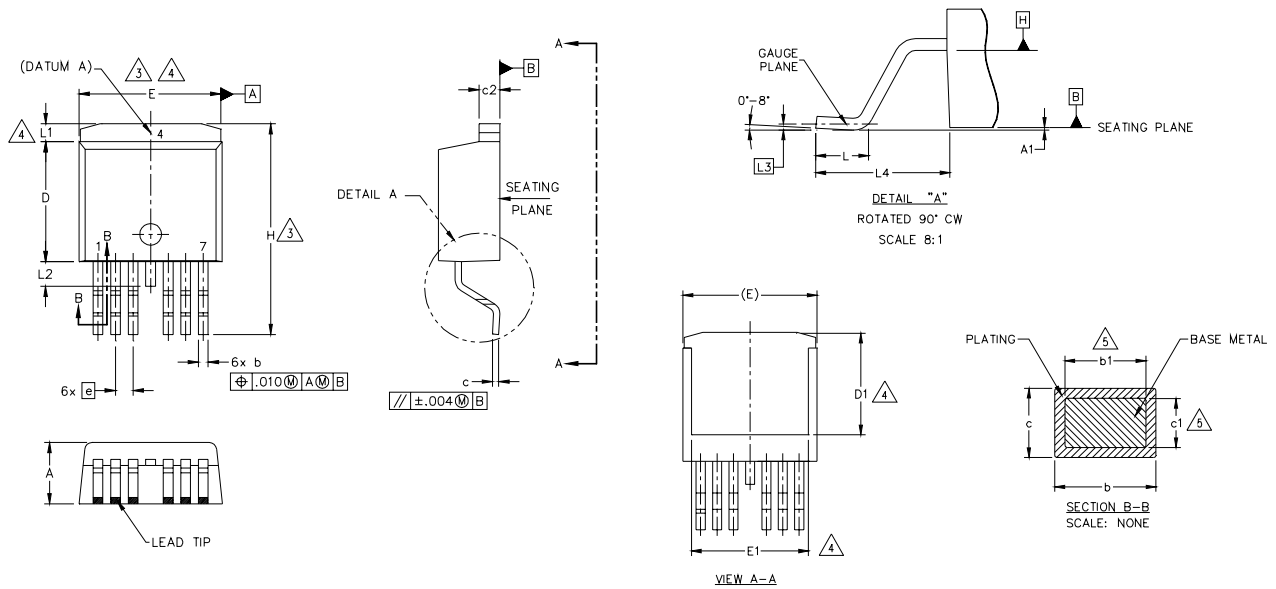
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

## TO-263-6L Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	
E	9.65	10.67	.380	.420	
E1	6.22	—	.245	—	
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.



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