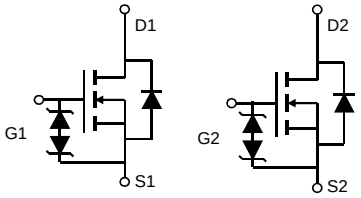
20V Dual N-Channel MOSFET

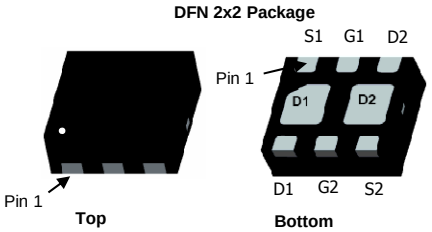
General Description

The FNK2220 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.



Product Summary

V_{DS}	20V
I_D (at V_{GS}=4.5V)	3.3A
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 45mΩ
$R_{DS(ON)}$ (at V_{GS}=2.5V)	< 60mΩ



Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	3.3	A
	T_A=70℃		2.6	
Pulsed Drain Current [C]		I_{DM}	16	
Power Dissipation [B]	T_A=25℃	P_D	1.5	W
	T_A=70℃		0.95	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	35	45	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		65	85	℃/W
Maximum Junction-to-Ambient [B]	t ≤ 10s	$R_{\theta JA}$	120	155	℃/W
Maximum Junction-to-Ambient [B]	Steady-State		175	235	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±8V			20	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	0.4	0.8	1.2	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	24			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=4A		29	45	mΩ
		T_J=125℃		50	65	
		V_{GS}=2.5V, I_D=3A		35	60	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=4A		14		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				1.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz	285	360	435	pF
C_{oss}	Output Capacitance		45	65	85	pF
C_{rss}	Reverse Transfer Capacitance		30	50	70	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.7	3.5	5.3	Ω
SWITCHING PARAMETERS						
Q_g(4.5V)	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=4A		4.15	6	nC
Q_{gs}	Gate Source Charge			0.55		nC
Q_{gd}	Gate Drain Charge			1.15		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=4.5V, V_{DS}=10V, R_L=2.5Ω, R_{GEN}=3Ω		9.5		ns
t_r	Turn-On Rise Time			43		ns
$t_{D(off)}$	Turn-Off DelayTime			26		ns
t_f	Turn-Off Fall Time			39		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=4A, dI/dt=100A/μs		11		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=4A, dI/dt=100A/μs		3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it to.

B. The value of $R_{\theta JA}$ is measured with the device mounted on a minimum pad board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it to.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

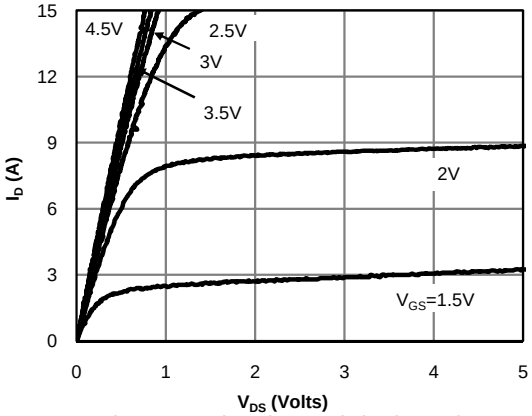


Fig 1: On-Region Characteristics (Note D)

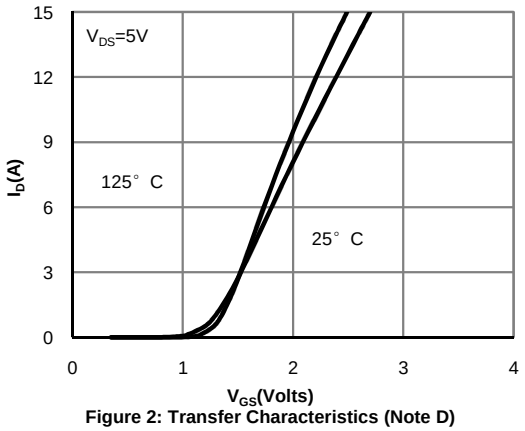


Figure 2: Transfer Characteristics (Note D)

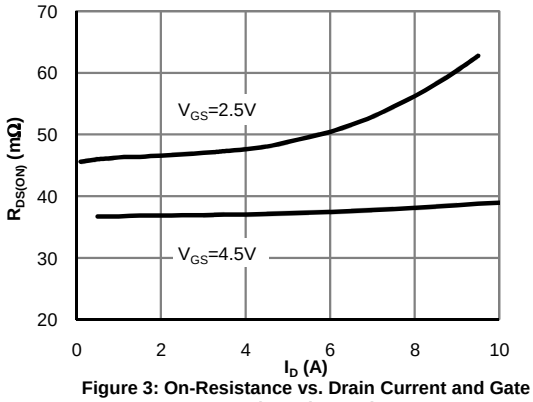


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note D)

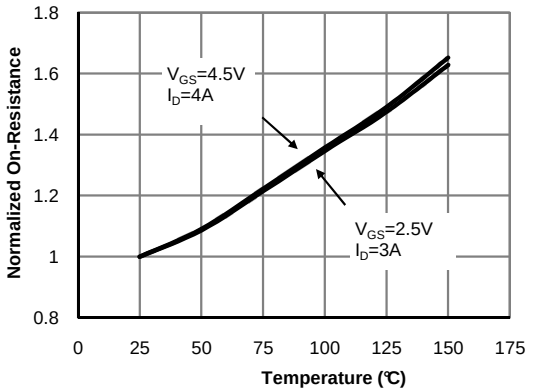


Figure 4: On-Resistance vs. Junction Temperature (Note D)

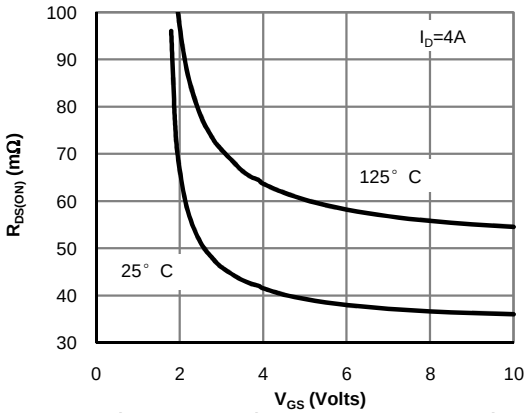


Figure 5: On-Resistance vs. Gate-Source Voltage (Note D)

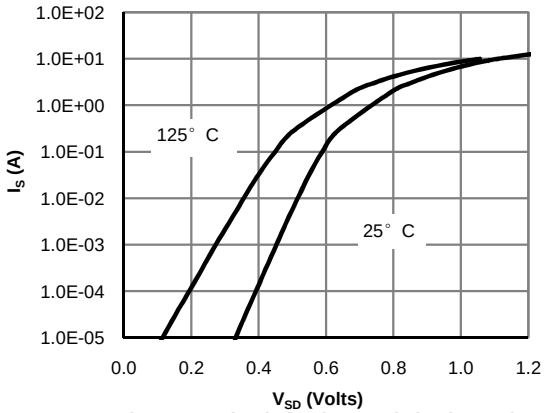


Figure 6: Body-Diode Characteristics (Note D)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

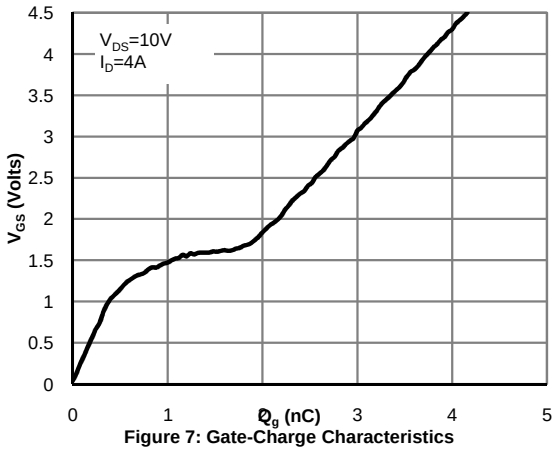


Figure 7: Gate-Charge Characteristics

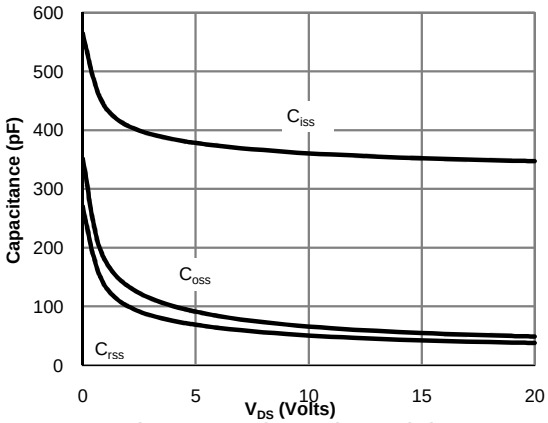


Figure 8: Capacitance Characteristics

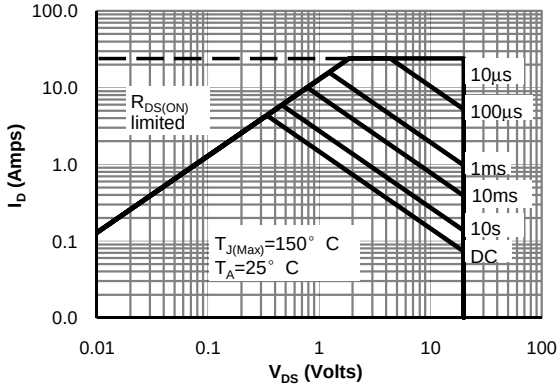


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

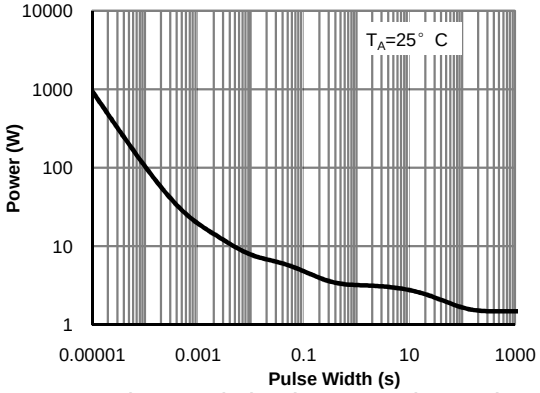


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

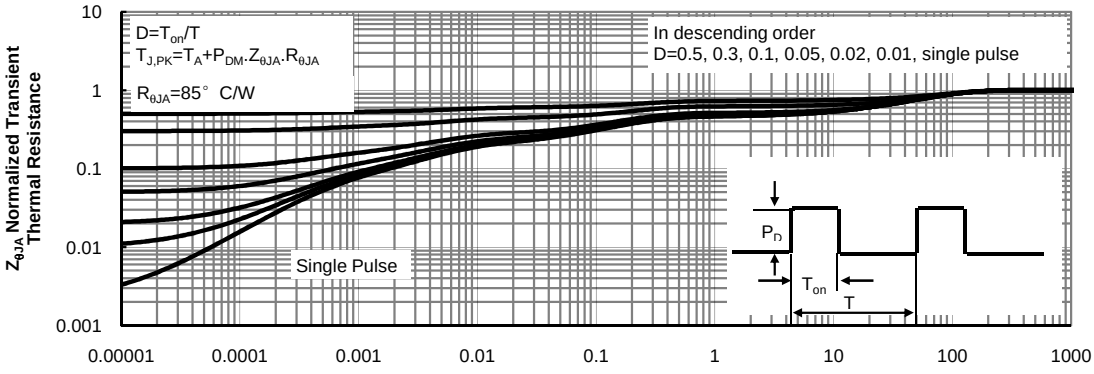
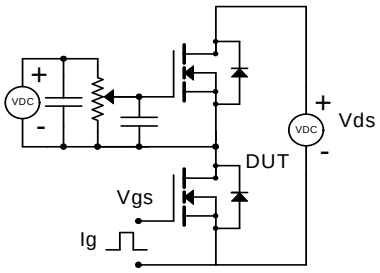
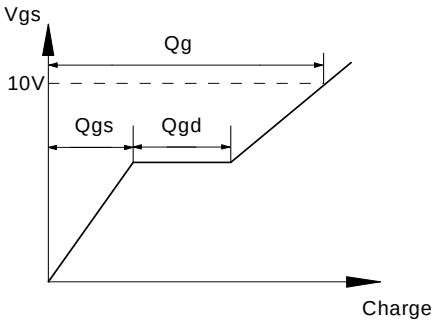


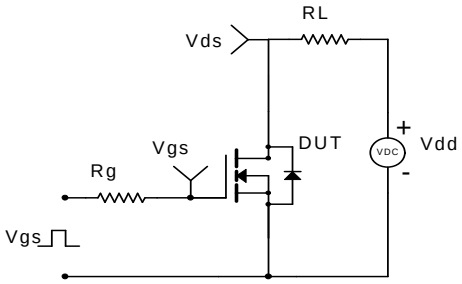
Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

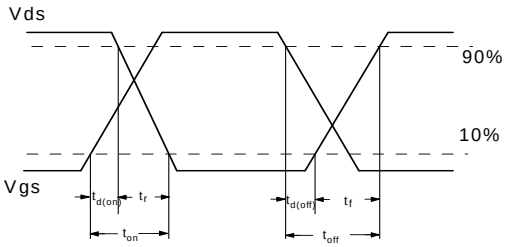
Gate Charge Test Circuit & Waveform



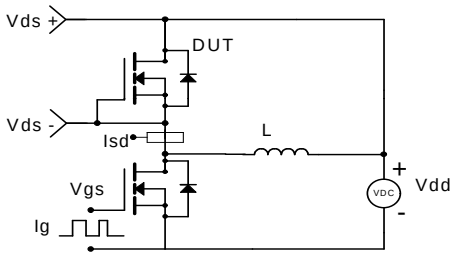


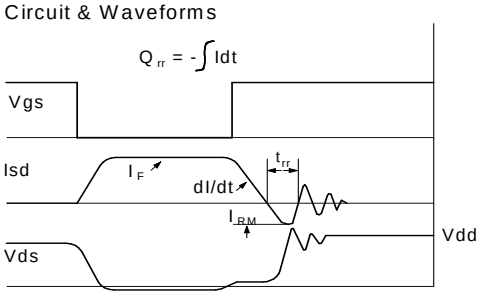
Resistive Switching Test Circuit & Waveforms



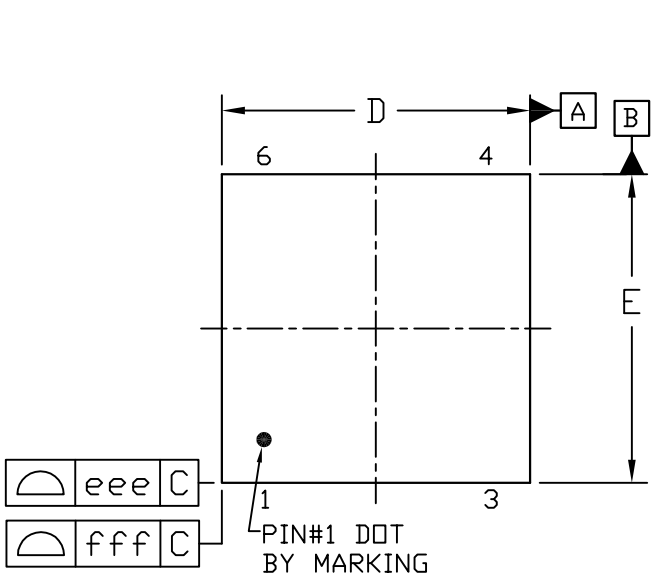


Diode Recovery Test Circuit & Waveforms

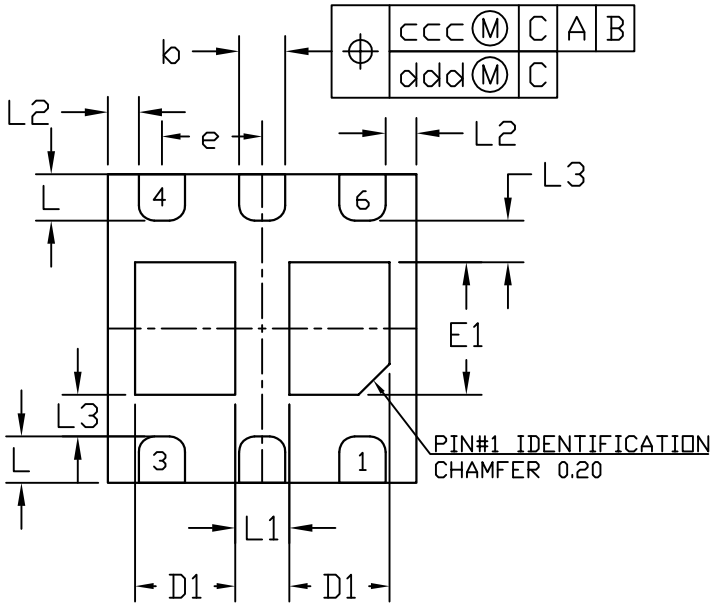




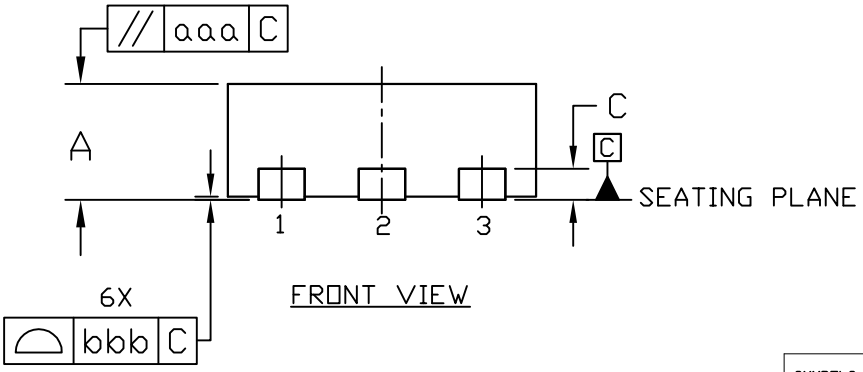
DFN2x2_6L_EP2_S PACKAGE OUTLINE



TOP VIEW

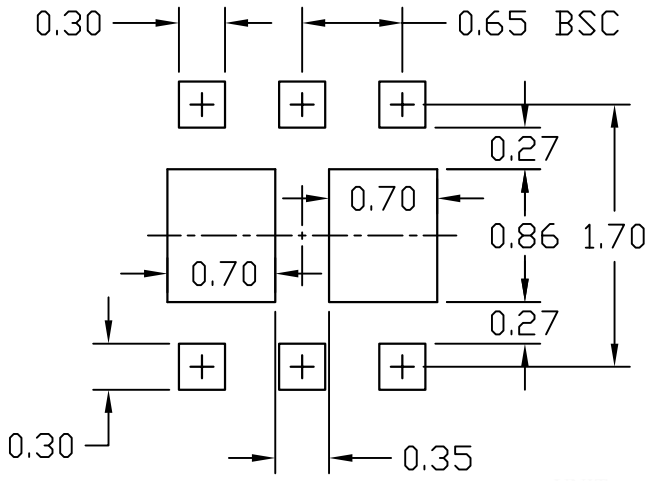


BOTTOM VIEW



FRONT VIEW

RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
b	0.25	0.30	0.35	0.010	0.012	0.014
c		0.20 Ref.			0.008 Ref.	
D	1.90	2.00	2.10	0.075	0.079	0.083
D1	0.620	0.650	0.680	0.024	0.026	0.027
E	1.90	2.00	2.10	0.075	0.079	0.083
E1	0.76	0.86	0.96	0.030	0.034	0.038
e		0.65 BSC			0.026 BSC	
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.320	0.350	0.380	0.013	0.014	0.015
L2	0.170	0.200	0.230	0.007	0.008	0.009
L3	0.240	0.270	0.300	0.009	0.011	0.012
aaa	---	0.100	---	---	0.004	---
bbb	---	0.080	---	---	0.003	---
ccc	---	0.100	---	---	0.004	---
ddd	---	0.050	---	---	0.002	---
eee	---	0.150	---	---	0.006	---
fff	---	0.150	---	---	0.006	---

Disclaimer:

- **FNK reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **All semiconductor products malfunction or fail with some probability under special conditions. When using FNK products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.**
- **FNK will supply the best possible product for customers!**