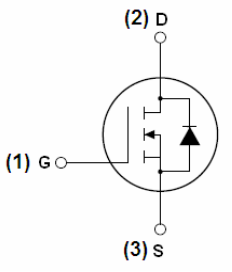
FNK N-Channel Enhancement Mode Power MOSFET

Description

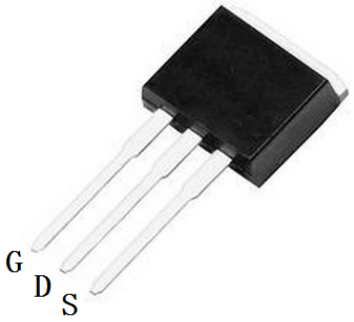
The FNK30H80A uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.



Schematic diagram

General Features

- V_{DS} =30V,I_D =80A
  $R_{DS(ON)}$ <6.6mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ < 8.2mΩ @ V_{GS}=5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



Marking and pin assignment

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FNK30H80A	FNK30H80A	TO-262	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	50	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	83	W
Derating factor		0.56	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	108	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	1.8	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

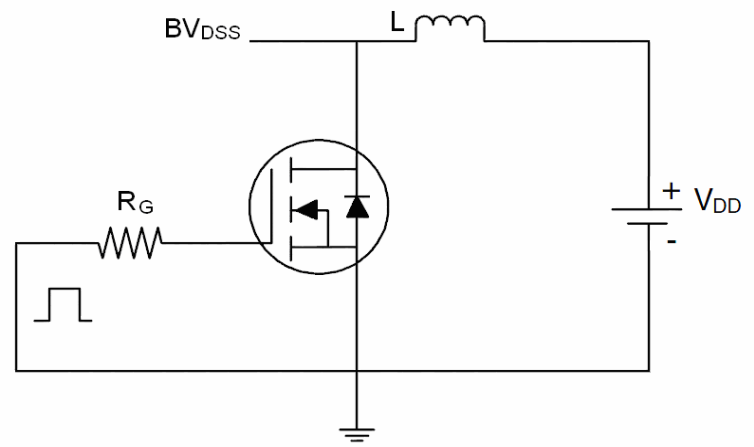
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	1.1	1.4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	5.4	6.6	mΩ
		V_{GS}=4.5V, I_D=20A	-	6.6	8.2	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=24A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	2060	-	PF
Output Capacitance	C_{oss}		-	345	-	PF
Reverse Transfer Capacitance	C_{rss}		-	320	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V,I_D=30A V_{GS}=10V,R_{GEN}=2.7Ω	-	20	-	nS
Turn-on Rise Time	t_r		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	60	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=30A, V_{GS}=10V	-	51	-	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain Charge	Q_{gd}		-	11	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=24A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	80	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 30A di/dt = 100A/μs (Note3)	-	32	50	nS
Reverse Recovery Charge	Qrr		-	12	20	nC

Notes:

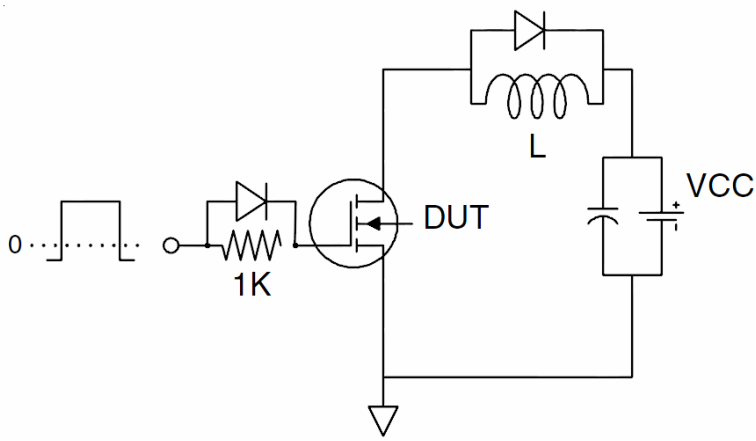
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω，I_{AS}=35A

Test Circuit

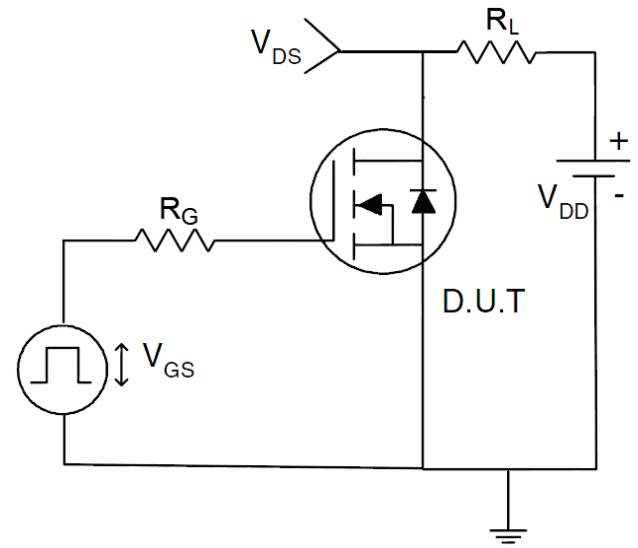
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

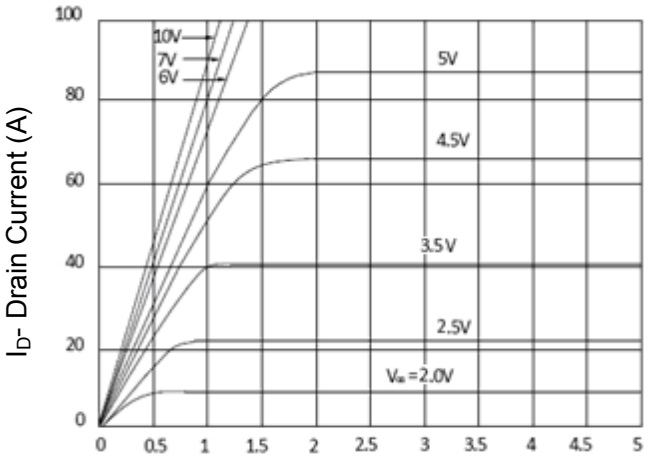


Figure 1 Output Characteristics

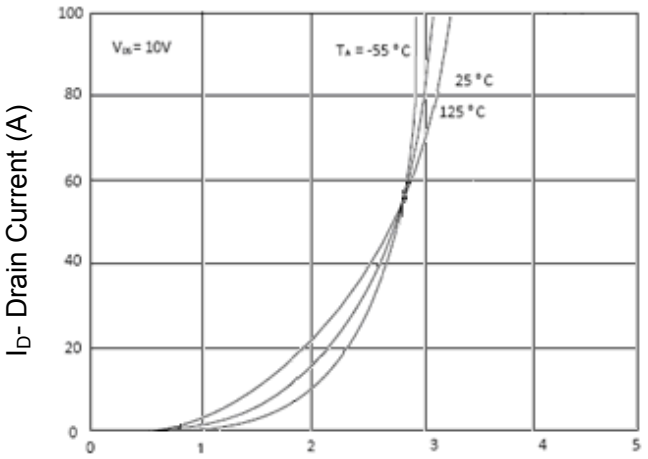


Figure 2 Transfer Characteristics

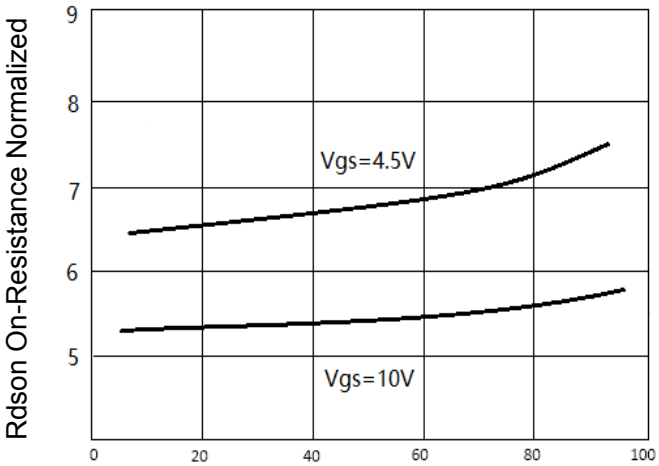


Figure 3 Rdson- Drain Current

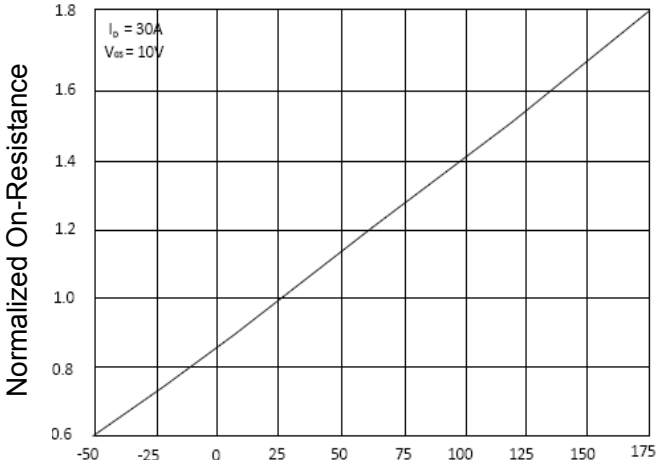


Figure 4 Rdson-Junction Temperature

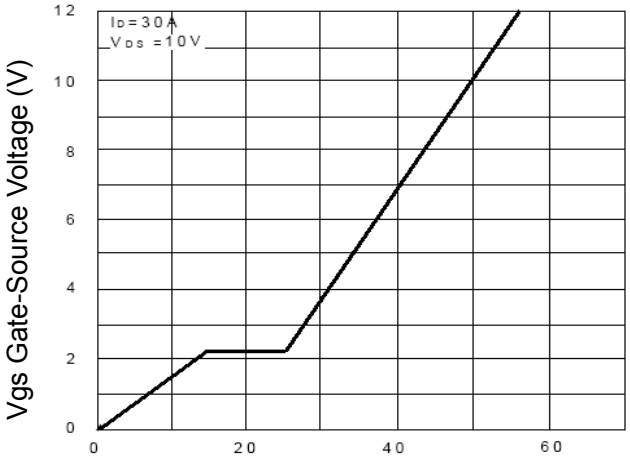


Figure 5 Gate Charge

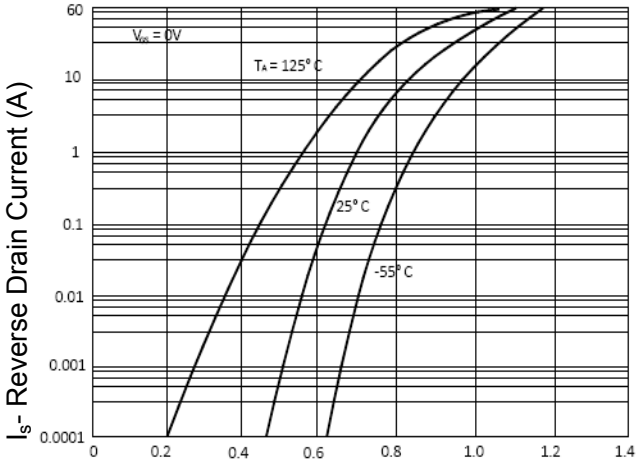


Figure 6 Source- Drain Diode Forward

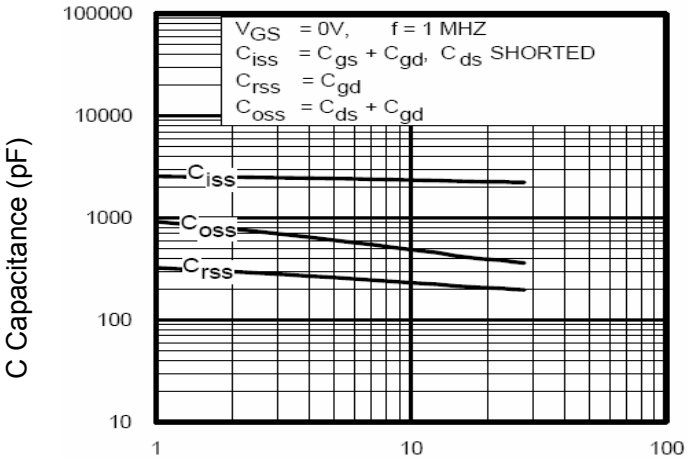


Figure 7 Capacitance vs Vds

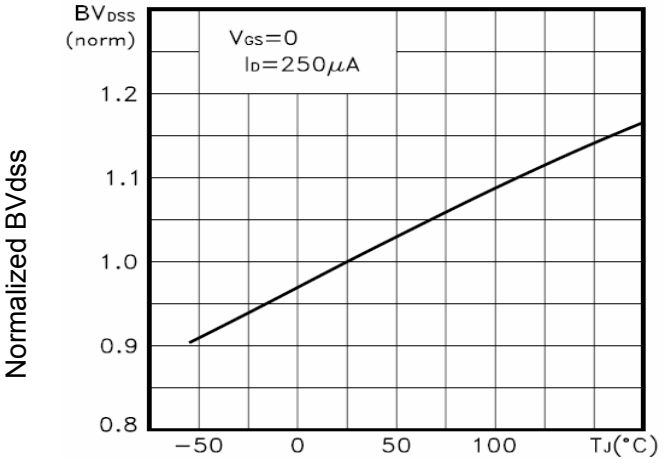


Figure 9 BV_{DSS} vs Junction Temperature

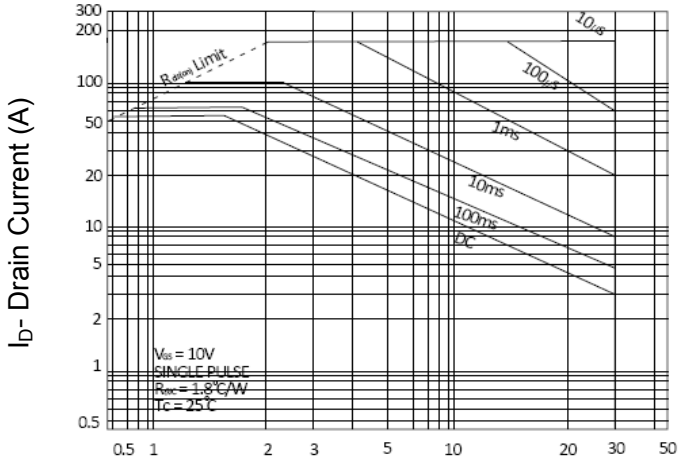


Figure 8 Safe Operation Area

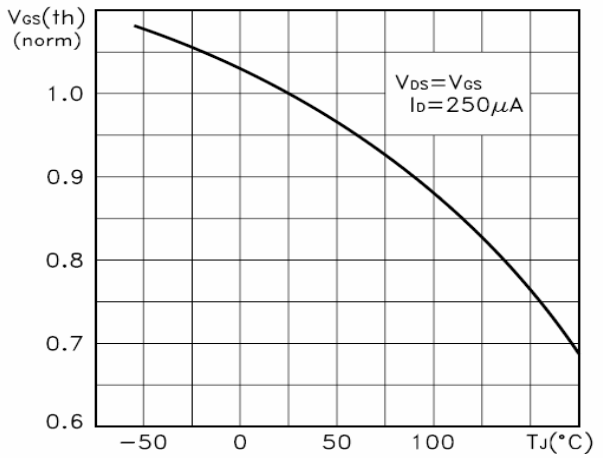


Figure 10 $V_{GS(th)}$ vs Junction Temperature

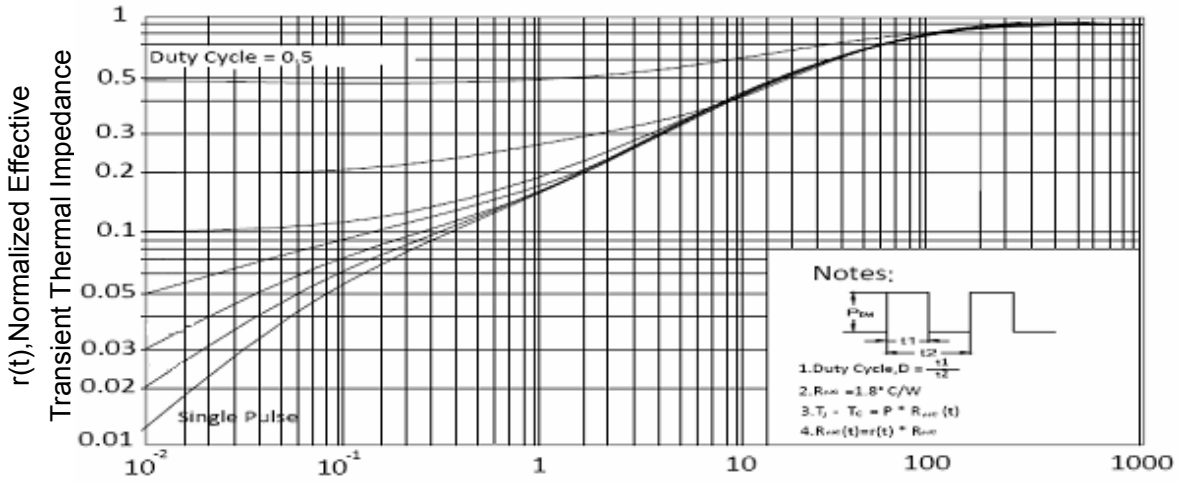
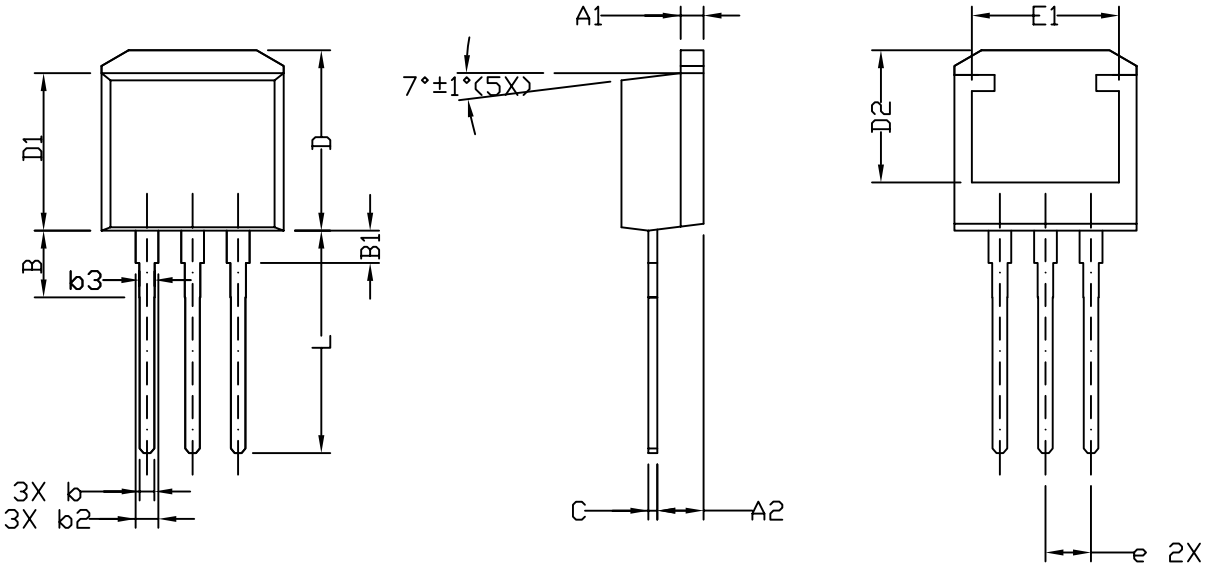
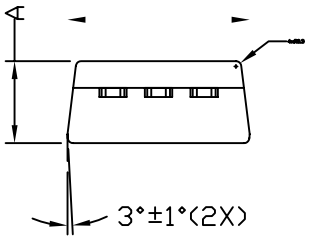


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-262 Package Information





SYMBOL	DIMENSIONAL REQMTS			INCHES REQMTS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.57	4.72	0.169	0.180	0.186
A1	1.17	1.27	1.37	0.046	0.050	0.054
A2	2.47	2.57	2.67	0.097	0.101	0.105
B	3.55	3.72	3.90	0.140	0.146	0.154
B1	1.65	1.80	2.00	0.065	0.071	0.079
b	0.69	0.813	0.94	0.027	0.032	0.037
b2	1.17	1.27	1.45	0.046	0.050	0.057
b3	0.74	0.86	0.91	0.029	0.034	0.036
c	0.48	0.50	0.60	0.019	0.020	0.024
				0.382		
				5		
L	12.27	12.40	13.48	0.483	0.488	0.531

Disclaimer:

- **FNK reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **All semiconductor products malfunction or fail with some probability under special conditions. When using FNK products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.**
- **FNK will supply the best possible product for customers!**