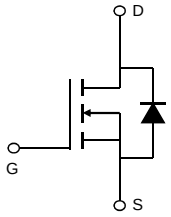
60V N-Channel MOSFET

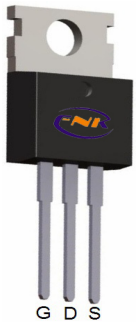
Description

The FNK3205A uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.



General Feature

- V_{DS} =60V,I_D =110A
  $R_{DS(ON)}$ < 6.0mΩ @ V_{GS}=10V (Typ:4.9mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



To-220 Top View

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**		**Units**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25℃	I_D	110	A
	T_C=100℃		80	
Pulsed Drain Current [C]		I_{DM}	390	
Continuous Drain Current	T_A=25℃	I_{DSM}	13	A
	T_A=70℃		10	
Avalanche Current [C]		I_{AS}	62	A
Avalanche energy L=0.1mH [C]		E_{AS}	20	mJ
Power Dissipation [B]	T_C=25℃	P_D	200	W
	T_C=100℃		79	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.1	W
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics					
Parameter		**Symbol**			**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	15	15	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		60	60	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.3	4.1	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.5	3	3.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	260			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		4.9	6.0	mΩ
		T_J=125℃		6.2	7.8	
		V_{GS}=4.5V, I_D=20A		10.2	13.6	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		44		S
V	Diode Forward Voltage	I_S=1A,V_{GS}=0V			1.3	V
I_S	Maximum Body-Diode Continuous Current [G]				110	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		4050		pF
C_{oss}	Output Capacitance			345		pF
C_{rss}	Reverse Transfer Capacitance			16.8		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.3	0.65	1.0	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=20A		53	75	nC
Q_g(4.5V)	Total Gate Charge			22	31	nC
Q_{gs}	Gate Source Charge			17		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=1.5Ω, R_{GEN}=3Ω		18		ns
t_r	Turn-On Rise Time			20		ns
$t_{D(off)}$	Turn-Off DelayTime			33		ns
t_f	Turn-Off Fall Time			4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/μs		26		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/μs		125		nC

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

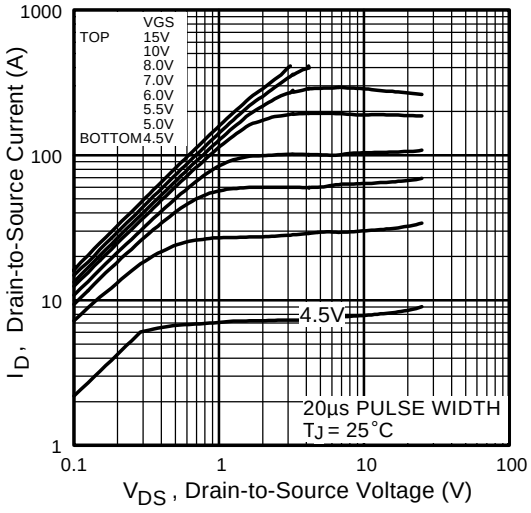


Fig 1. Typical Output Characteristics

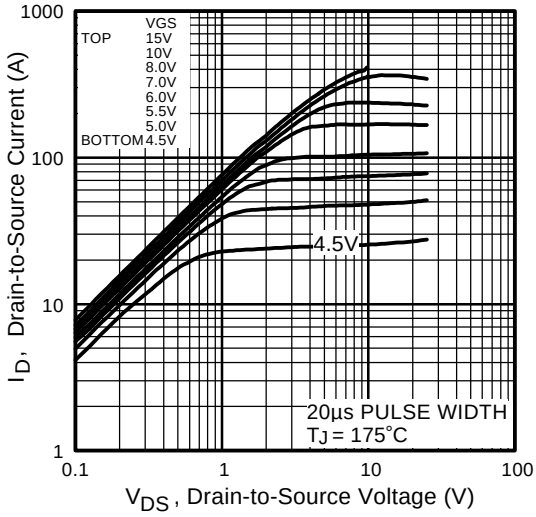


Fig 2. Typical Output Characteristics

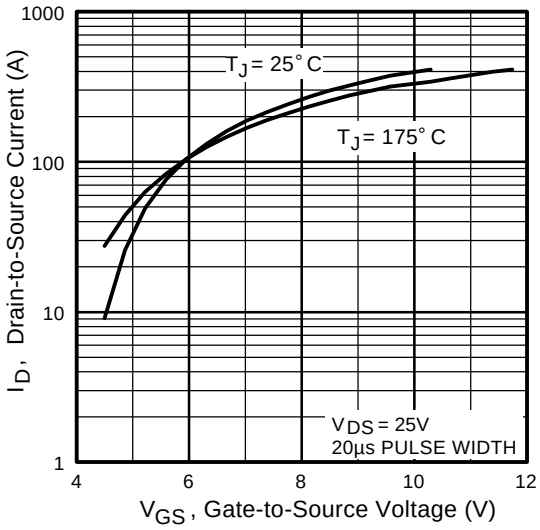


Fig 3. Typical Transfer Characteristics

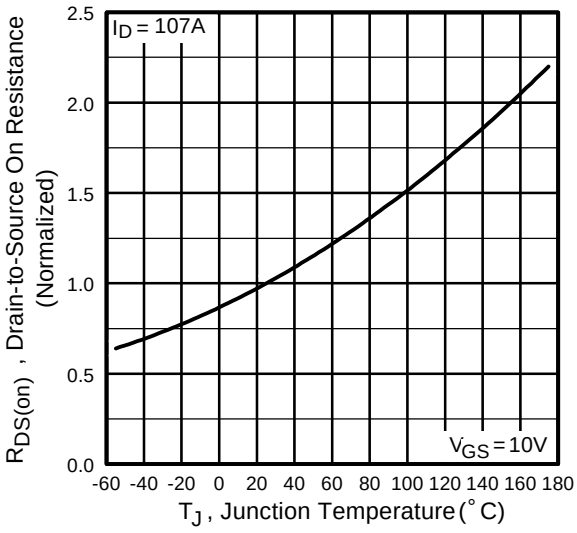


Fig 4. Normalized On-Resistance Vs. Temperature

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

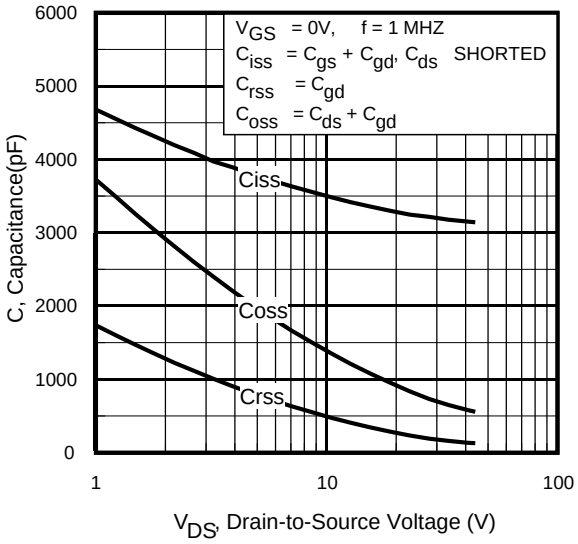


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

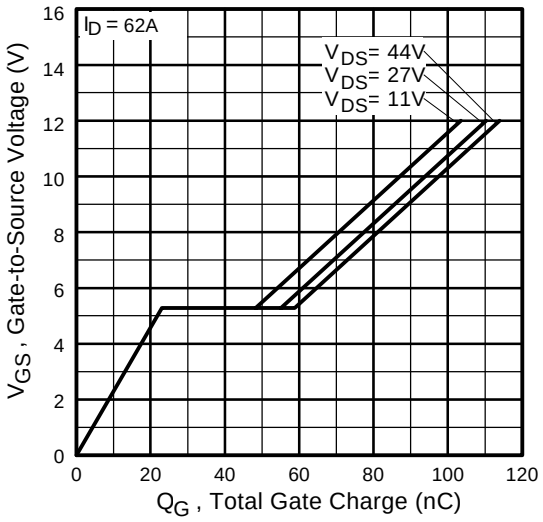


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

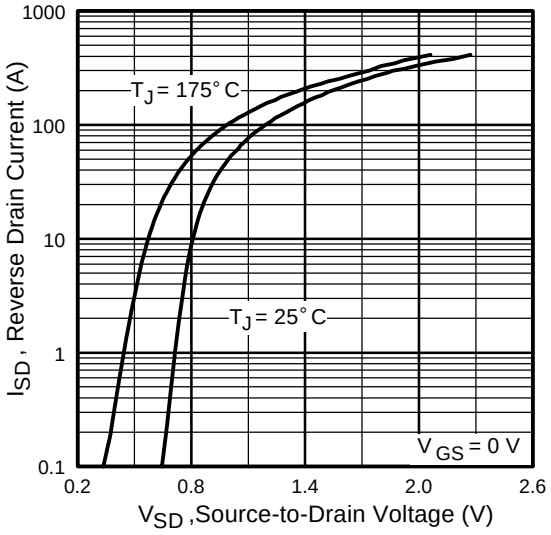


Fig 7. Typical Source-Drain Diode Forward Voltage

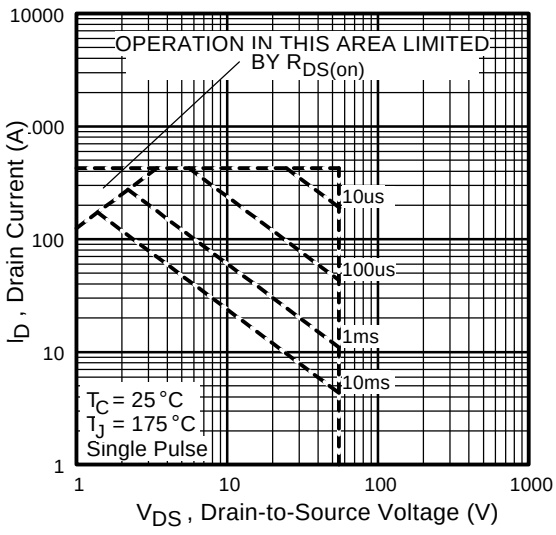


Fig 8. Maximum Safe Operating Area

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

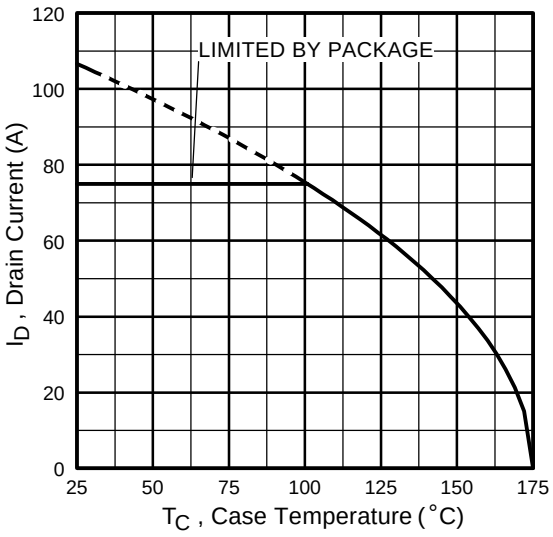


Fig 9. Maximum Drain Current Vs. Case Temperature

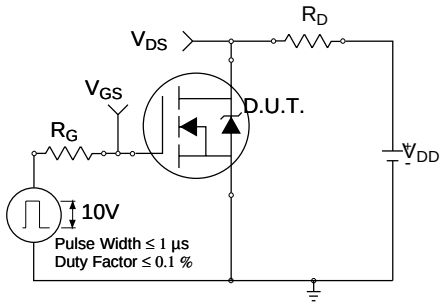


Fig 10a. Switching Time Test Circuit

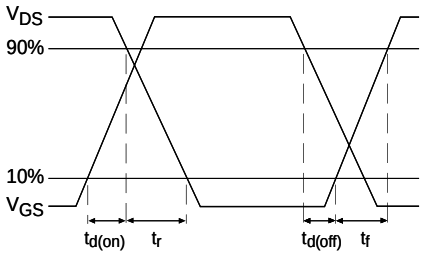


Fig 10b. Switching Time Waveforms

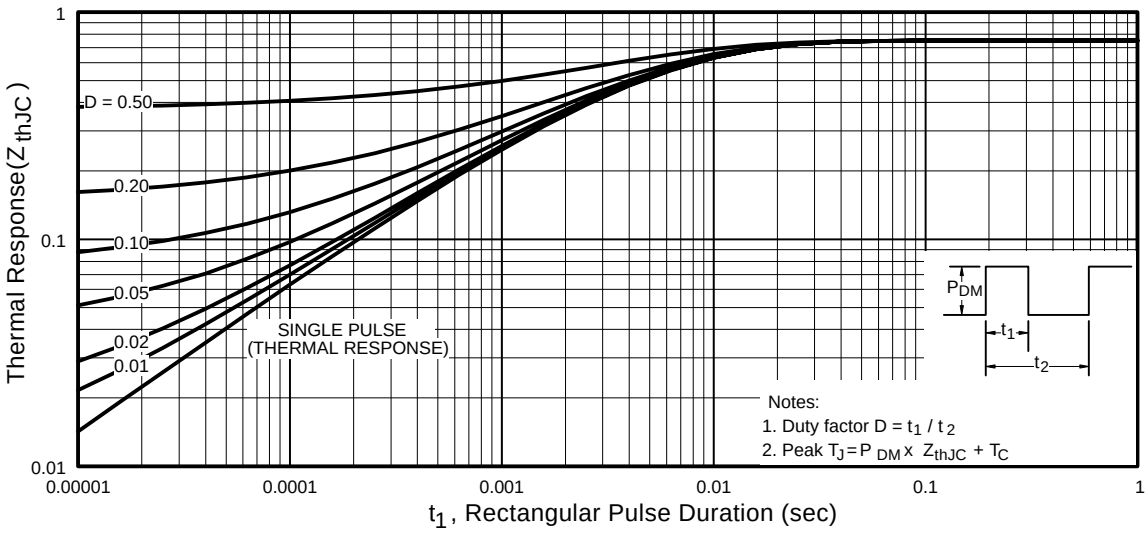


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

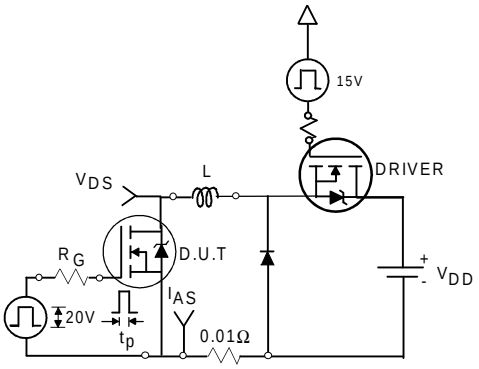


Fig 12a. Unclamped Inductive Test Circuit

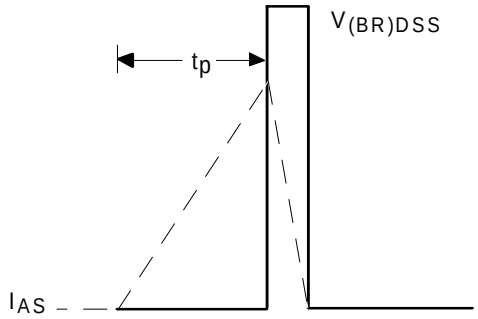


Fig 12b. Unclamped Inductive Waveforms

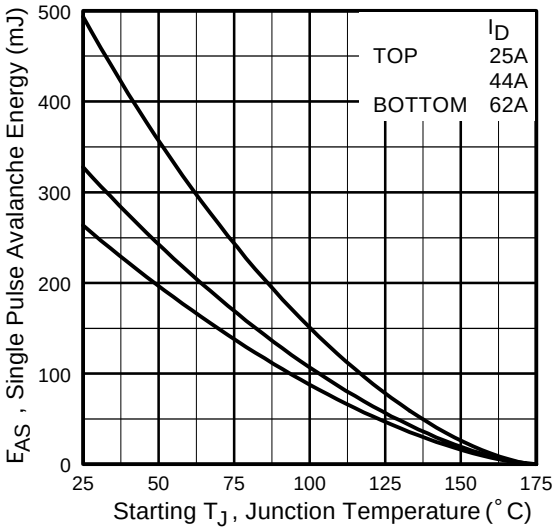


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

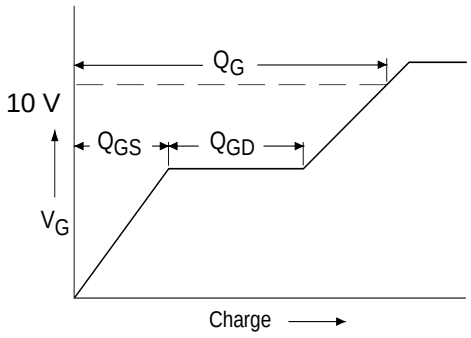


Fig 13a. Basic Gate Charge Waveform

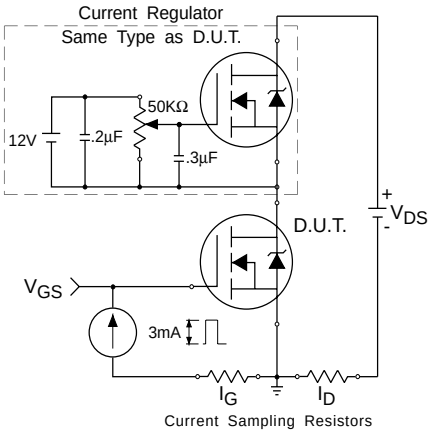
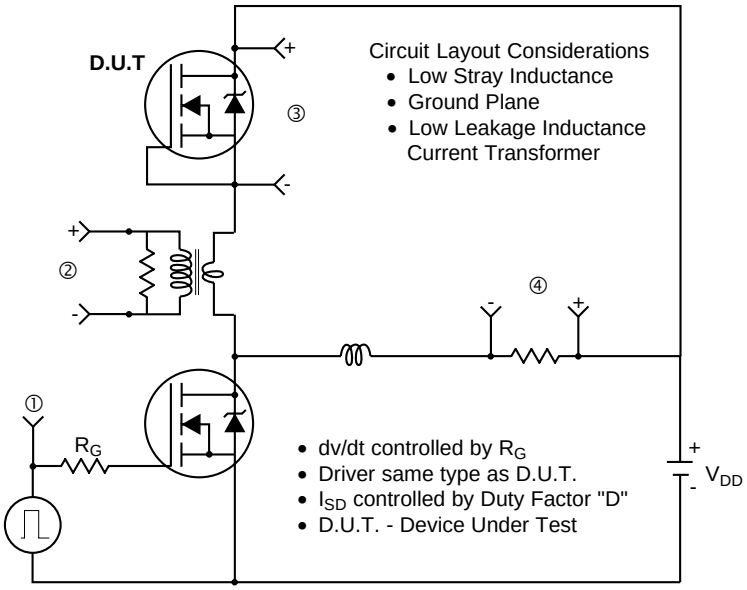
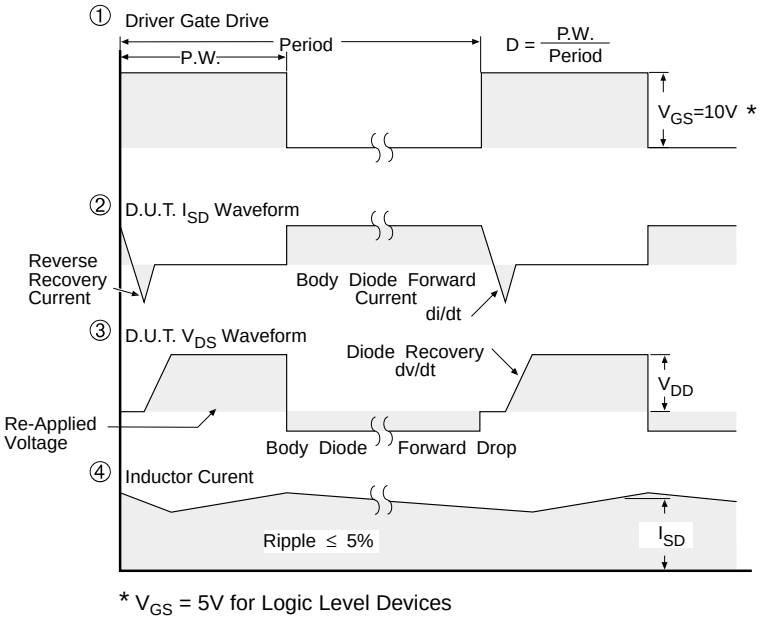


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

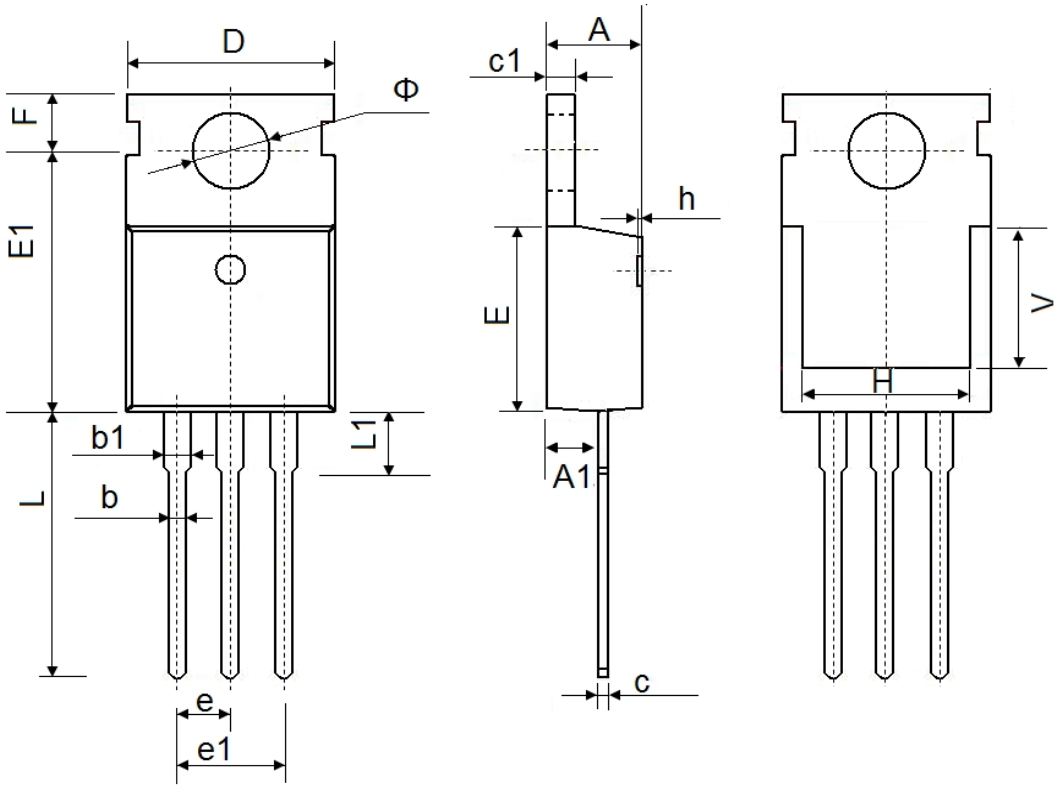




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

TO-220 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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