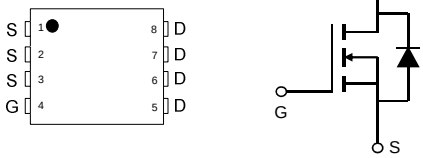
FNK3318

30V N-Channel MOSFET

General Description

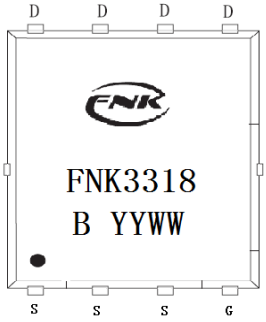
The FNK3318 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$,and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.

Top View



Product Summary

V_{DS}	30V
I_D (at V_{GS}=10V)	80A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 6.5mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 10 mΩ



Marking and pin Assignment

Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25℃	I_D	80	A
	T_C=100℃		56	
Pulsed Drain Current [C]		I_{DM}	200	
Continuous Drain Current	T_A=25℃	I_{DSM}	32	A
	T_A=70℃		24	
Avalanche Current [C]		I_{AS}	34	A
Avalanche energy L=0.1mH [C]		E_{AS}	14	mJ
Power Dissipation [B]	T_C=25℃	P_D	26	W
	T_C=100℃		10	
Power Dissipation [A]	T_A=25℃	P_{DSM}	3.1	W
	T_A=70℃		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		60	75	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4	4.8	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.5	mA
		T_J=125℃			100	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.2	1.7	2.9	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A		5.5	6.5	mΩ
		T_J=125℃		7	11	
		V_{GS}=4.5V, I_D=10A		7.5	10	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A		45		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.4	0.7	V
I_S	Maximum Body-Diode Continuous Current				30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1690		pF
C_{oss}	Output Capacitance			175		pF
C_{rss}	Reverse Transfer Capacitance			120		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.7	1.4	2.1	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=12A		31	44	nC
Q_g(4.5V)	Total Gate Charge			14	20	nC
Q_{gs}	Gate Source Charge			4		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.25Ω, R_{GEN}=3Ω		6		ns
t_r	Turn-On Rise Time			9		ns
$t_{D(off)}$	Turn-Off DelayTime			27		ns
t_f	Turn-Off Fall Time			4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=500A/μs		7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=500A/μs		8		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

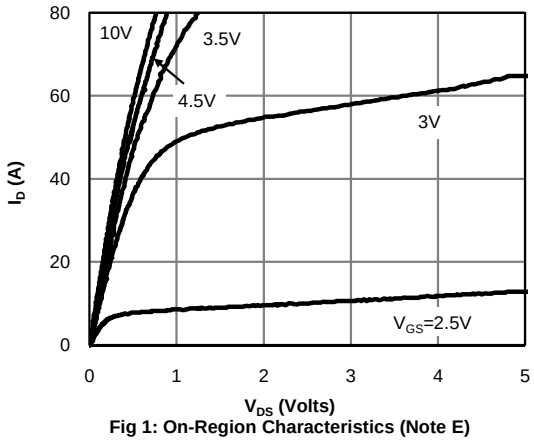


Fig 1: On-Region Characteristics (Note E)

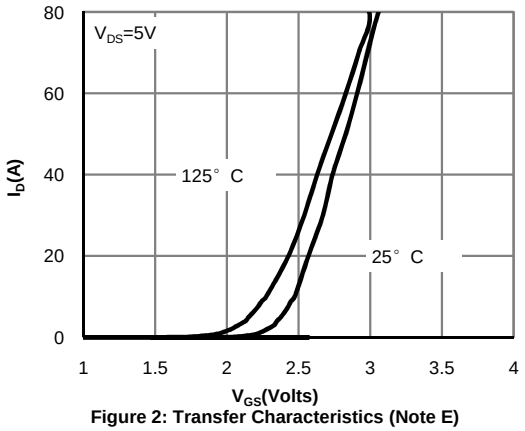


Figure 2: Transfer Characteristics (Note E)

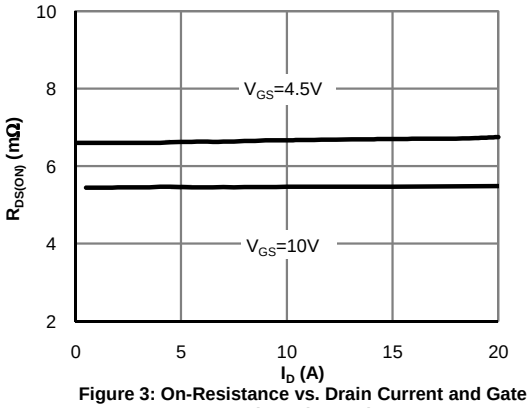


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

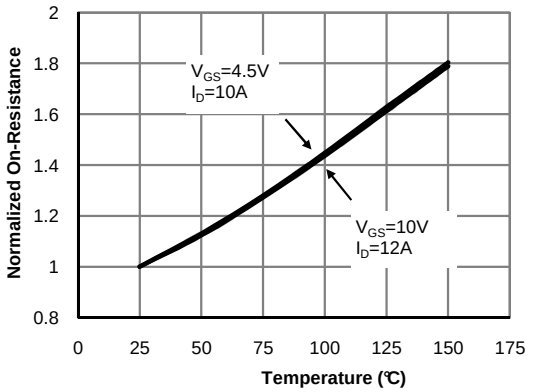


Figure 4: On-Resistance vs. Junction Temperature (Note E)

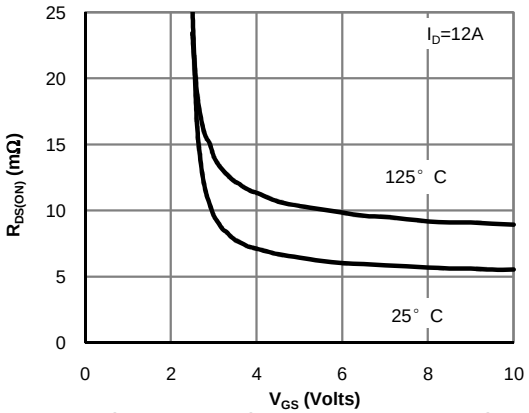


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

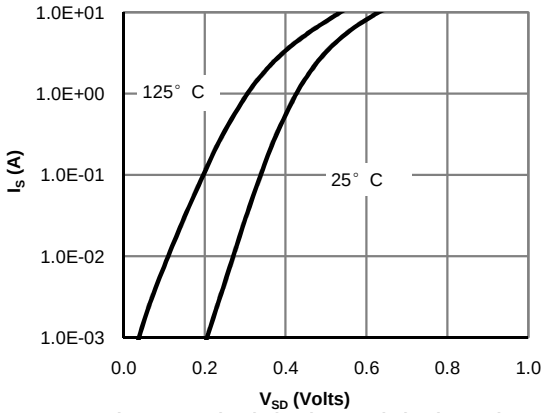


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

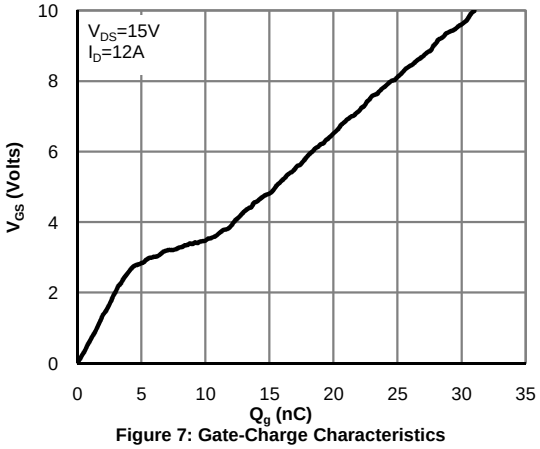


Figure 7: Gate-Charge Characteristics

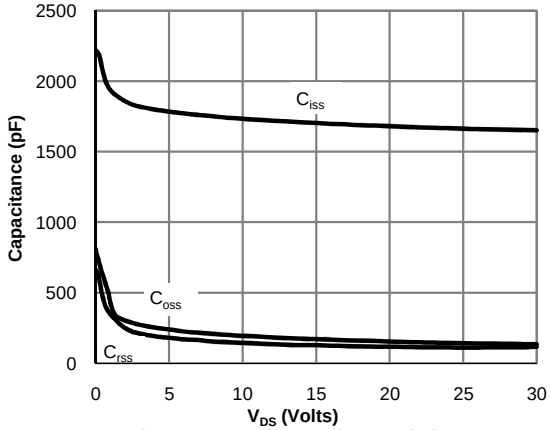


Figure 8: Capacitance Characteristics

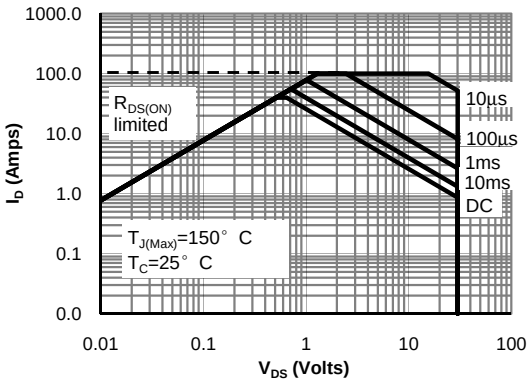


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

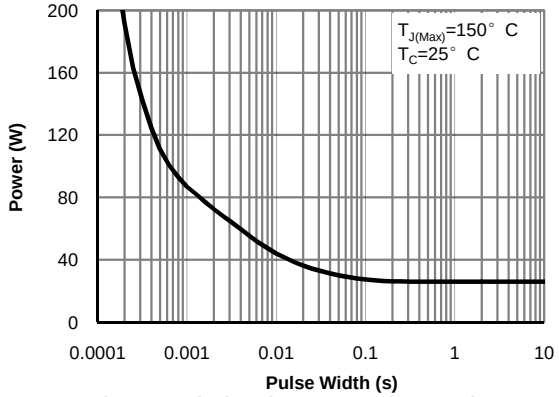


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

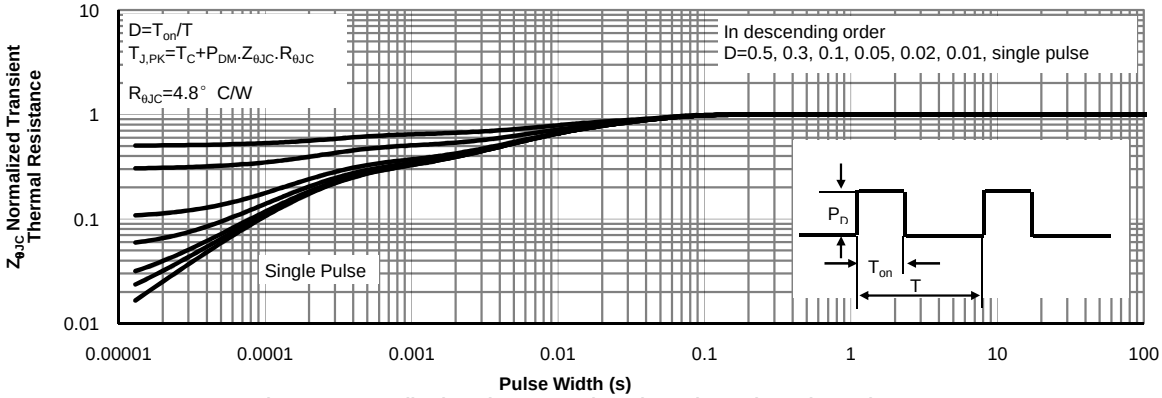


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

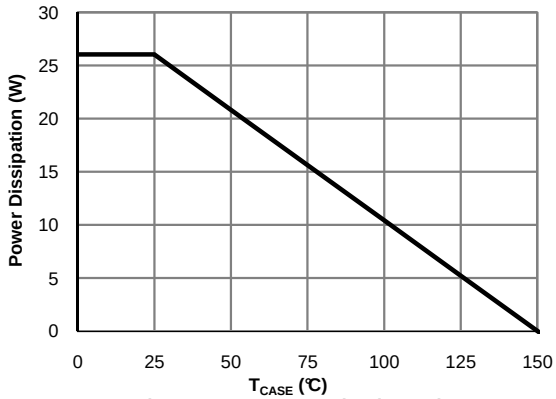


Figure 12: Power De-rating (Note F)

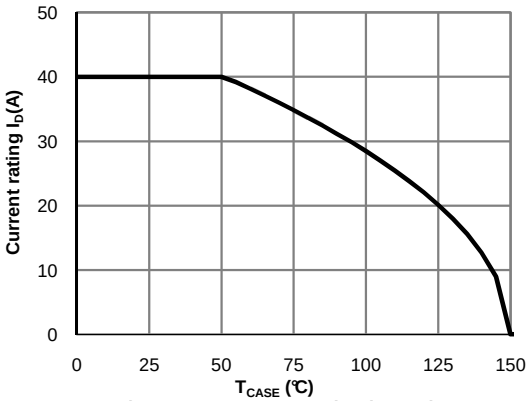


Figure 13: Current De-rating (Note F)

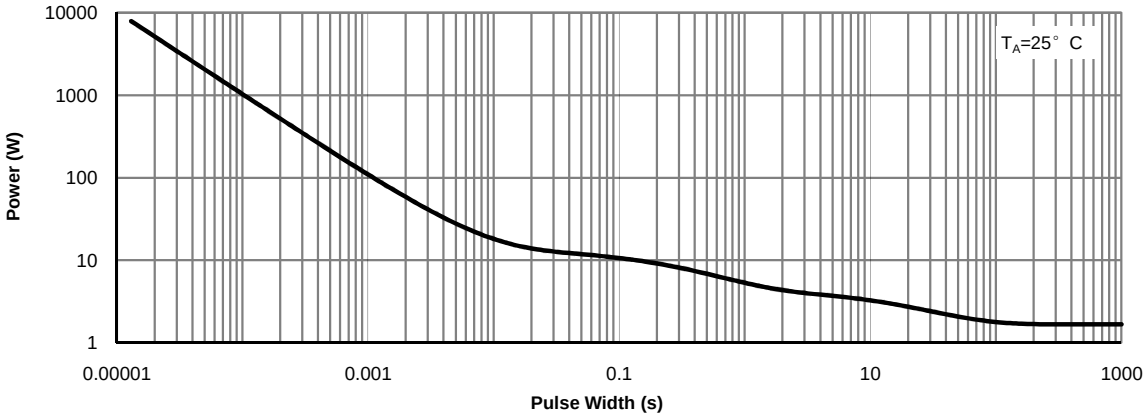


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

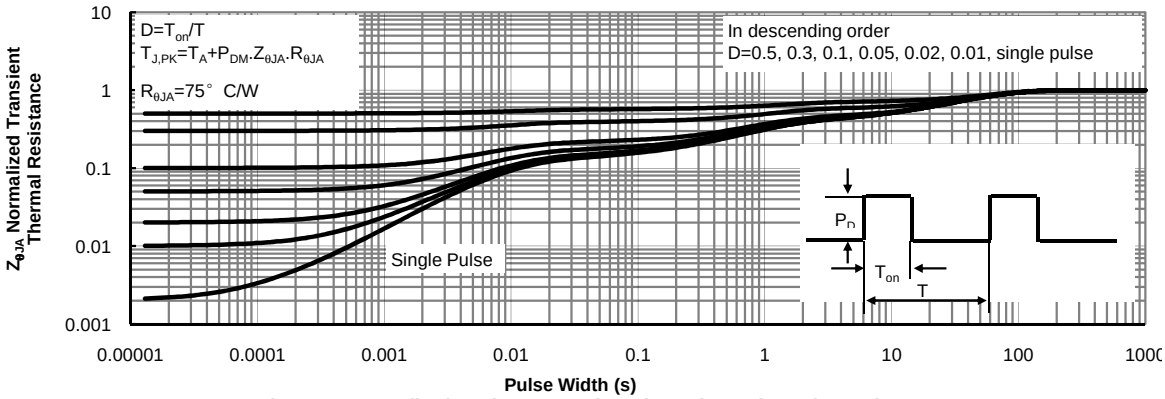


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

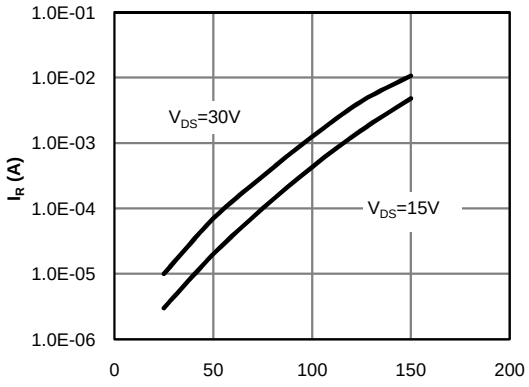


Figure 16: Diode Reverse Leakage Current vs. Junction Temperature

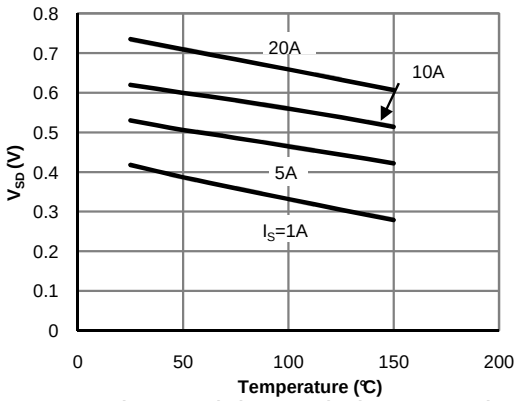


Figure 17: Diode Forward voltage vs. Junction Temperature

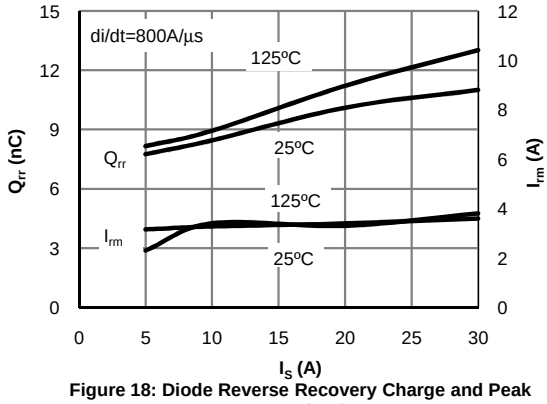


Figure 18: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

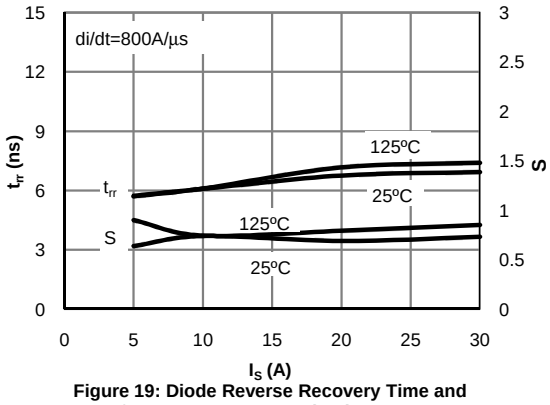


Figure 19: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

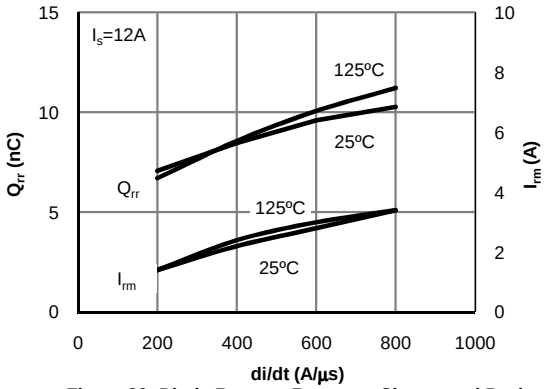


Figure 20: Diode Reverse Recovery Charge and Peak Current vs. di/dt

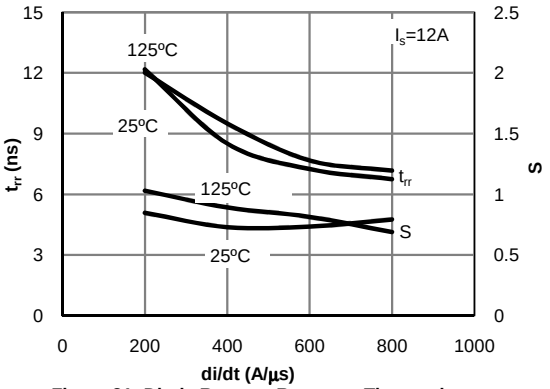
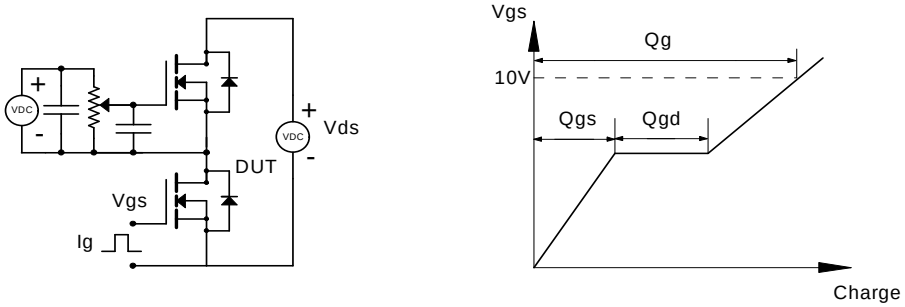
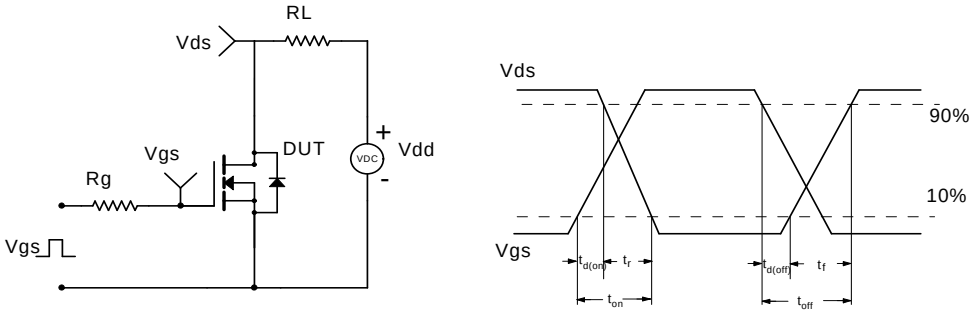


Figure 21: Diode Reverse Recovery Time and Softness Factor vs. di/dt

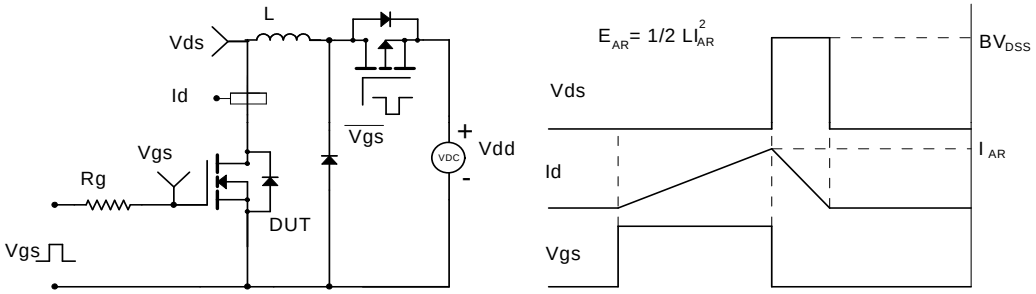
Gate Charge Test Circuit & Waveform



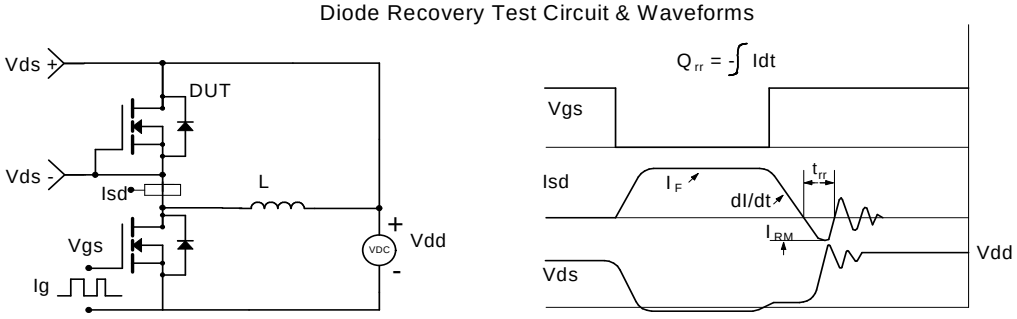
Resistive Switching Test Circuit & Waveforms



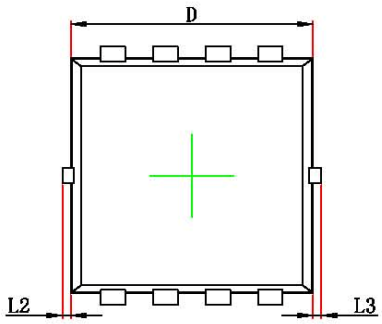
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



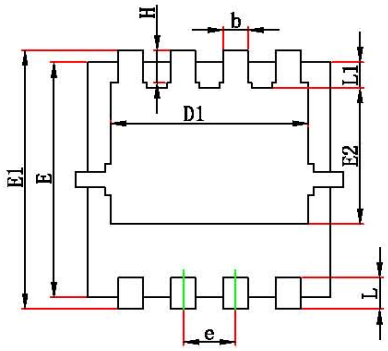
Diode Recovery Test Circuit & Waveforms



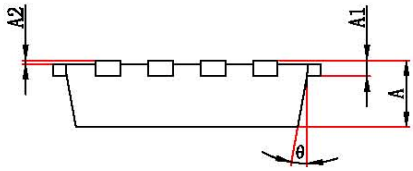
PDFNWB(3 × 3)-8L(P0.65T0.80) PACKAGE OUTLINE DIMENSIONS



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

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- **FNK will supply the best possible product for customers!**