

20V N-Channel MOSFET

General Description

The FNK3328E uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 0.5V while retaining a 12V $V_{GS(MAX)}$ rating. This device is suitable for use as load switch and general purpose FET application.

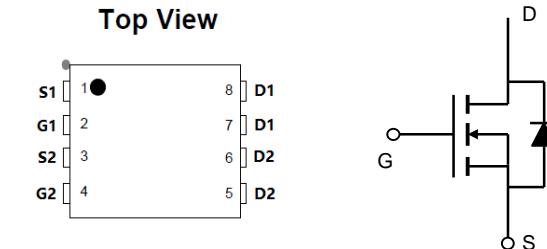
Product Summary

V_{DS} (V) = 20V

I_D = 10A (V_{GS} = 4.5V)

$R_{DS(ON)} < 9m\Omega$ (V_{GS} = 4.5V)

$R_{DS(ON)} < 12m\Omega$ (V_{GS} = 2.5V)



Marking and pin Assignment

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^A	I_D	10	A
$T_A=70^\circ C$		9.2	
Pulsed Drain Current ^B	I_{DM}	40	
Power Dissipation ^A	P_D	3.1	W
$T_A=70^\circ C$		2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	40	°C/W
Steady-State		65	80	°C/W
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	20	25	°C/W



Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=16\text{V}, V_{GS}=0\text{V}$			10	μA
		$T_J=55^\circ\text{C}$			25	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 10\text{V}$			10	μA
BV_{GSO}	Gate-Source Breakdown Voltage	$V_{DS}=0\text{V}, I_G=\pm 250\mu\text{A}$	± 12			V
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.5	0.78	1	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=4.5\text{V}, V_{DS}=5\text{V}$	40			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=4.5\text{V}, I_D=12\text{A}$		7.1	9	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		11	16	
		$V_{GS}=2.5\text{V}, I_D=10.5\text{A}$		8.5	12	
		$V_{GS}=1.8\text{V}, I_D=8.5\text{A}$		14	19	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=12\text{A}$		37		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.73	1	V
I_S	Maximum Body-Diode Continuous Current				4.8	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=10\text{V}, f=1\text{MHz}$		1810		pF
C_{oss}	Output Capacitance			232		pF
C_{rss}	Reverse Transfer Capacitance			200		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		1.6		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=4.5\text{V}, V_{DS}=10\text{V}, I_D=12\text{A}$		17.9		nC
Q_{gs}	Gate Source Charge			1.5		nC
Q_{gd}	Gate Drain Charge			4.7		nC
$t_{\text{D(on)}}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=10\text{V}, R_L=1.0\Omega, R_{\text{GEN}}=3\Omega$		2.5		ns
t_r	Turn-On Rise Time			7.2		ns
$t_{\text{D(off)}}$	Turn-Off DelayTime			49		ns
t_f	Turn-Off Fall Time			10.8		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=12\text{A}, dI/dt=100\text{A}/\mu\text{s}$		20.2		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=12\text{A}, dI/dt=100\text{A}/\mu\text{s}$		8		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

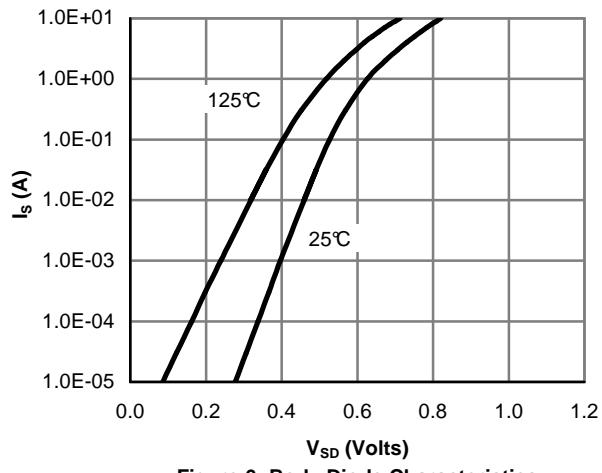
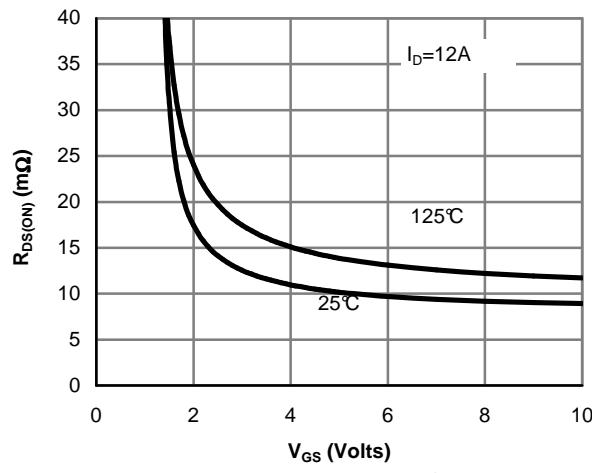
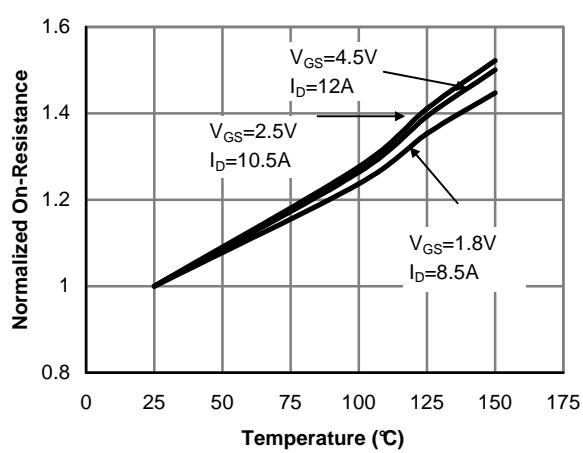
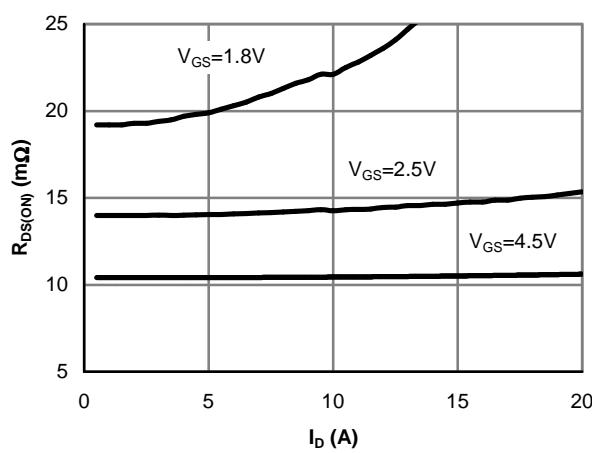
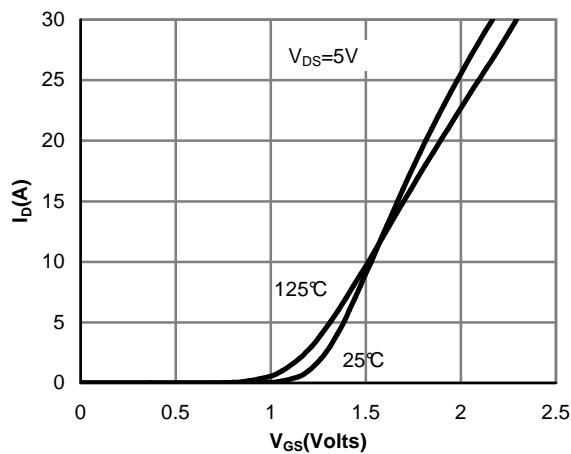
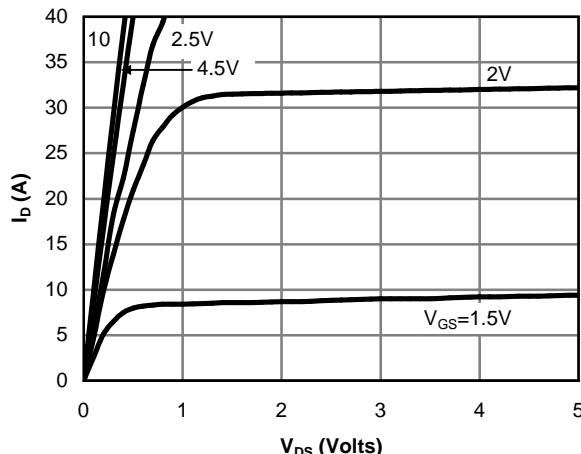
C. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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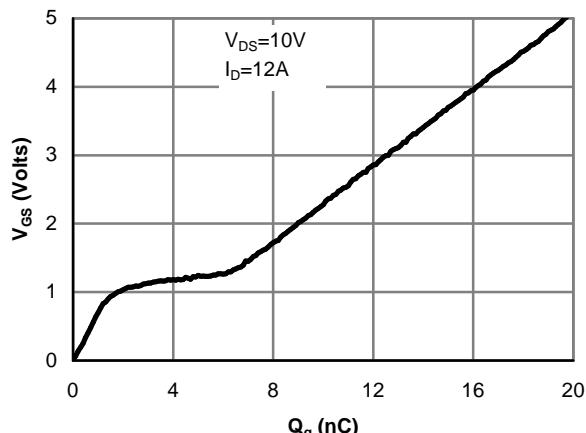


Figure 7: Gate-Charge Characteristics

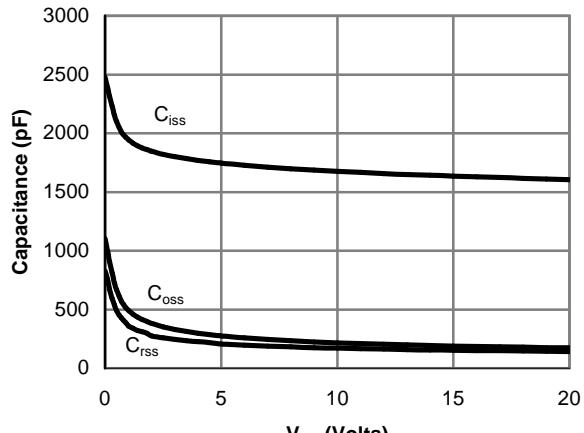


Figure 8: Capacitance Characteristics

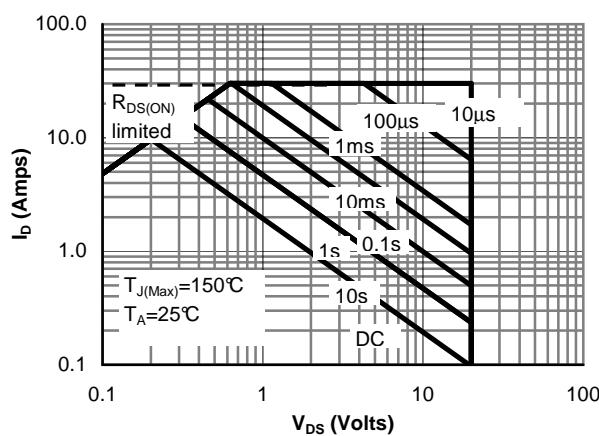


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

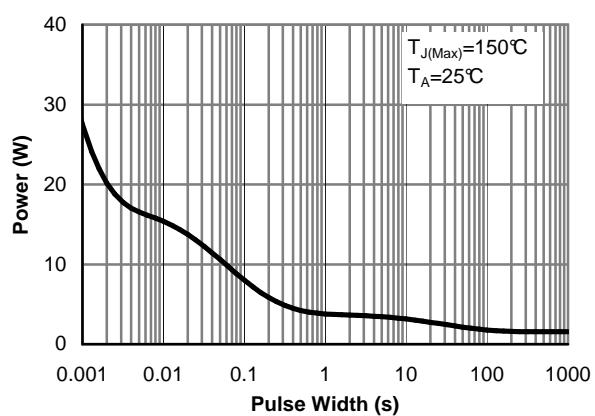


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

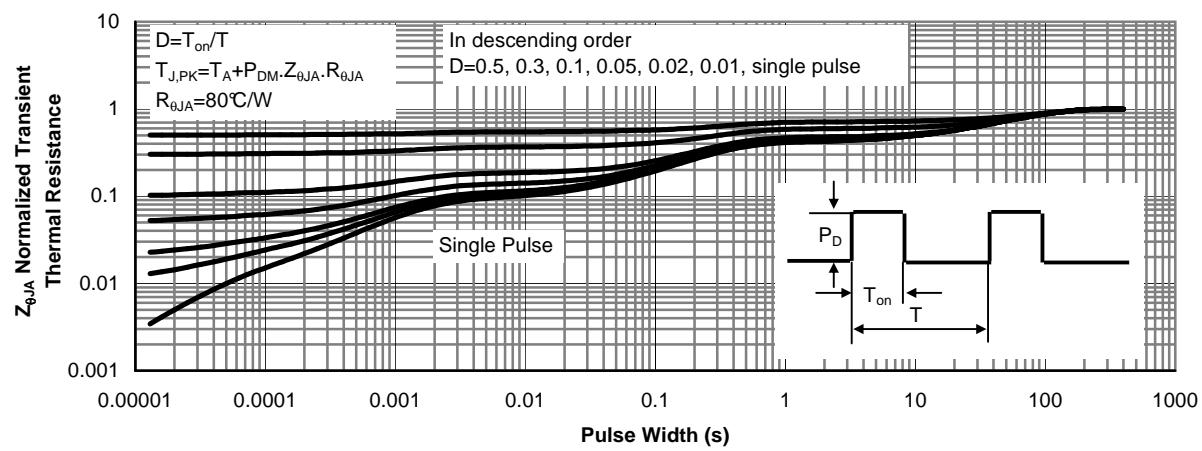
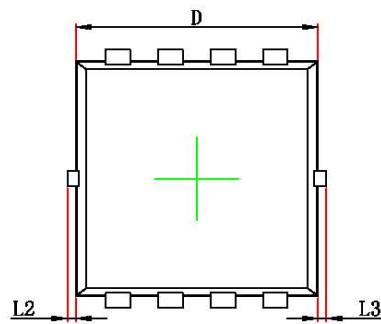


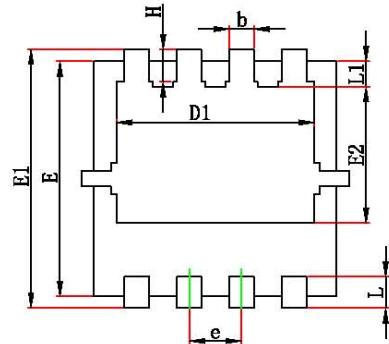
Figure 11: Normalized Maximum Transient Thermal Impedance



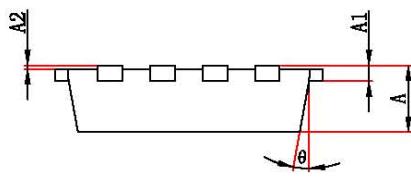
PDFNWB(3 × 3)-8L(P0.65T0.80) PACKAGE OUTLINE DIMENSIONS



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

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