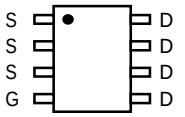
FNK4408
N-Channel Enhancement Mode Field Effect Transistor

General Description

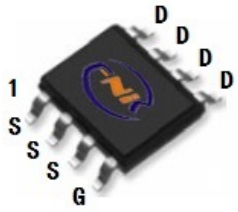
The FNK4408 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and fast switching. This device makes an excellent high side switch for notebook CPU core DC-DC conversion.



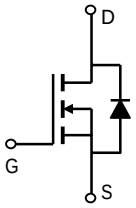
SOIC-8

Features

V_{DS} (V) = 30V
I_D = 12A (V_{GS} = 10V)
$R_{DS(ON)}$ < 11.3mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 14.3mΩ (V_{GS} = 4.5V)



SOP-8 top view



Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [AF]	T_A=25°C	I_D	12	A
	T_A=70°C		10	
Pulsed Drain Current [B]		I_{DM}	120	
Avalanche Current [B]		I_{AV}	30	A
Repetitive Avalanche Energy [B] L=0.3mH		E_{AV}	135	mJ
Power Dissipation	T_A=25°C	P_D	3	W
	T_A=70°C		2.1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	23	40	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		48	65	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	12	16	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±12V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1	1.5	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A		9.8	11.3	mΩ
		T_J=125°C		12	16	
		V_{GS}=4.5V, I_D=10A		11.4	14.3	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10A	30	48		S
V_{SD}	Diode Forward Voltage	I_S=10A,V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				4.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1020	1200	pF
C_{oss}	Output Capacitance			320		pF
C_{rss}	Reverse Transfer Capacitance			80	112	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.13	0.25	0.5	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=12A		10.3	12.5	nC
Q_{gs}	Gate Source Charge			2.1		nC
Q_{gd}	Gate Drain Charge			3.9		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.2Ω, R_{GEN}=3Ω		3.9	5.5	ns
t_r	Turn-On Rise Time			3	6	ns
$t_{D(off)}$	Turn-Off DelayTime			19.2	30	ns
t_f	Turn-Off Fall Time			2.6	5	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=100A/μs		26	32	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=100A/μs		18	32	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. The current rating is based on the ≤ 10s junction to ambient thermal resistance rating.

Rev8: July 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

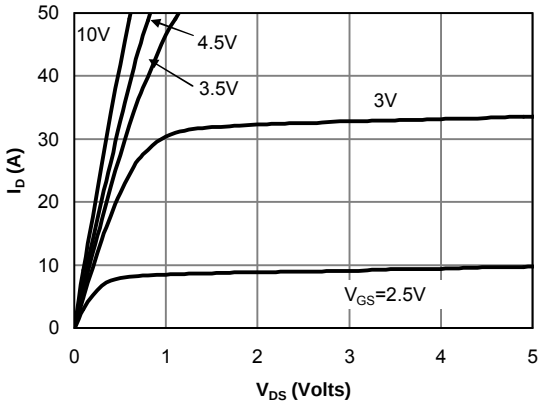


Fig 1: On-Region Characteristics

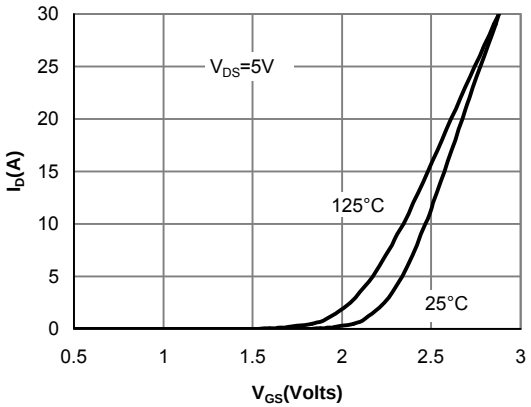


Figure 2: Transfer Characteristics

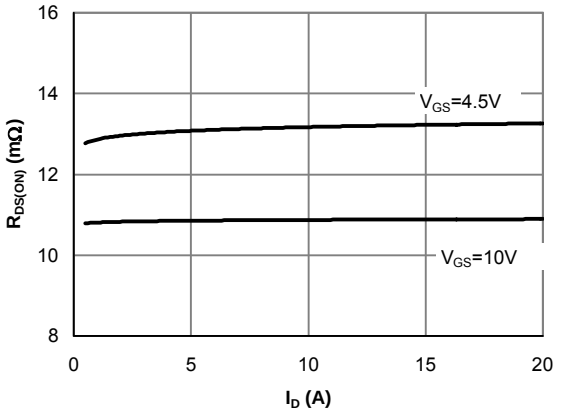


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

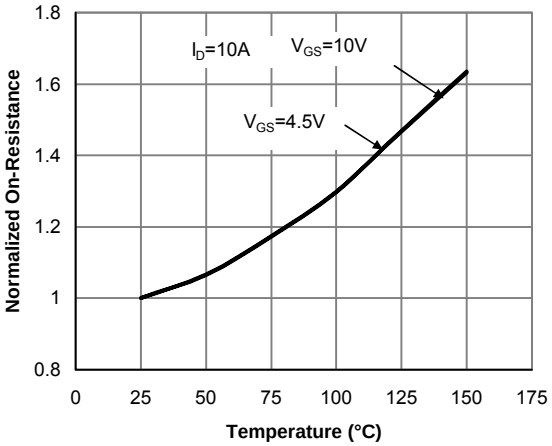


Figure 4: On-Resistance vs. Junction Temperature

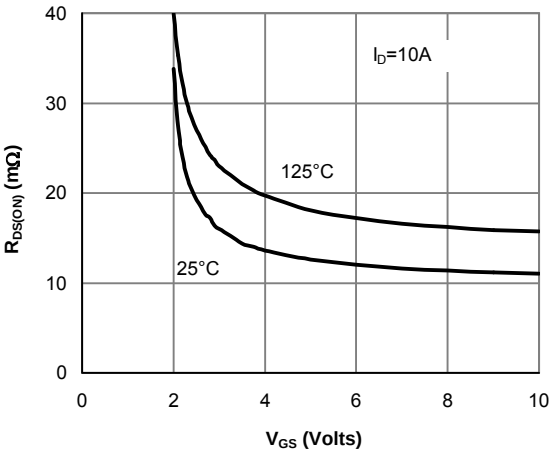


Figure 5: On-Resistance vs. Gate-Source Voltage

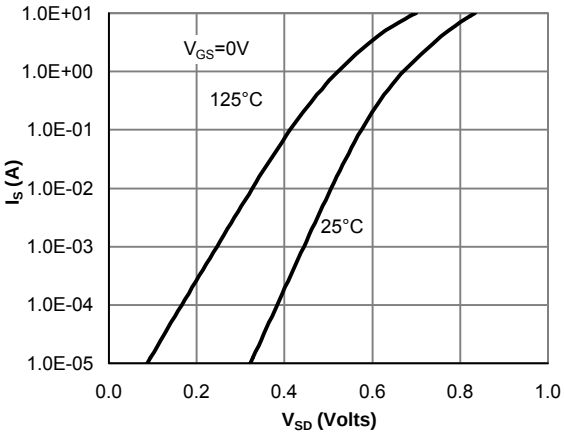


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

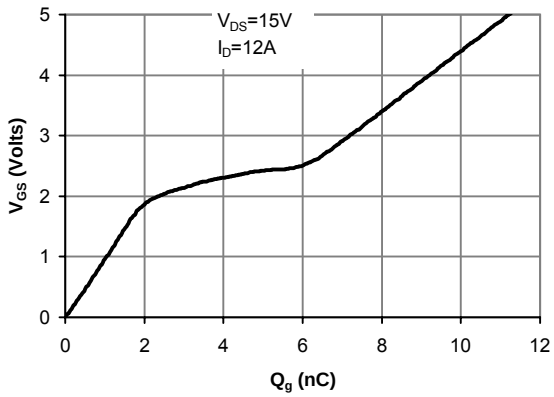


Figure 7: Gate-Charge Characteristics

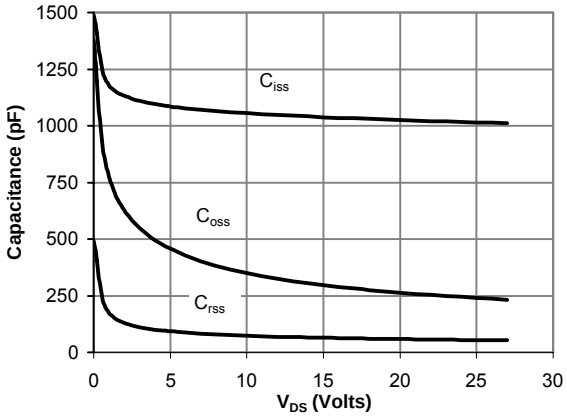


Figure 8: Capacitance Characteristics

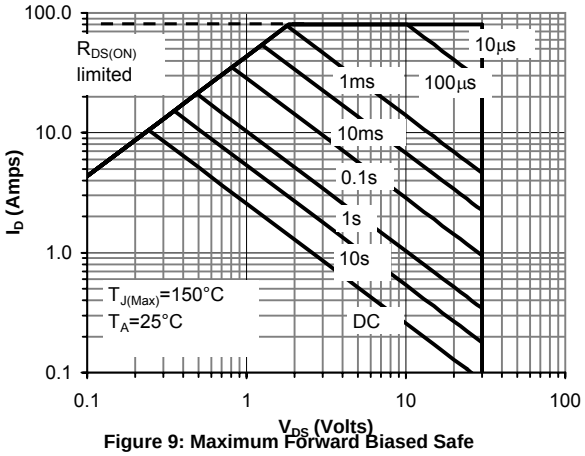


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

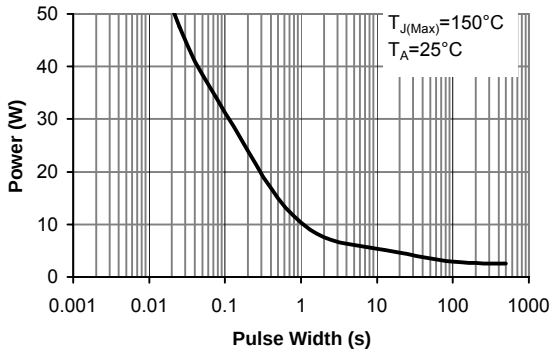


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

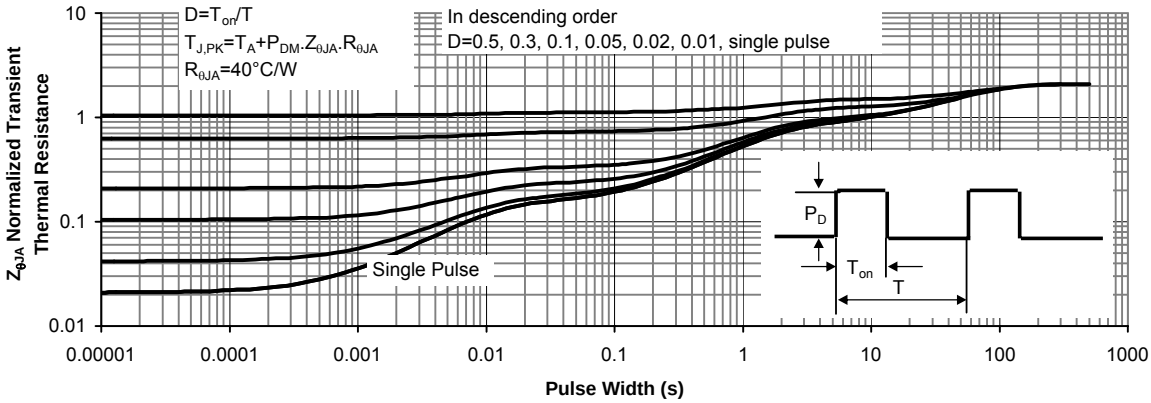


Figure 11: Normalized Maximum Transient Thermal Impedance

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

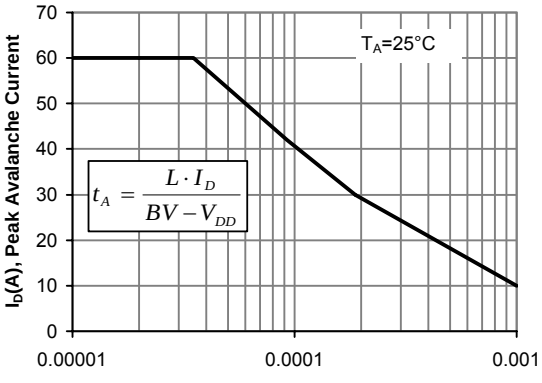


Figure 12: Avalanche capability

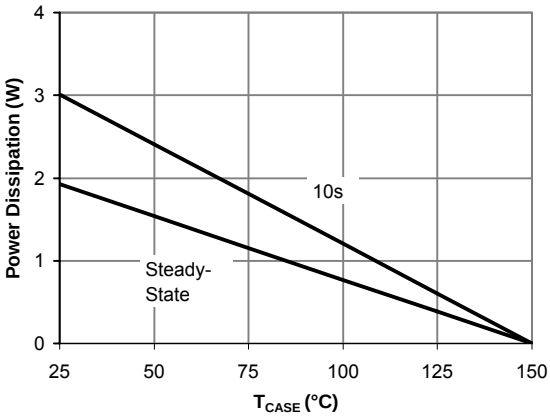
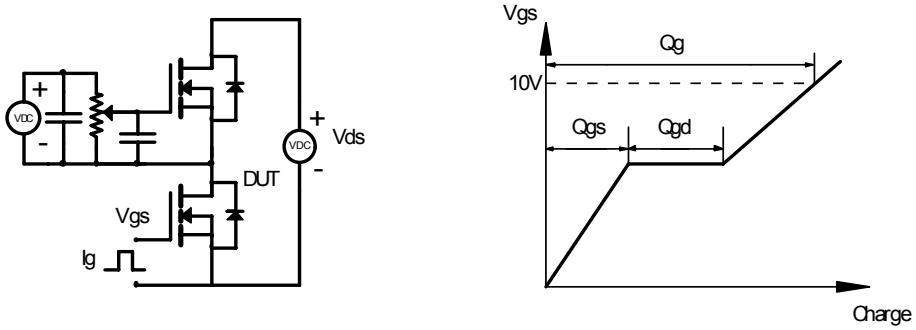
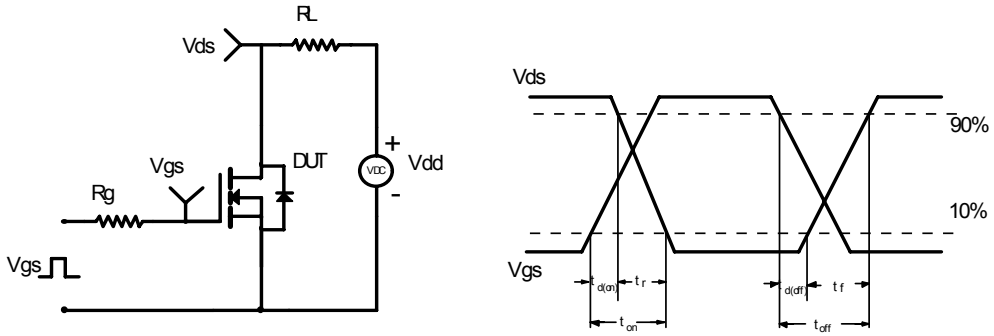


Figure 13: Power De-rating (Note A)

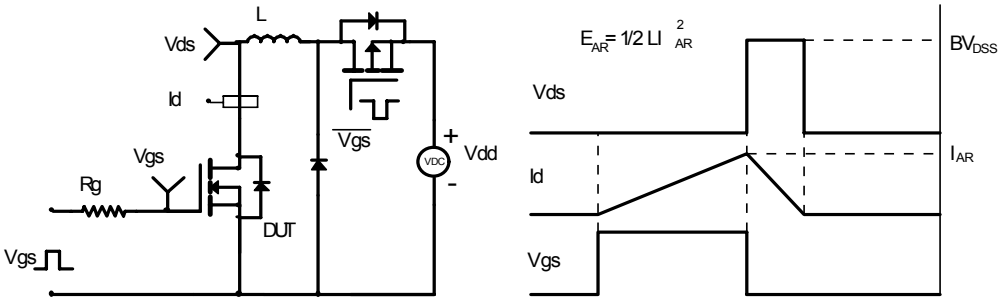
Gate Charge Test Circuit & Waveform



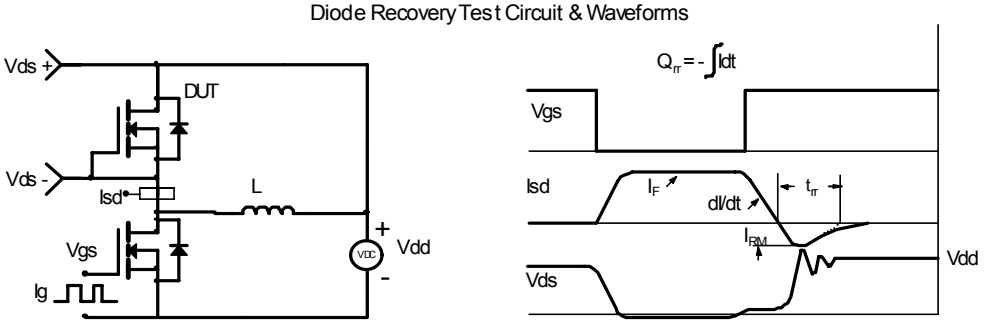
Resistive Switching Test Circuit & Waveforms



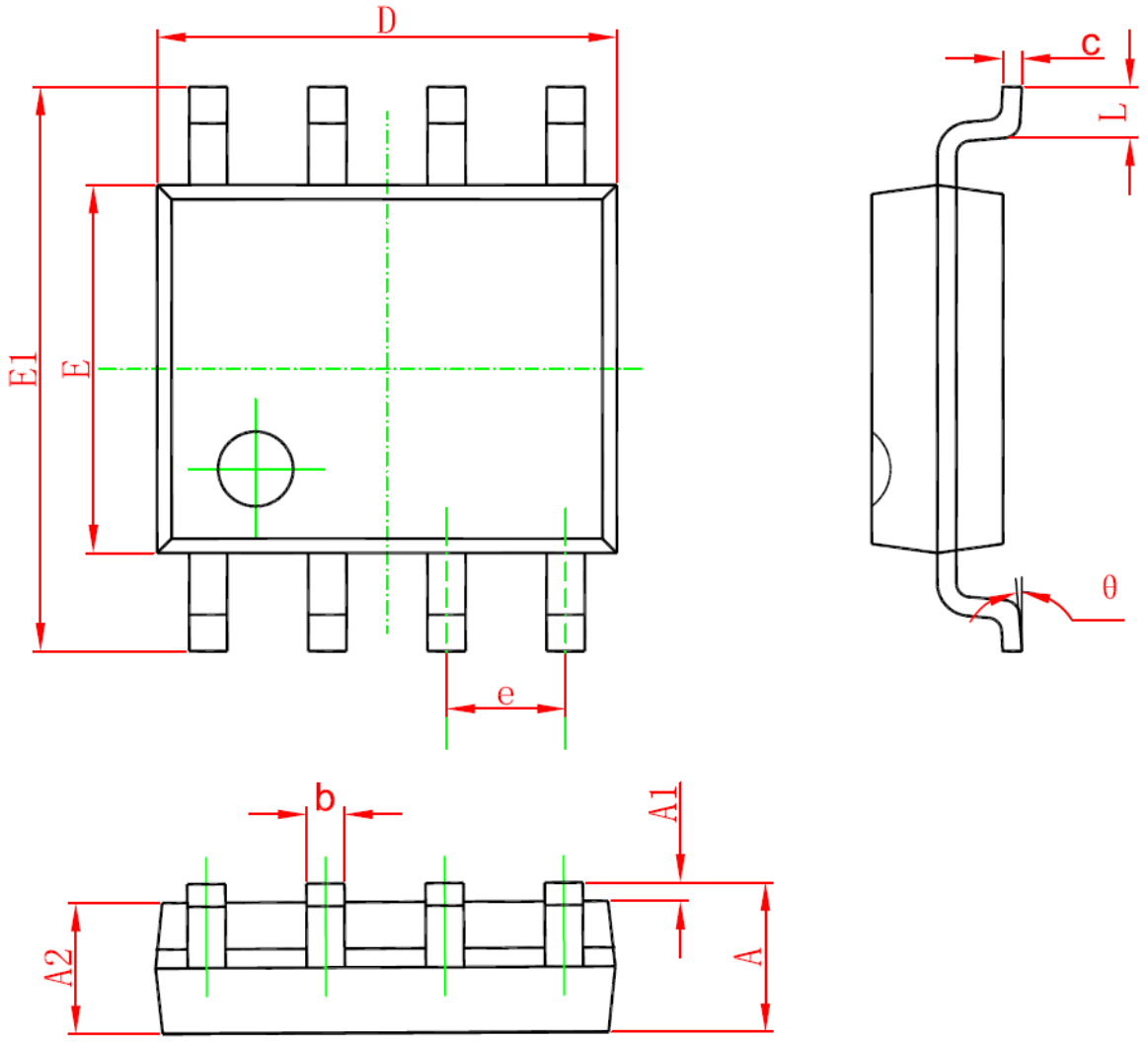
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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