



July 2014

# FOD8160

## High Noise Immunity, 3.3 V / 5 V, 10 Mbit/sec, Logic Gate Optocoupler in Wide-Body SOP 5-Pin

### Features

- Optoplanar<sup>®</sup> Packaging Technology Allows More Than 10 mm Creepage and Clearance Distance, and 0.5 mm Insulation Distance to Achieve Reliable and High Voltage Insulation
- High Noise Immunity Characterized by Common Mode Transient Immunity (CMTI)
  - 20 kV/ $\mu$ s Minimum CMTI
- Specifications Guaranteed Over 3 V to 5.5 V Supply Voltage and -40°C to 100°C Extended Industrial Temperature Range
- High-Speed, 10 Mbit/s Data Rate (NRZ)
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC<sub>RMS</sub> for 1 Minute
  - DIN-EN/IEC60747-5-5, 1,414 V Peak Working Insulation Voltage

### Applications

- Isolating Intelligent Power Module
- Isolating Industrial Communication Interface

### Related Resources

- [www.fairchildsemi.com/products/opto/](http://www.fairchildsemi.com/products/opto/)
- [www.fairchildsemi.com/pf/FO/FODM8061.html](http://www.fairchildsemi.com/pf/FO/FODM8061.html)
- [www.fairchildsemi.com/pf/FO/FODM611.html](http://www.fairchildsemi.com/pf/FO/FODM611.html)

### Description

The FOD8160 is a 3.3 V / 5 V high-speed logic gate optocoupler with open-collector output, which supports isolated communications to allow digital signals to communicate between systems without conducting ground loops or hazardous voltages. The device utilizes Fairchild's proprietary Optoplanar<sup>®</sup> coplanar packaging technology and optimized IC design to achieve high-noise immunity, characterized by high common-mode rejection specifications.

The FOD8160, packaged in a wide-body SOP 5-Pin package, consists of an aluminium gallium arsenide (AlGaAs) LED and an integrated high-speed photodetector. The output of the detector IC is an open collector Schottky-clamped transistor. The electrical and switching characteristics are guaranteed over the extended industrial temperature range of -40°C to 100°C and a  $V_{CC}$  range of 3 V to 5.5 V.

### Functional Schematic

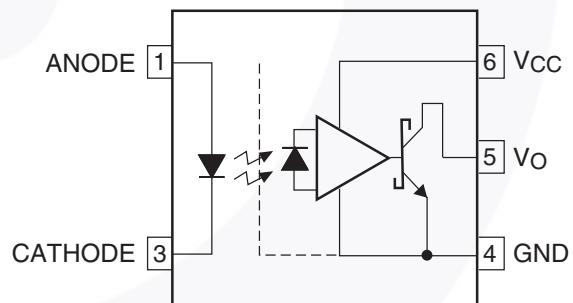


Figure 1. Functional Schematic

FOD8160 — High Noise Immunity, 3.3 V / 5 V, 10 Mbit/sec, Logic Gate Optocoupler in Wide-Body SOP 5-Pin

### Truth Table

LED	Output
Off	HIGH
On	LOW

### Pin Configuration

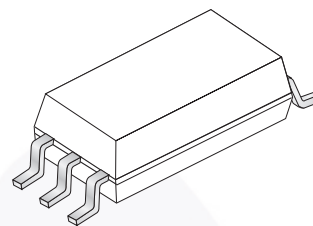
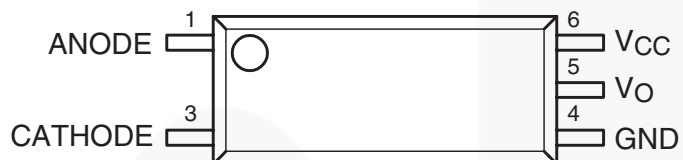


Figure 2. Pin Configuration

### Pin Definitions

Pin #	Name	Description
1	Anode	Anode
3	Cathode	Cathode
4	GND	Output Ground
5	V <sub>O</sub>	Output Voltage
6	V <sub>CC</sub>	Output Supply Voltage

## Safety and Insulation Ratings

As per DIN EN/IEC60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data below. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150 V <sub>RMS</sub>		I-IV		
	For Rated Mains Voltage < 300 V <sub>RMS</sub>		I-IV		
	For Rated Mains Voltage < 450 V <sub>RMS</sub>		I-IV		
	For Rated Mains Voltage < 600 V <sub>RMS</sub>		I-IV		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V <sub>PR</sub>	Input to Output Test Voltage, Method b, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 s, Partial Discharge < 5 pC	2651			V <sub>peak</sub>
	Input to Output Test Voltage, Method a, V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 10 s, Partial Discharge < 5 pC	2262			V <sub>peak</sub>
V <sub>IORM</sub>	Maximum Working Insulation Voltage	1414			V <sub>peak</sub>
V <sub>IOTM</sub>	Highest Allowable Over Voltage	8000			V <sub>peak</sub>
	External Creepage	10.0			mm
	External Clearance	10.0			mm
	Insulation Thickness	0.5			mm
	Safety Limit Values – Maximum Values Allowed in the Event of a Failure				
T <sub>S</sub>	Case Temperature	150			°C
I <sub>S,INPUT</sub>	Input Current	200			mA
P <sub>S,OUTPUT</sub>	Output Power	600			mW
R <sub>IO</sub>	Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V	10 <sup>9</sup>			Ω

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Value	Units
$T_{\text{STG}}$	Storage Temperature	-40 to +125	$^\circ\text{C}$
$T_{\text{OPR}}$	Operating Temperature	-40 to +100	$^\circ\text{C}$
$T_{\text{J}}$	Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_{\text{SOL}}$	Lead Solder Temperature (Refer to Reflow Temperature Profile on page 12)	260 for 10 seconds	$^\circ\text{C}$
<b>Input Characteristics</b>			
$I_{\text{F}}$	Average Forward Input Current	25	mA
$V_{\text{R}}$	Reverse Input Voltage	5.0	V
$\text{PD}_{\text{I}}$	Input Power Dissipation <sup>(1)</sup>	45	mW
<b>Output Characteristics</b>			
$V_{\text{CC}}$	Supply Voltage	0 to 7.0	V
$V_{\text{O}}$	Output Voltage	-0.5 to $V_{\text{CC}} + 0.5$	V
$I_{\text{O}}$	Average Output Current	50	mA
$\text{PD}_{\text{O}}$	Output Power Dissipation <sup>(1)</sup>	85	mW

**Note:**

1. No derating required up to  $100^\circ\text{C}$ .

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$T_{\text{A}}$	Ambient Operating Temperature	-40	+100	$^\circ\text{C}$
$V_{\text{CC}}$	Supply Voltages <sup>(2)</sup>	3.0	5.5	V
$V_{\text{FL}}$	Logic Low Input Voltage	0	0.8	V
$I_{\text{FL}}$	Logic Low Input Current		250	$\mu\text{A}$
$I_{\text{FH}}$	Logic High Input Current	6.0	15	mA
N	Fan Out (at $R_{\text{L}} = 1 \text{ k}\Omega$ )		5	TTL loads
$R_{\text{L}}$	Output Pull-up Resistor	330	4000	$\Omega$

**Note:**

2.  $0.1 \mu\text{F}$  bypass capacitor must be connected between pins 4 and 6.

## Isolation Characteristics

Apply over all recommended conditions, typical value is measured at  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ISO}$	Input-Output Isolation Voltage	$T_A = 25^\circ\text{C}$ , R.H. < 50%, $t = 1.0$ min, $I_{I-O} \leq 20 \mu\text{A}^{(3)(4)}$	5,000			$VAC_{RMS}$
$R_{ISO}$	Isolation Resistance	$V_{I-O} = 500 \text{ V}^{(3)}$		$10^{11}$		$\Omega$
$C_{ISO}$	Isolation Capacitance	$V_{I-O} = 0 \text{ V}$ , frequency = $1.0 \text{ MHz}^{(3)}$		1.0		pF

### Notes:

- Device is considered a two-terminal device: pins 1 and 3 are shorted together and pins 4, 5, and 6 are shorted together.
- 5,000  $VAC_{RMS}$  for 1-minute duration is equivalent to 6,000  $VAC_{RMS}$  for 1-second duration.

## Electrical Characteristics

Apply over all recommended conditions;  $T_A = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ ,  $3.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ ; unless otherwise specified. Typical value is measured at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
<b>Input Characteristics</b>							
$V_F$	Forward Voltage	$I_F = 10 \text{ mA}$	1.05	1.45	1.80	V	3
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/°C	
$BV_R$	Input Reverse Breakdown Voltage	$I_R = 10 \mu\text{A}$	5.0			V	
$I_{FHL}$	Threshold Input Current	$V_O = 0.6 \text{ V}$ , $I_{OL}(\text{sink}) = 13 \text{ mA}$		2.5	6.0	mA	4
<b>Output Characteristics</b>							
$V_{OL}$	Logic Low Output Voltage	$I_F = \text{rated } I_{FHL}$ , $I_{OL}(\text{sink}) = 13 \text{ mA}$		0.4	0.6	V	5
$I_{OH}$	Logic High Output Current	$I_F = 250 \mu\text{A}$ , $V_O = 3.3 \text{ V}$		8.0	50.0	$\mu\text{A}$	6
		$I_F = 250 \mu\text{A}$ , $V_O = 5.0 \text{ V}$		3.0	40.0	$\mu\text{A}$	6
$I_{CCL}$	Logic Low Output Supply Current	$I_F = 10 \text{ mA}$ , $V_{CC} = 3.3 \text{ V}$		5.3	8.5	mA	7, 9
		$I_F = 10 \text{ mA}$ , $V_{CC} = 5.0 \text{ V}$		7.1	10.0	mA	7, 9
$I_{CCH}$	Logic High Output Supply Current	$I_F = 0 \text{ mA}$ , $V_{CC} = 3.3 \text{ V}$		3.5	7.0	mA	8, 9
		$I_F = 0 \text{ mA}$ , $V_{CC} = 5.0 \text{ V}$		5.3	9.0	mA	8, 9

## Switching Characteristics

Apply over all recommended conditions;  $T_A = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $I_F = 6.0\text{ mA}$ ; unless otherwise specified. Typical value is measured at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 3.3\text{ V}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
Data Rate		$R_L = 350\ \Omega$			10	Mbit/sec	
$t_{PHL}$	Propagation Delay to Logic Low Output	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		40	80	ns	10, 11, 15
$t_{PLH}$	Propagation Delay to Logic High Output	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		50	90	ns	10, 11, 15
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		10	35	ns	12, 13, 15
$t_{PSK}$	Propagation Delay Skew	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ <sup>(5)</sup>			40	ns	
$t_R$	Output Rise Time (10% to 90%)	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		20		ns	14, 15
$t_F$	Output Fall Time (90% to 10%)	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		10		ns	14, 15
$ CM_H $	Common-Mode Transient Immunity at Output High	$I_F = 0\text{ mA}$ , $V_O > 2\text{ V}$ , $V_{CM} = 1,000\text{ V}^{(6)}$	20	40		kV/ $\mu\text{s}$	16
$ CM_L $	Common-Mode Transient Immunity at Output Low	$I_F = 6.0\text{ mA}$ , $V_O < 0.8\text{ V}$ , $V_{CM} = 1,000\text{ V}^{(6)}$	20	40		kV/ $\mu\text{s}$	16

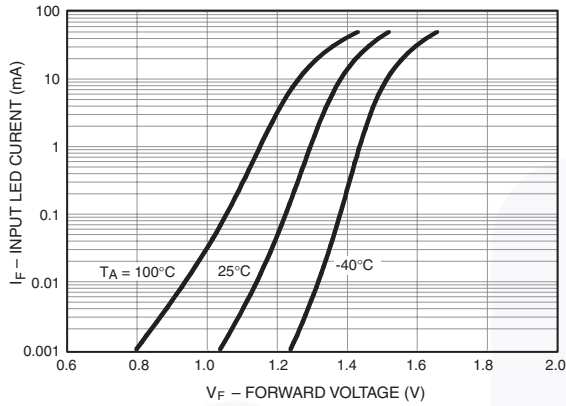
Apply over all recommended conditions;  $T_A = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $I_F = 6.0\text{ mA}$ ; unless otherwise specified. Typical value is measured at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
Data Rate		$R_L = 350\ \Omega$			10	Mbit/sec	
$t_{PHL}$	Propagation Delay to Logic Low Output	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		37	80	ns	10, 11, 15
$t_{PLH}$	Propagation Delay to Logic High Output	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		41	90	ns	10, 11, 15
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		4	25	ns	12, 13, 15
$t_{PSK}$	Propagation Delay Skew	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}^{(5)}$			40	ns	
$t_R$	Output Rise Time (10% to 90%)	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		22		ns	14, 15
$t_F$	Output Fall Time (90% to 10%)	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		9		ns	14, 15
$ CM_H $	Common-Mode Transient Immunity at Output High	$I_F = 0\text{ mA}$ , $V_O > 2\text{ V}$ , $V_{CM} = 1,000\text{ V}^{(6)}$	20	40		kV/ $\mu\text{s}$	16
$ CM_L $	Common-Mode Transient Immunity at Output Low	$I_F = 6.0\text{ mA}$ , $V_O < 0.8\text{ V}$ , $V_{CM} = 1,000\text{ V}^{(6)}$	20	40		kV/ $\mu\text{s}$	16

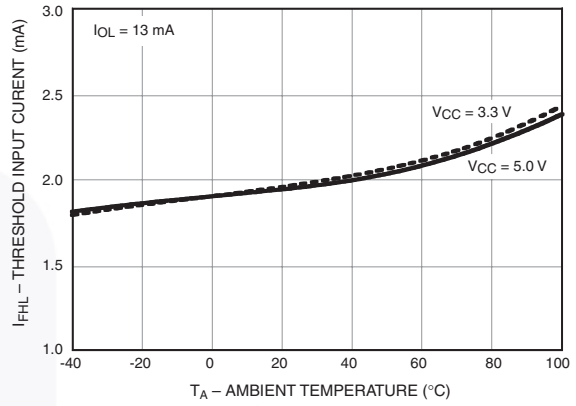
**Notes:**

5.  $t_{PSK}$  is equal to the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between any two units from the same manufacturing date code that are operated at same case temperature ( $\pm 5^{\circ}\text{C}$ ), at same operating conditions, with equal loads ( $R_L = 350\ \Omega$ ,  $C_L = 15\ \text{pF}$ ), and with an input rise time less than 5 ns.
6. Common-mode transient immunity at output HIGH is the maximum tolerable positive  $dV_{cm}/dt$  on the leading edge of the common-mode impulse signal,  $V_{CM}$ , to assure that the output remains HIGH. Common-mode transient immunity at output LOW is the maximum tolerable negative  $dV_{cm}/dt$  on the trailing edge of the common pulse signal,  $V_{CM}$ , to assure that the output remains LOW.

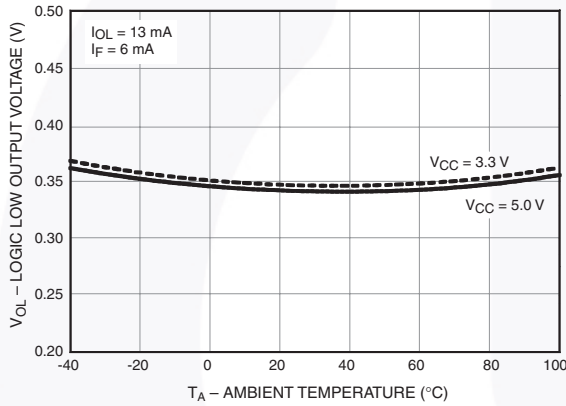
### Typical Performance Characteristics



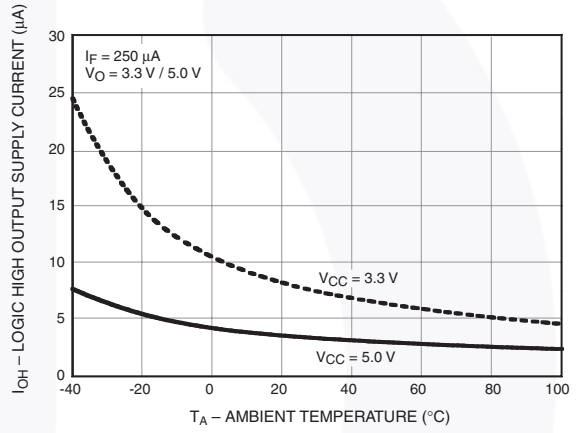
**Figure 3. Input LED Current ( $I_F$ ) vs. Forward Voltage ( $V_F$ )**



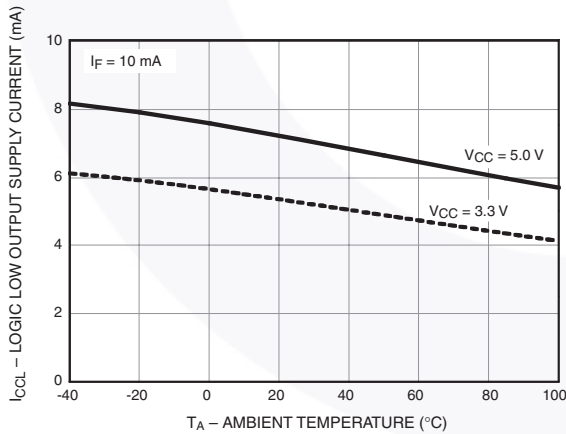
**Figure 4. Threshold Input Current ( $I_{FHL}$ ) vs. Ambient Temperature**



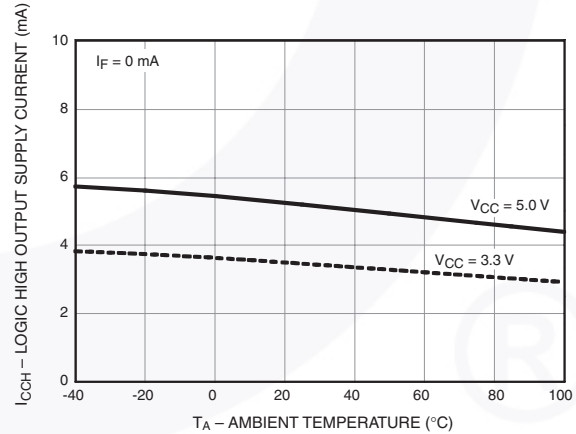
**Figure 5. Logic Low Output Voltage ( $V_{OL}$ ) vs. Ambient Temperature**



**Figure 6. Logic High Output Current ( $I_{OH}$ ) vs. Ambient Temperature**



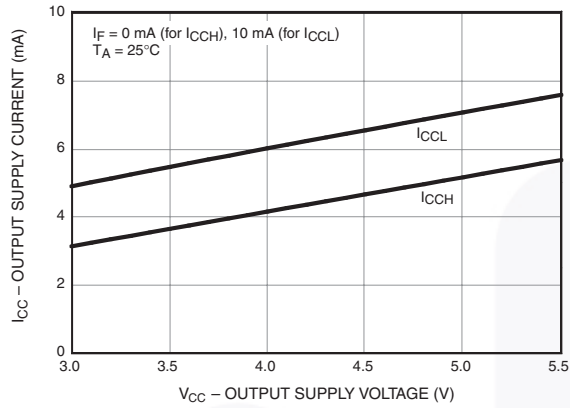
**Figure 7. Logic Low Output Supply Current ( $I_{CCL}$ ) vs. Ambient Temperature**



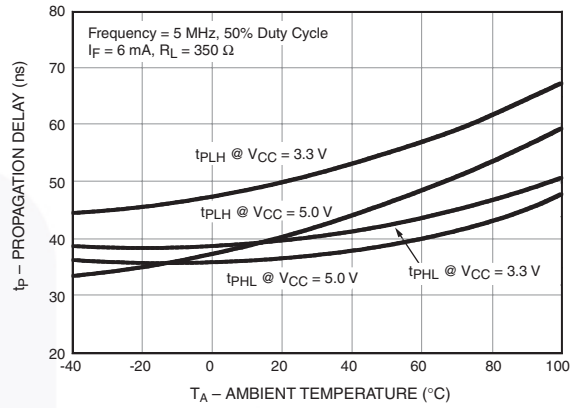
**Figure 8. Logic High Output Supply Current ( $I_{CCH}$ ) vs. Ambient Temperature**



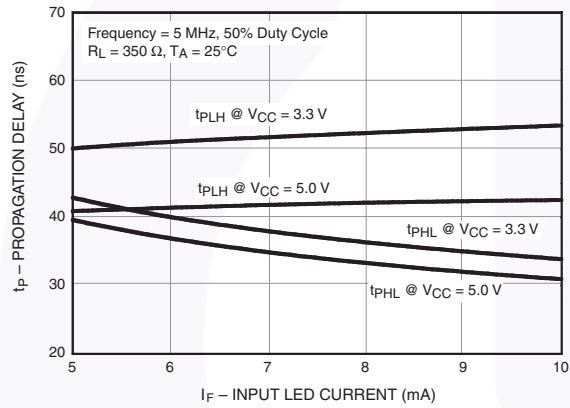
### Typical Performance Characteristics (Continued)



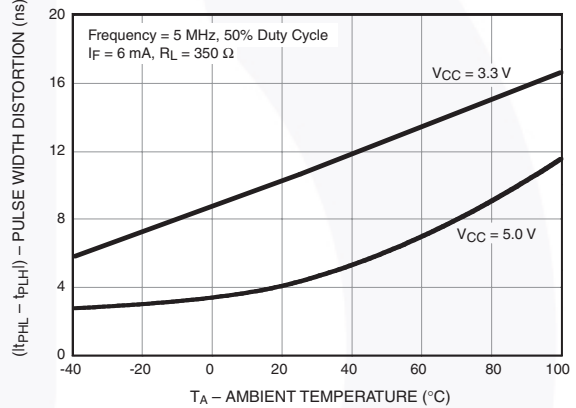
**Figure 9. Output Supply Current ( $I_{CC}$ ) vs. Output Supply Voltage ( $V_{CC}$ )**



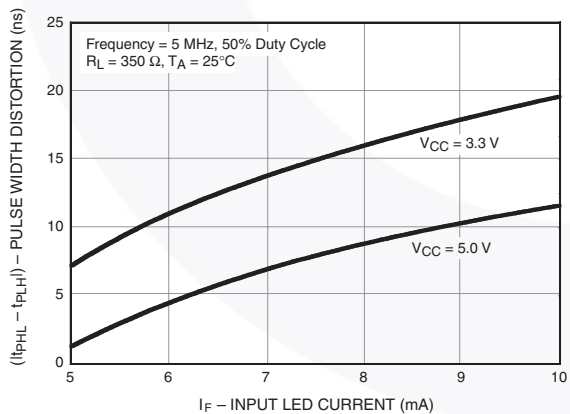
**Figure 10. Propagation Delay vs. Ambient Temperature**



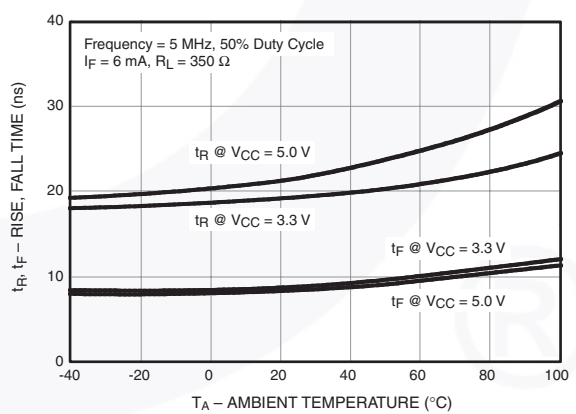
**Figure 11. Propagation Delay vs. Input LED Current ( $I_F$ )**



**Figure 12. Pulse Width Distortion vs. Ambient Temperature**

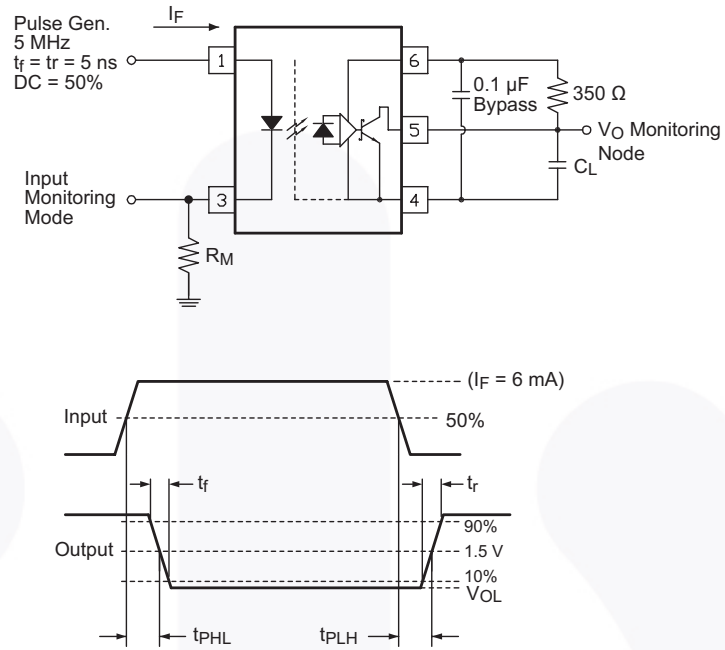


**Figure 13. Pulse Width Distortion vs. Input LED Current ( $I_F$ )**

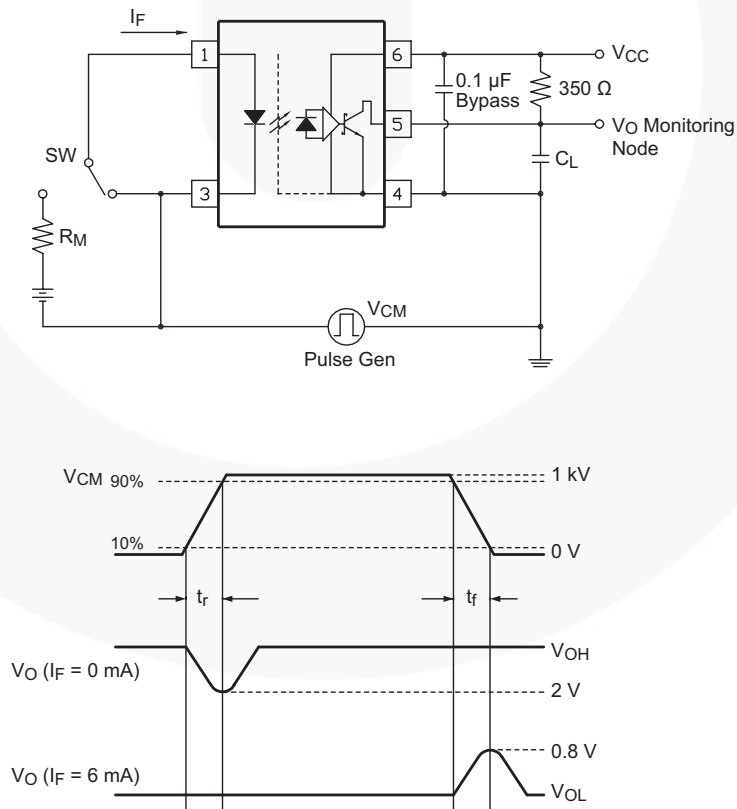


**Figure 14. Rise Time ( $t_r$ ) and Fall Time ( $t_f$ ) vs. Ambient Temperature**

### Test Circuit




**Figure 15. Test Circuit for Propagation Delay, Rise Time, and Fall Time**



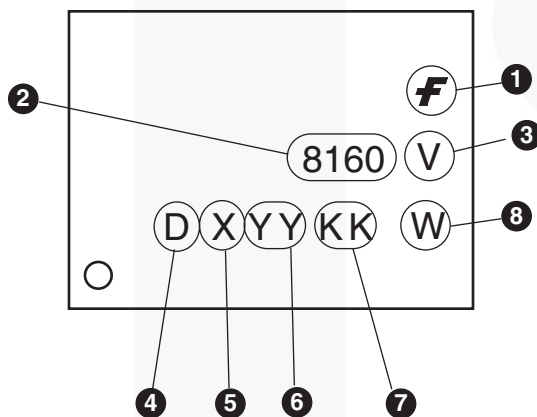
**Figure 16. Test Circuit for Instantaneous Common-Mode Rejection Voltage**

## Ordering Information

Part Number	Package	Packing Method
FOD8160	Wide Body SOP 5-Pin	Tube (100 units per tube)
FOD8160R2	Wide Body SOP 5-Pin	Tape and Reel (1,000 units per reel)
FOD8160V	Wide Body SOP 5-Pin, DIN EN/IEC60747-5-5 Option	Tube (100 units per tube)
FOD8160R2V	Wide Body SOP 5-Pin, DIN EN/ IEC60747-5-5 Option	Tape and Reel (1,000 units per reel)

 All packages are lead free per JEDEC: J-STD-020B standard.

## Marking Information



### Definitions

1	Fairchild logo
2	Device number, e.g., '8160' for FOD8160
3	DIN EN/IEC60747-5-5 option (only appears on component ordered with this option)
4	Plant code, e.g., 'D'
5	Last-digit year code, e.g., 'E' for 2014
6	Two-digit work week ranging from '01' to '53'
7	Lot-traceability code
8	Package assembly code, W

## Reflow Profile

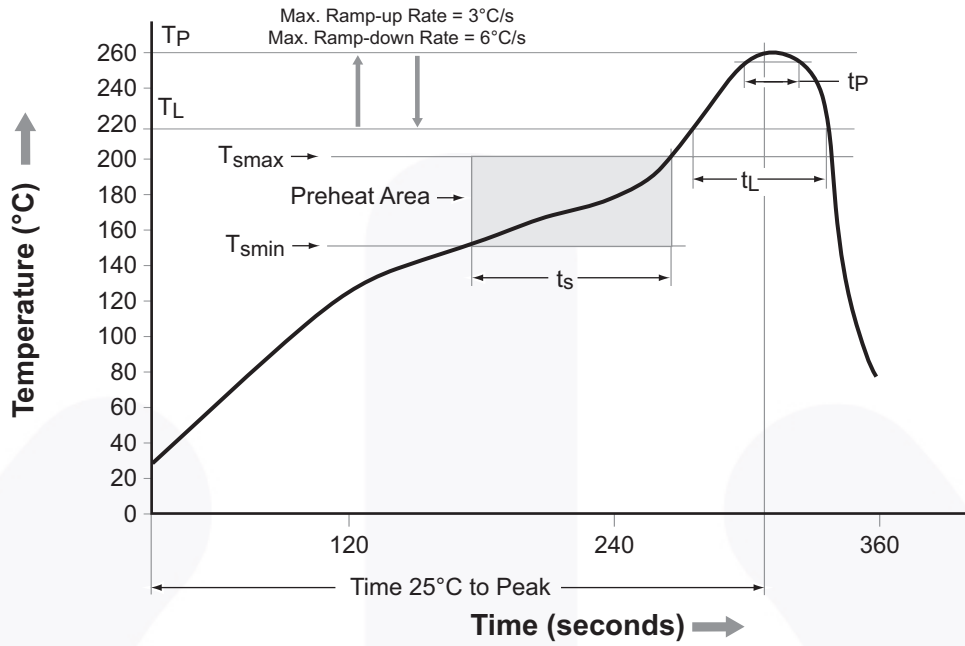
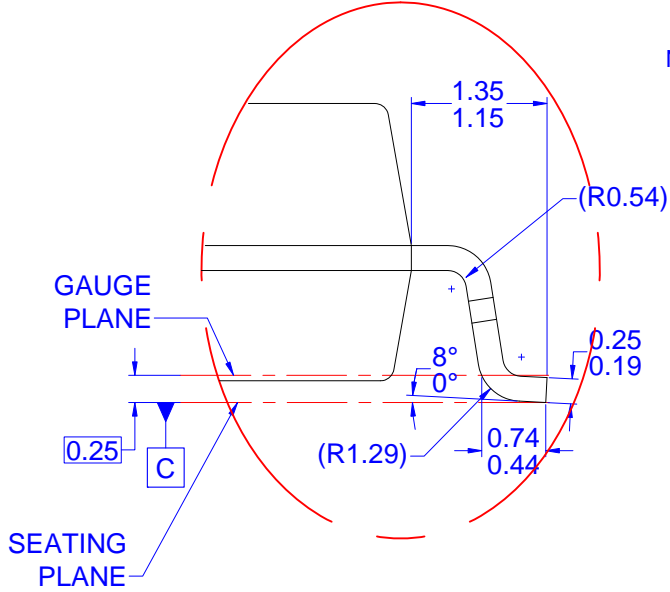
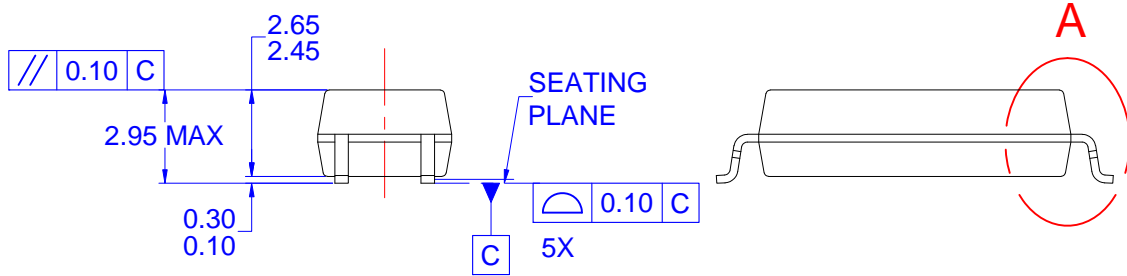
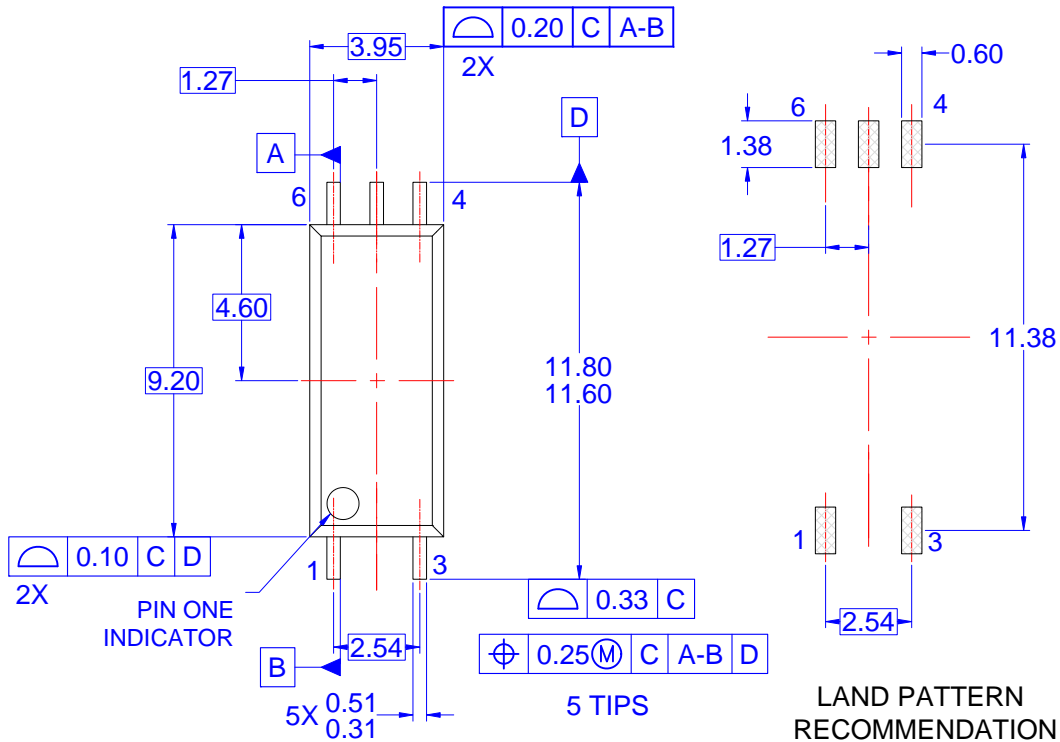


Figure 17. Reflow Profile

Profile Feature	Pb-Free Assembly Profile
Temperature Minimum ( $T_{smin}$ )	150°C
Temperature Maximum ( $T_{smax}$ )	200°C
Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )	60 to 120 seconds
Ramp-Up Rate ( $t_L$ to $t_P$ )	3°C/second maximum
Liquidous Temperature ( $T_L$ )	217°C
Time ( $t_L$ ) Maintained Above ( $T_L$ )	60 to 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time ( $t_P$ ) within 5°C of 260°C	30 seconds
Ramp-Down Rate ( $T_P$ to $T_L$ )	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum



**DETAIL A**  
SCALE: 3.2:1

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT CONFORM TO ANY STANDARD.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
  - D) DRAWING CONFORMS TO ASME Y14.5M-1994
  - E) DRAWING FILE NAME: MKT-M05AREV3

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