

# FOD8316

## 2.5A Output Current, IGBT Drive Optocoupler with Desaturation Detection and Isolated Fault Sensing

### Features

- High Noise Immunity characterized by common mode rejection
  - 35kV/μs Minimum Common Mode Rejection ( $V_{cm} = 1500V_{pk}$ )
- 2.5A peak output current driving capability for most 1200V/150A IGBT
- Optically isolated fault sensing feedback
- “Soft” IGBT turn-off
- Built-in IGBT protection
  - Desaturation detection
  - Under voltage lockout protection
- 1,414V (peak) working voltage rating
- 8,000V (peak) transient isolation voltage rating
- Wide supply voltage range from 15V to 30V
  - Use of P-Channel MOSFETs at output stage enables output voltage swing close to the supply rail (rail-to-rail output)
- 3.3V/5V, CMOS/TTL compatible inputs
- High Speed
  - 500ns max. propagation delay over full operating temperature range
- Extended industrial temperature range, -40°C to 100°C temperature range
- Safety and regulatory
  - UL1577, 4,243  $V_{RMS}$  for 1 min.
  - DIN EN/IEC 60747-5-5
- $R_{DS(ON)}$  of 1Ω (typ.) offers lower power dissipation
- User configurable: inverting, non-inverting, auto-reset, auto-shutdown
- 8mm creepage and clearance distances

### Applications

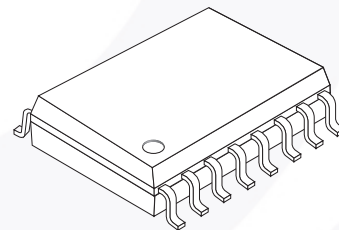
- Industrial inverter
- Induction heating
- Isolated IGBT drive

### Description

The FOD8316 is an advanced 2.5A Output Current IGBT Drive Optocoupler, capable of driving most 1200V/150A IGBTs. It is ideally suited for fast switching driving of power IGBTs and MOSFETs used in motor control inverter applications and high performance power systems. It offers critical protection features necessary for preventing fault conditions that lead to destructive thermal runaway of IGBTs.

It utilizes Fairchild’s patented coplanar packaging technology, Optoplanar®, and optimized IC design to achieve high noise immunity, characterized by high common mode rejection and power supply rejection specifications.

It consists of an integrated gate drive optocoupler featuring low  $R_{DS(ON)}$  CMOS transistors to drive the IGBT from rail to rail and an integrated high speed isolated feedback for fault sensing. The device is housed in a compact 16-pin small outline plastic package which meets the 8mm creepage and clearance requirements.

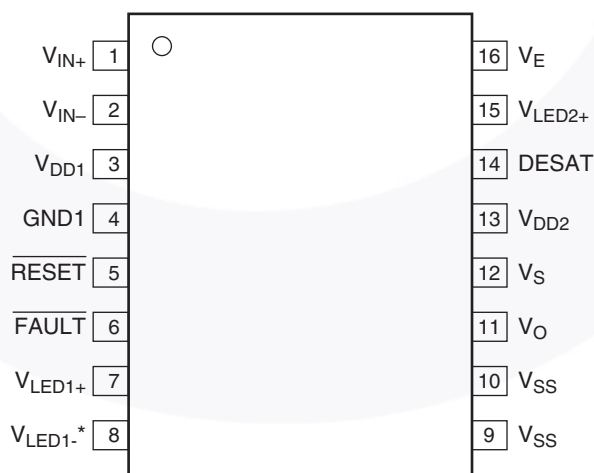


### Truth Table

$V_{IN+}$	$V_{IN-}$	UVLO ( $V_{DD2} - V_E$ )	DESAT Detected?	$\overline{\text{FAULT}}$	$V_O$
X	X	Active	X	X	Low
X	X	X	Yes	Low	Low
Low	X	X	X	X	Low
X	High	X	X	X	Low
High	Low	Not Active	No	High	High

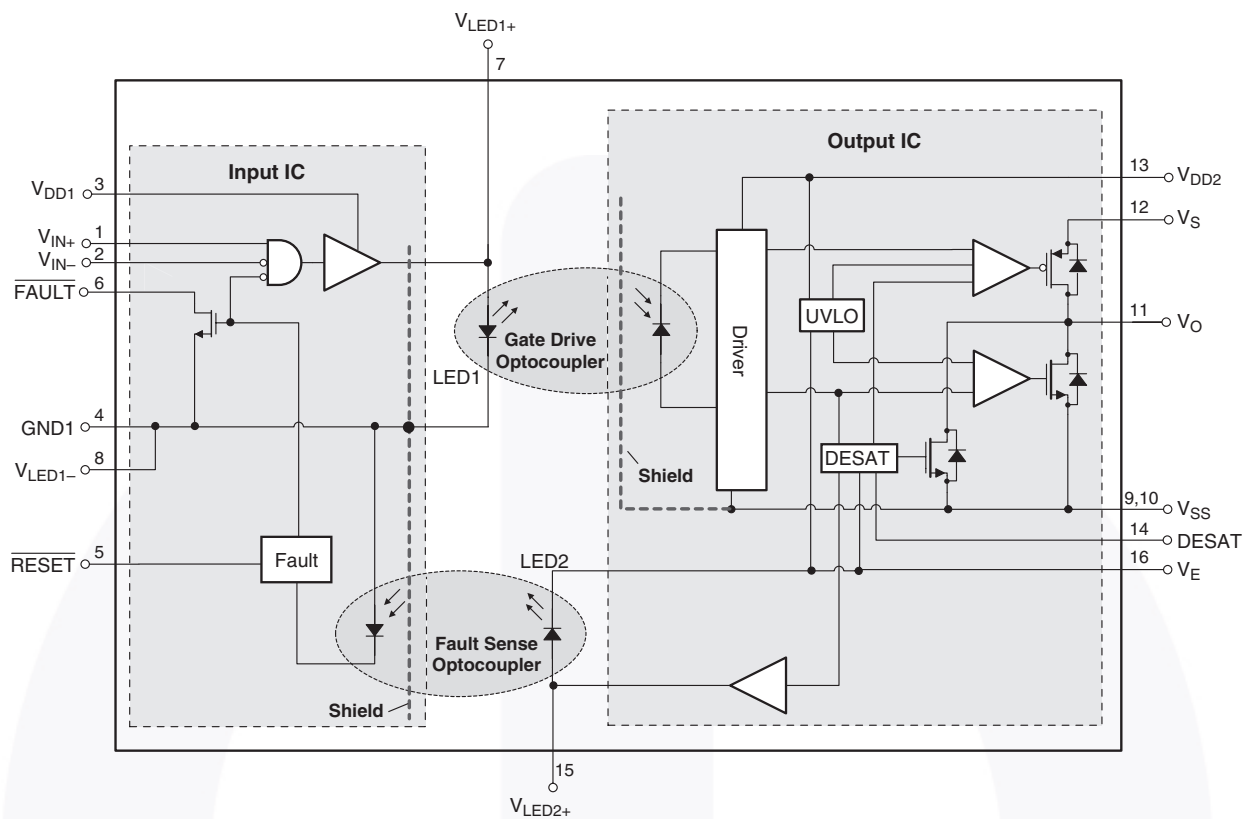
### Pin Definitions

Pin #	Name	Description
1	$V_{IN+}$	Non inverting gate drive control input
2	$V_{IN-}$	Inverting gate drive control input
3	$V_{DD1}$	Positive input supply voltage (3V to 5.5V)
4	GND1	Input ground
5	$\overline{\text{RESET}}$	FAULT reset input
6	$\overline{\text{FAULT}}$	Fault output (open drain)
7	$V_{LED1+}$	LED 1 anode (must be left unconnected)
8	$V_{LED1-}$	LED 1 cathode (must be connected to ground)
9	$V_{SS}$	Output supply voltage (negative)
10	$V_{SS}$	Output supply voltage (negative)
11	$V_O$	Gate drive output voltage
12	$V_S$	Source of pull-up PMOS transistor
13	$V_{DD2}$	Positive output supply voltage
14	DESAT	Desaturation voltage input
15	$V_{LED2+}$	LED 2 anode (must be left unconnected)
16	$V_E$	Output Supply Voltage/IGBT Emitter



\*Pin 8 ( $V_{LED1-}$ ) is internally connected to Pin 4 (GND1).

### Block Diagram



## Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150Vrms		I-IV		
	For Rated Mains Voltage < 300Vrms		I-IV		
	For Rated Mains Voltage < 450Vrms		I-IV		
	For Rated Mains Voltage < 600Vrms		I-IV		
	For Rated Mains Voltage < 1000Vrms		I-III		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V <sub>PR</sub>	Input to Output Test Voltage, Method b, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 sec., Partial Discharge < 5pC	2651			V <sub>peak</sub>
	Input to Output Test Voltage, Method a, V <sub>IORM</sub> × 1.5 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 60 sec., Partial Discharge < 5 pC	2121			V <sub>peak</sub>
V <sub>IORM</sub>	Max Working Insulation Voltage	1,414			V <sub>peak</sub>
V <sub>IOTM</sub>	Highest Allowable Over Voltage	8000			V <sub>peak</sub>
	External Creepage	8			mm
	External Clearance	8			mm
	Insulation Thickness	0.5			mm
T <sub>Case</sub>	Safety Limit Values – Maximum Values Allowed in the Event of a Failure				
	Case Temperature	150			°C
P <sub>S,INPUT</sub>	Input Power	100			mW
P <sub>S,OUTPUT</sub>	Output Power	600			mW
R <sub>IO</sub>	Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500V	10 <sup>9</sup>			Ω

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
$T_{STG}$	Storage Temperature	-40 to +125	$^\circ\text{C}$
$T_{OPR}$	Operating Temperature	-40 to +100	$^\circ\text{C}$
$T_J$	Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_{SOL}$	Lead Wave Solder Temperature (no solder immersion) Refer to page 27 for reflow temperature profile.	260 for 10 sec	$^\circ\text{C}$
$I_{FAULT}$	Fault Output Current	15	mA
$I_{O(PEAK)}$	Peak Output Current <sup>(1)</sup>	3	A
$V_E - V_{SS}$	Negative Output Supply Voltage <sup>(2)</sup>	0 to 15	V
$V_{DD2} - V_E$	Positive Output Supply Voltage	-0.5 to 35 – ( $V_E - V_{SS}$ )	V
$V_{O(peak)}$	Gate Drive Output Voltage	-0.5 to 35	V
$V_{DD2} - V_{SS}$	Output Supply Voltage	-0.5 to 35	V
$V_{DD1}$	Positive Input Supply Voltage	-0.5 to 6	V
$V_{IN+}$ , $V_{IN-}$ and $V_{RESET}$	Input Voltages	-0.5 to $V_{DD1}$	V
$V_{FAULT}$	Fault Pin Voltage	-0.5 to $V_{DD1}$	V
$V_S$	Source of Pull-up PMOS Transistor Voltage	$V_{SS} + 6.5$ to $V_{DD2}$	V
$V_{DESAT}$	DESAT Voltage	$V_E$ to $V_E + 11$	V
$PD_I$	Input Power Dissipation <sup>(3)(5)</sup>	100	mW
$PD_O$	Output Power Dissipation <sup>(4)(5)</sup>	600	mW

**Notes:**

- Maximum pulse width = 10 $\mu\text{s}$ , maximum duty cycle = 0.2%.
- This negative output supply voltage is optional. It's only needed when negative gate drive is implemented. Refer to "Dual Supply Operation – Negative Bias at  $V_{SS}$ " on page 23.
- No derating required across temperature range.
- Derate linearly above 64 $^\circ\text{C}$ , free air temperature at a rate of 10.2mW/ $^\circ\text{C}$
- Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

**Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$T_A$	Ambient Operating Temperature	-40	+100	$^\circ\text{C}$
$V_{DD1}$	Input Supply Voltage <sup>(6)</sup>	3	5.5	V
$V_{DD2} - V_{SS}$	Total Output Supply Voltage	15	30	V
$V_E - V_{SS}$	Negative Output Supply Voltage	0	15	V
$V_{DD2} - V_E$	Positive Output Supply Voltage <sup>(6)</sup>	15	30 – ( $V_E - V_{SS}$ )	V
$V_S$	Source of Pull-up PMOS Transistor Voltage	$V_{SS} + 7.5$	$V_{DD2}$	V

**Note:**

- During power up or down, it is important to ensure that  $V_{IN+}$  remains low until both the input and output supply voltages reaches the proper recommended operating voltages to avoid any momentary instability at the output state. See also the discussion in the "Time to Good Power" section on page 23.

## Isolation Characteristics

Apply over all recommended conditions, typical value is measured at  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ISO}$	Input-Output Isolation Voltage	$T_A = 25^\circ\text{C}$ , R.H. < 50%, $t = 1.0\text{min}$ , $I_{I-O} \leq 10\mu\text{A}$ , 50Hz <sup>(7)(8)(9)</sup>	4,243			$V_{RMS}$
$R_{ISO}$	Isolation Resistance	$V_{I-O} = 500V^{(7)}$		$10^{11}$		$\Omega$
$C_{ISO}$	Isolation Capacitance	$V_{I-O} = 0V$ , Freq = 1.0MHz <sup>(7)</sup>		1		pF

### Notes:

- Device is considered a two terminal device: Pins 1 to 8 are shorted together and Pins 9 to 16 are shorted together.
- 4,243 VRMS for 1 minute duration is equivalent to 5,091 VRMS for 1 second duration.
- The Input-Output Isolation Voltage is a dielectric voltage rating as per UL1577. It should not be regarded as an input-output continuous voltage rating. For the continuous working voltage rating refer to your equipment level safety specification or DIN EN/IEC 60747-5-5 Safety and Insulation Ratings Table.

## Electrical Characteristics

Apply over all recommended conditions, typical value is measured at  $V_{DD1} = 5V$ ,  $V_{DD2} - V_{SS} = 30V$ ,  $V_E - V_{SS} = 0V$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
$V_{IN+L}, V_{IN-L}, V_{RESETL}$	Logic Low Input Voltages				0.8	V	
$V_{IN+H}, V_{IN-H}, V_{RESETH}$	Logic High Input Voltages		2.0			V	
$I_{IN+L}, I_{IN-L}, I_{RESETL}$	Logic Low Input Currents	$V_{IN} = 0.4V$	-0.5	-0.001		mA	
$I_{FAULTL}$	$\overline{\text{FAULT}}$ Logic Low Output Current	$V_{FAULT} = 0.4V$	5.0	12.0		mA	1, 32
$I_{FAULTH}$	$\overline{\text{FAULT}}$ Logic High Output Current	$V_{FAULT} = V_{DD1}$	-40	0.002		$\mu\text{A}$	32
$I_{OH}$	High Level Output Current	$V_O = V_{DD2} - 3V$	-1	-3		A	2, 7, 33
		$V_O = V_{DD2} - 6V^{(10)}$	-2.5			A	
$I_{OL}$	Low Level Output Current	$V_O = V_{SS} + 3V$	1	3		A	3, 34
		$V_O = V_{SS} + 6V^{(11)}$	2.5			A	
$I_{OLF}$	Low Level Output Current During Fault Condition	$V_O - V_{SS} = 14V$	90	185	230	mA	4, 38
$V_{OH}$	High Level Output Voltage	$I_O = -100\text{mA}^{(12)(13)(14)}$	$V_S - 1.0V$	$V_S - 0.5V$		V	5, 7, 35
$V_{OL}$	Low Level Output Voltage	$I_O = 100\text{mA}$		0.1	0.5	V	6, 8, 35
$I_{DD1H}$	High Level Supply Current	$V_{IN+} = V_{DD1} = 5.5V$ , $V_{IN-} = 0V$		14	17	mA	9, 36
$I_{DD1L}$	Low Level Supply Current	$V_{IN+} = V_{IN-} = 0V$ , $V_{DD1} = 5.5V$		2	3	mA	
$I_{DD2H}$	High Level Output Supply Current	$V_O = \text{Open}^{(14)}$		1	3	mA	10, 11, 37
$I_{DD2L}$	Low Level Output Supply Current	$V_O = \text{Open}$		0.8	2.8	mA	
$I_{SH}$	High Level Source Current	$I_O = 0\text{mA}$		0.65	1.5	mA	37
$I_{SL}$	Low Level Source Current	$I_O = 0\text{mA}$		0.6	1.4	mA	37
$I_{EL}$	$V_E$ Low Level Supply Current		-0.5	-0.2		mA	13, 37
$I_{EH}$	$V_E$ High Level Supply Current		-0.5	-0.25		mA	
$I_{CHG}$	Blanking Capacitor Charge Current	$V_{DESAT} = 2V^{(14)(15)}$	-0.13	-0.25	-0.37	mA	12, 38
$I_{DSCHG}$	Blanking Capacitor Discharge Current	$V_{DESAT} = 7V$	10	36		mA	38

### Electrical Characteristics (Continued)

Apply over all recommended conditions, typical value is measured at  $V_{DD1} = 5V$ ,  $V_{DD2} - V_{SS} = 30V$ ,  $V_E - V_{SS} = 0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
$V_{UVLO+}$	Under Voltage Lockout Threshold <sup>(14)</sup>	$V_O > 5V @ 25^\circ C$		11.5	13.5	V	15, 29, 39
$V_{UVLO-}$		$V_O < 5V @ 25^\circ C$	9	10		V	
$UVLO_{HYS}$	Under Voltage Lockout Threshold Hysteresis	@ $25^\circ C$	0.4	1.5		V	
$V_{DESAT}$	DESAT Threshold <sup>(14)</sup>	$V_{DD2} - V_E > V_{UVLO-}$ , $V_O < 5V$	6.0	7.0	9.0	V	16, 38

#### Notes:

10. Maximum pulse width = 10 $\mu$ s, maximum duty cycle = 0.2%.
11. Maximum pulse width = 4.99ms, maximum duty cycle = 99.8%.
12.  $V_{OH}$  is measured with the DC load current in this testing (Maximum pulse width = 1ms, Maximum duty cycle = 20%). When driving capacitive loads,  $V_{OH}$  will approach  $V_{DD}$  as  $I_{OH}$  approaches zero units.
13. Positive Output supply voltage ( $V_{DD2} - V_E$ ) should be at least 15V. This is to ensure adequate margin in excess of the maximum Under Voltage Lockout Threshold  $V_{UVLO+}$  of 13.5V.
14. When  $V_{DD2} - V_E > V_{UVLO}$  and output state  $V_O$  of the FOD8316 is allowed to go high, the DESAT detection feature will be active and will provide the primary source of IGBT protection. UVLO is needed to ensure DESAT detection is functional.
15. The blanking time,  $t_{BLANK}$  is adjustable by an external capacitor ( $C_{BLANK}$ ) where  $t_{BLANK} = C_{BLANK} * (V_{DESAT}/I_{CHG})$

### Switching Characteristics

Apply over all recommended conditions, typical value is measured at  $V_{DD1} = 5V$ ,  $V_{DD2} - V_{SS} = 30V$ ,  $V_E - V_{SS} = 0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure	
$t_{PHL}$	Propagation Delay Time to Logic Low Output <sup>(17)</sup>	$R_g = 10\Omega$ , $C_g = 10nF$ , $f = 10kHz$ , Duty Cycle = 50% <sup>(16)</sup>		300	500	ns	17, 18, 19, 20, 21, 22, 40, 48	
$t_{PLH}$	Propagation Delay Time to Logic High Output <sup>(18)</sup>			250	500	ns		
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $ <sup>(19)</sup>				50	300		ns
PDD Skew	Propagation Delay Difference Between Any Two Parts or Channels, $(t_{PHL} - t_{PLH})$ <sup>(20)</sup>		-350		350	ns		
$t_R$	Output Rise Time (10% – 90%)			34		ns	40, 48	
$t_F$	Output Fall Time (90% – 10%)			34		ns		
$t_{DESAT(90\%)}$	DESAT Sense to 90% $V_O$ Delay <sup>(21)</sup>	$R_g = 10\Omega$ , $C_g = 10nF$ , $V_{DD2} - V_{SS} = 30V$		850		ns	23, 41	
$t_{DESAT(10\%)}$	DESAT Sense to 10% $V_O$ Delay <sup>(21)</sup>			2	3	$\mu$ s		24, 26, 27, 41
$t_{DESAT(\overline{FAULT})}$	DESAT Sense to Low Level $\overline{FAULT}$ Signal Delay <sup>(22)</sup>				1.8	5	$\mu$ s	25, 41, 49
$t_{DESAT(LOW)}$	DESAT Sense to DESAT Low Propagation Delay <sup>(23)</sup>				850		ns	41
$t_{RESET(\overline{FAULT})}$	$\overline{RESET}$ to High Level $\overline{FAULT}$ Signal Delay <sup>(24)</sup>			3	6	20	$\mu$ s	28, 42, 49
$PW_{\overline{RESET}}$	$\overline{RESET}$ Signal Pulse Width			1.2			$\mu$ s	
$t_{UVLO ON}$	UVLO Turn On Delay <sup>(25)</sup>		$V_{DD2} = 20V$ in 1.0ms Ramp		4		$\mu$ s	29, 43
$t_{UVLO OFF}$	UVLO Turn Off Delay <sup>(26)</sup>				3		$\mu$ s	

### Switching Characteristics (Continued)

Apply over all recommended conditions, typical value is measured at  $V_{DD1} = 5V$ ,  $V_{DD2} - V_{SS} = 30V$ ,  $V_E - V_{SS} = 0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
$t_{GP}$	Time to Good Power <sup>(27)</sup>	$V_{DD2} = 0$ to $30V$ in $10\mu s$ Ramp		30		$\mu s$	30, 31, 43
$ CM_H $	Common Mode Transient Immunity at Output High	$T_A = 25^\circ C$ , $V_{DD1} = 5V$ , $V_{DD2} = 25V$ , $V_{SS} = \text{Ground}$ , $V_{CM} = 1500V_{pk}$ <sup>(28)</sup>	35	50		$kV/\mu s$	45, 46
$ CM_L $	Common Mode Transient Immunity at Output Low	$T_A = 25^\circ C$ , $V_{DD1} = 5V$ , $V_{DD2} = 25V$ , $V_{SS} = \text{Ground}$ , $V_{CM} = 1500V_{pk}$ <sup>(29)</sup>	35	50		$kV/\mu s$	44, 47

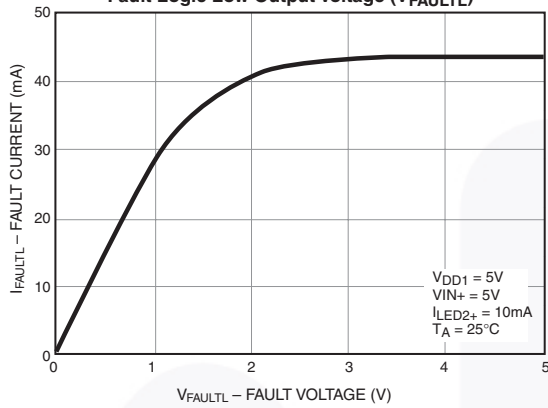
#### Notes:

16. This load condition approximates the gate load of a 1200 V/150A IGBT.
17.  $t_{PHL}$  propagation delay is measured from the 50% level on the falling edge of the input pulse ( $V_{IN+}$ ,  $V_{IN-}$ ) to the 50% level of the falling edge of the  $V_O$  signal. Refer to Figure 48.
18.  $t_{PHL}$  propagation delay is measured from the 50% level on the rising edge of the input pulse ( $V_{IN+}$ ,  $V_{IN-}$ ) to the 50% level of the rising edge of the  $V_O$  signal. Refer to Figure 48.
19. PWD is defined as  $|t_{PHL} - t_{PLH}|$  for any given device.
20. The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two FOD8316 parts under same operating conditions, with equal loads.
21. This is the amount of time the DESAT threshold must be exceeded before  $V_O$  begins to go low. This is supply voltage dependent. See Figure 49.
22. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low. See Figure 49.
23. This is the amount of time the DESAT threshold must be exceeded before  $V_O$  begins to go low, and the FAULT output to go low. See Figure 49.
24. This is the amount of time from when RESET is asserted low, until FAULT output goes high. See Figure 49.
25.  $t_{UVLO\ ON}$  UVLO Turn On Delay is measured from  $V_{UVLO+}$  threshold voltage of the output supply voltage ( $V_{DD2}$ ) to the 5V level of the rising edge of the  $V_O$  signal.
26.  $t_{UVLO\ OFF}$  UVLO Turn Off Delay is measured from  $V_{UVLO-}$  threshold voltage of the output supply voltage ( $V_{DD2}$ ) to the 5V level of the falling edge of the  $V_O$  signal.
27.  $t_{GP}$  Time to Good Power is measured from 13.5V level of the rising edge of the output supply voltage ( $V_{DD2}$ ) to the 5V level of the rising edge of the  $V_O$  signal.
28. Common mode transient immunity at output high state is the maximum tolerable negative  $dV_{CM}/dt$  on the trailing edge of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in the high state (i.e.,  $V_O > 15V$  or  $FAULT > 2V$ ).
29. Common mode transient immunity at output low state is the maximum positive tolerable  $dV_{CM}/dt$  on the leading edge of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (i.e.,  $V_O < 1.0V$  or  $FAULT < 0.8V$ ).

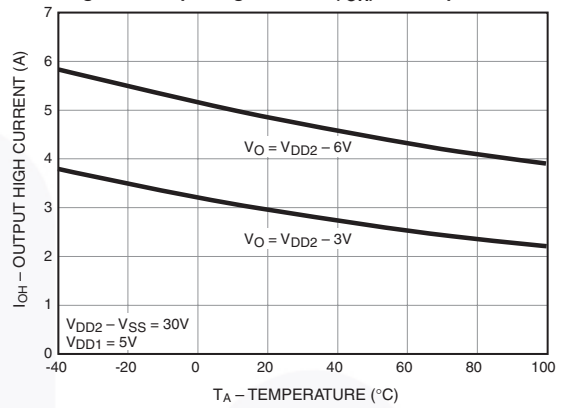


## Typical Performance Characteristics

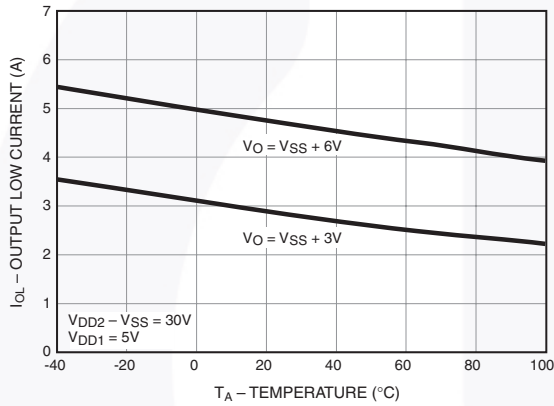
**Figure 1. Fault Logic Low Output Current ( $I_{FAULTL}$ ) vs. Fault Logic Low Output Voltage ( $V_{FAULTL}$ )**



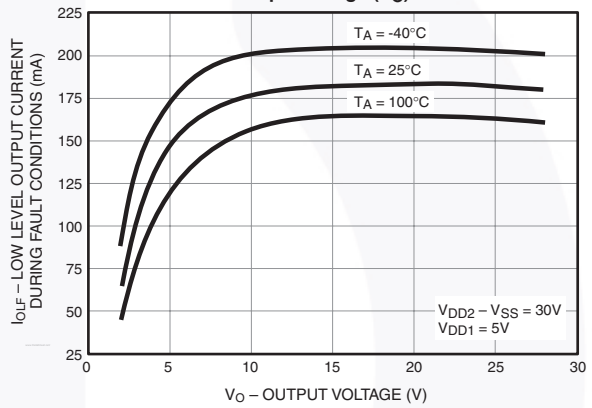
**Figure 2. Output High Current ( $I_{OH}$ ) vs. Temperature**



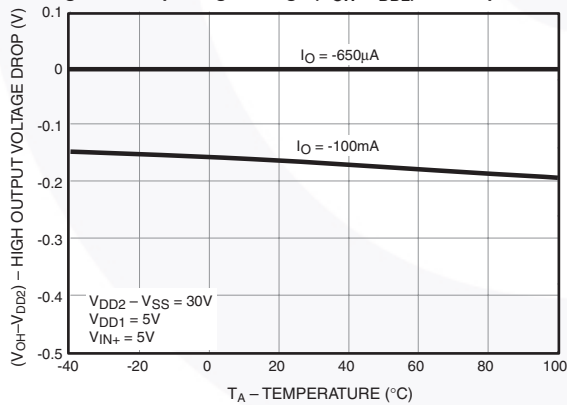
**Figure 3. Output Low Current ( $I_{OL}$ ) vs. Temperature**



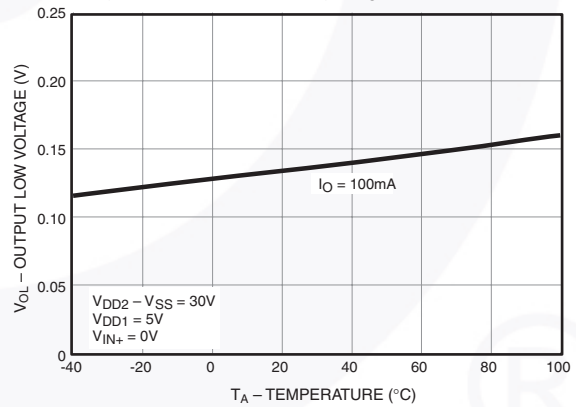
**Figure 4. Low Level Output Current ( $I_{OLF}$ ) vs. Output Voltage ( $V_O$ )**



**Figure 5. Output High Voltage ( $V_{OH} - V_{DD2}$ ) vs. Temperature**

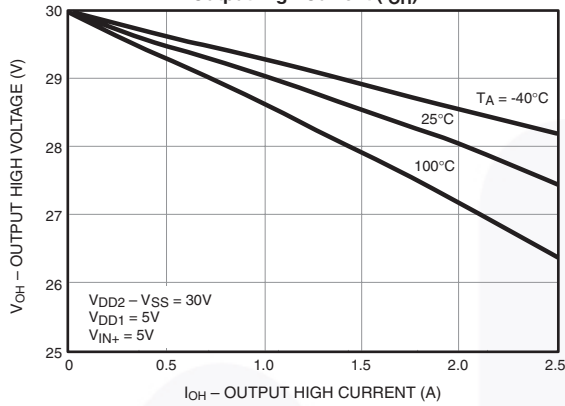


**Figure 6. Output Low Voltage ( $V_{OL}$ ) vs. Temperature**

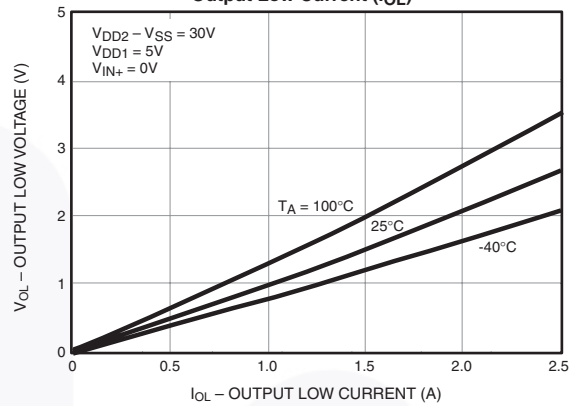


## Typical Performance Characteristics (Continued)

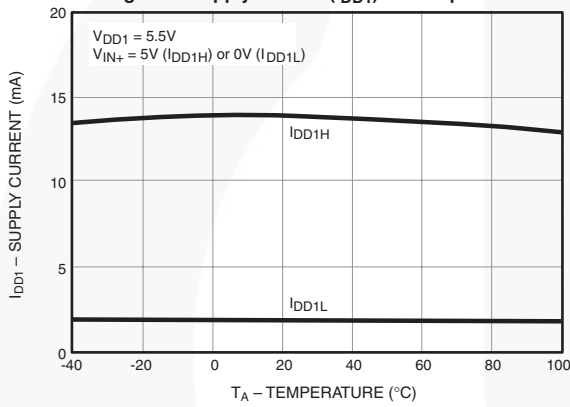
**Figure 7. Output High Voltage ( $V_{OH}$ ) vs. Output High Current ( $I_{OH}$ )**



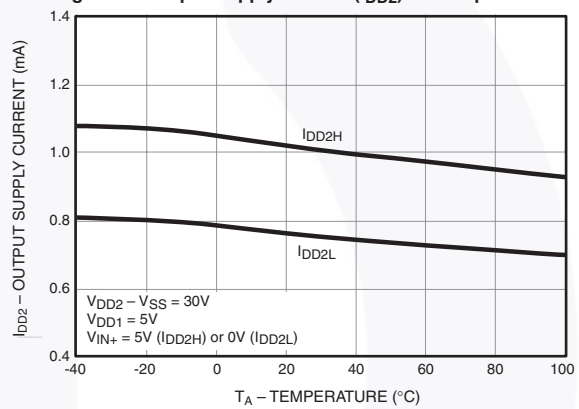
**Figure 8. Output Low Voltage ( $V_{OL}$ ) vs. Output Low Current ( $I_{OL}$ )**



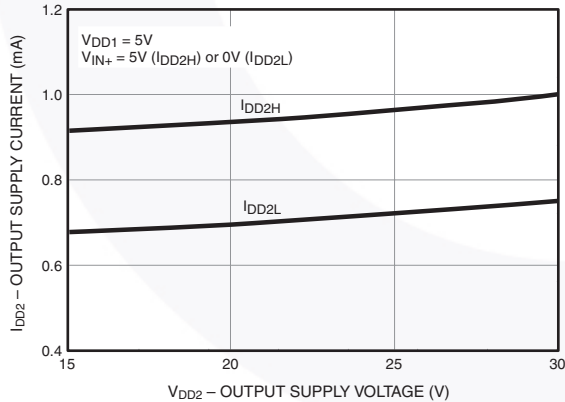
**Figure 9. Supply Current ( $I_{DD1}$ ) vs. Temperature**



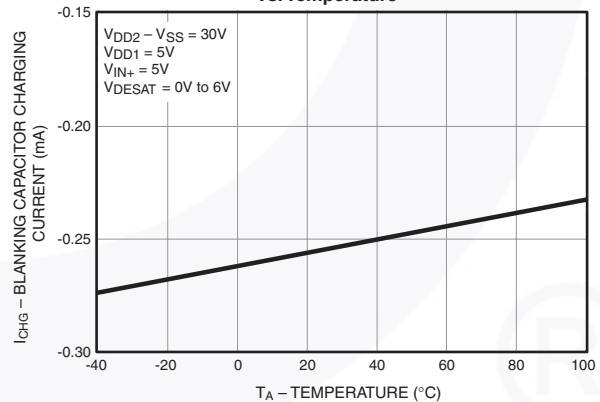
**Figure 10. Output Supply Current ( $I_{DD2}$ ) vs. Temperature**



**Figure 11. Output Supply Current ( $I_{DD2}$ ) vs. Output Supply Voltage ( $V_{DD2}$ )**

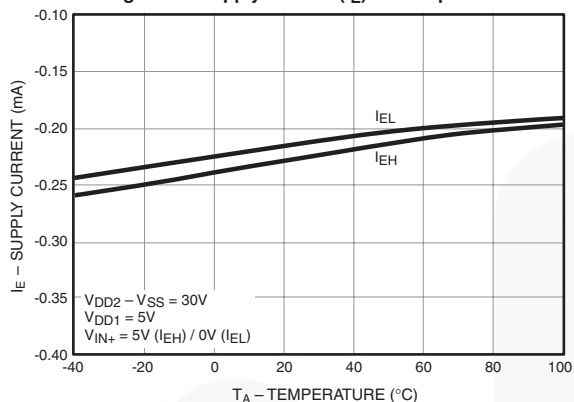


**Figure 12. Blanking Capacitor Charging Current ( $I_{CHG}$ ) vs. Temperature**

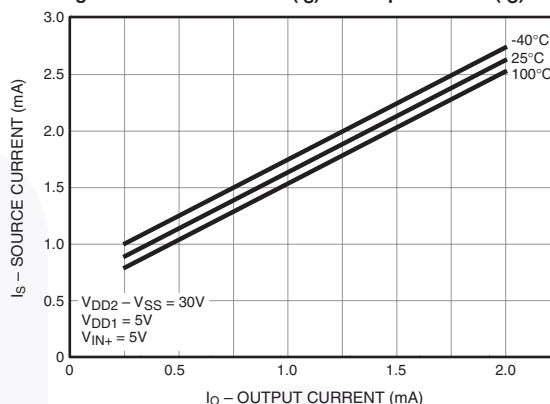


## Typical Performance Characteristics (Continued)

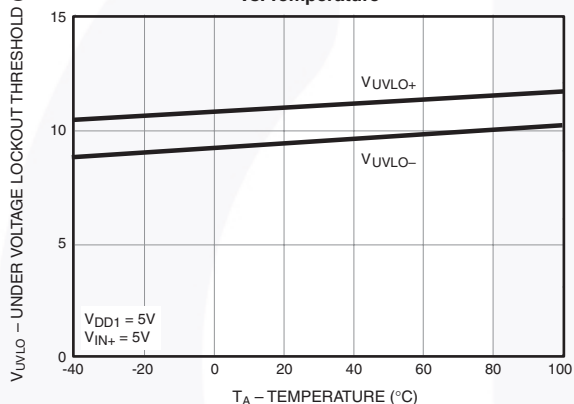
**Figure 13. Supply Current ( $I_E$ ) vs. Temperature**



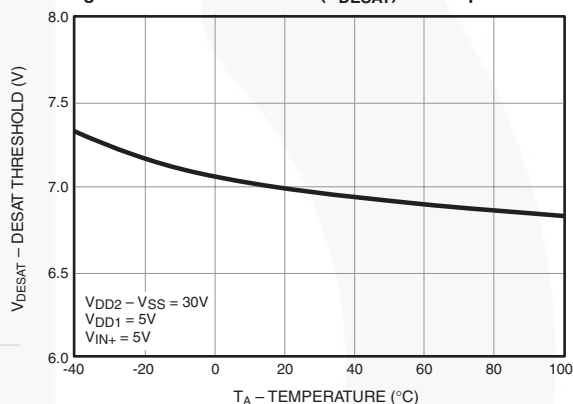
**Figure 14. Source Current ( $I_S$ ) vs. Output Current ( $I_O$ )**



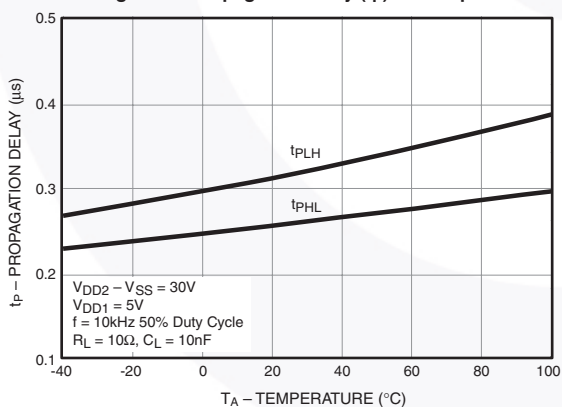
**Figure 15. Under Voltage Lockout Threshold ( $V_{UVLO}$ ) vs. Temperature**



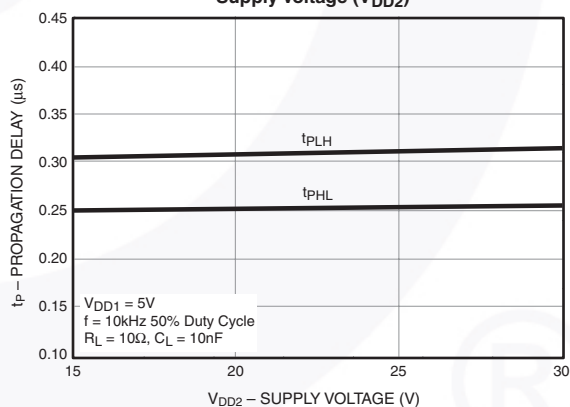
**Figure 16. DESAT Threshold ( $V_{DESAT}$ ) vs. Temperature**



**Figure 17. Propagation Delay ( $t_p$ ) vs. Temperature**

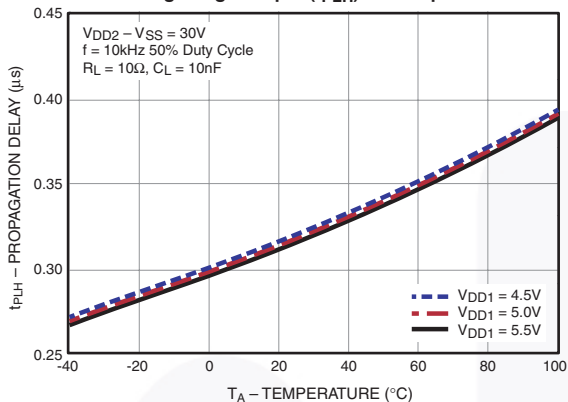


**Figure 18. Propagation Delay ( $t_p$ ) vs. Supply Voltage ( $V_{DD2}$ )**

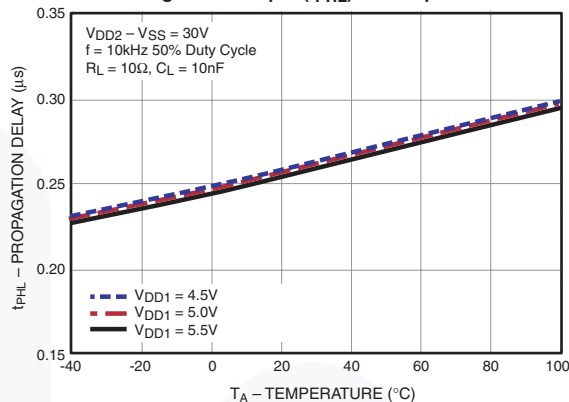


## Typical Performance Characteristics (Continued)

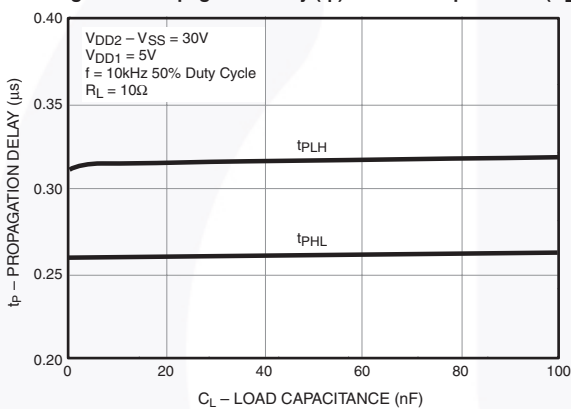
**Figure 19. Propagation Delay Time to Logic High Output ( $t_{PLH}$ ) vs. Temperature**



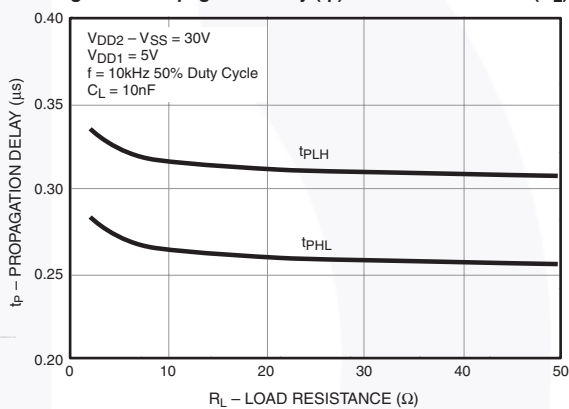
**Figure 20. Propagation Delay Time to Logic Low Output ( $t_{PHL}$ ) vs. Temperature**



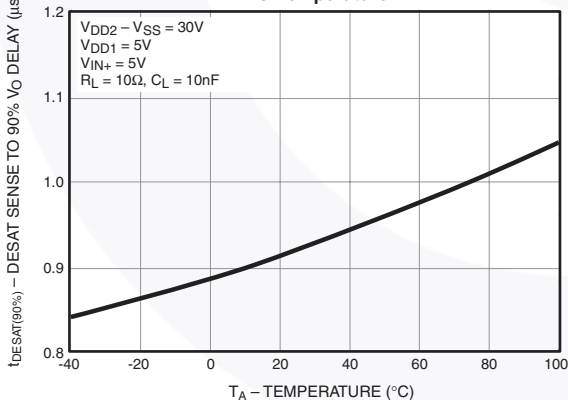
**Figure 21. Propagation Delay ( $t_p$ ) vs. Load Capacitance ( $C_L$ )**



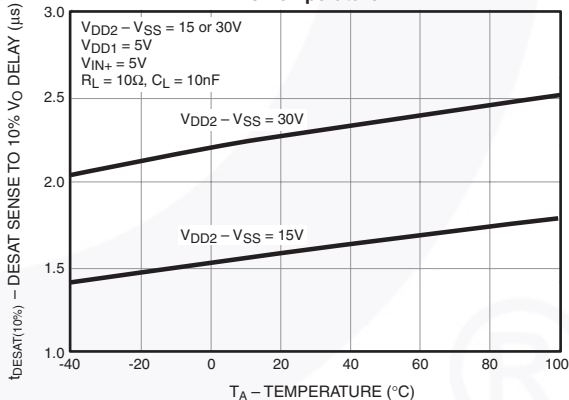
**Figure 22. Propagation Delay ( $t_p$ ) vs. Load Resistance ( $R_L$ )**



**Figure 23. DESAT Sense to 90%  $V_O$  ( $t_{DESAT(90\%)}$ ) vs. Temperature**

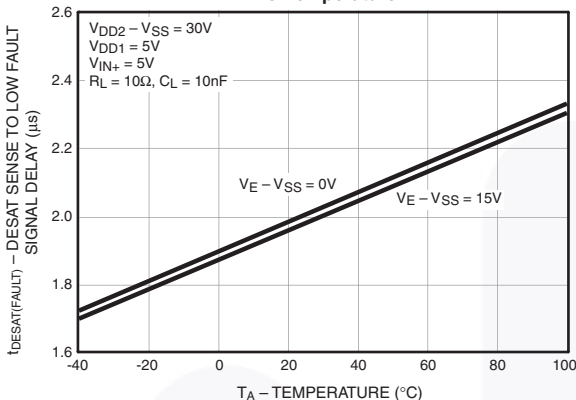


**Figure 24. DESAT Sense to 10%  $V_O$  Delay ( $t_{DESAT(10\%)}$ ) vs. Temperature**

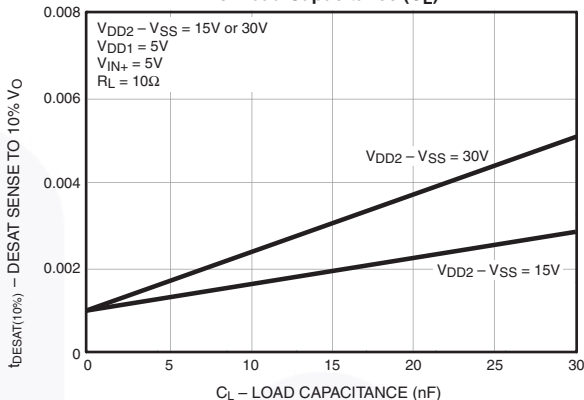


## Typical Performance Characteristics (Continued)

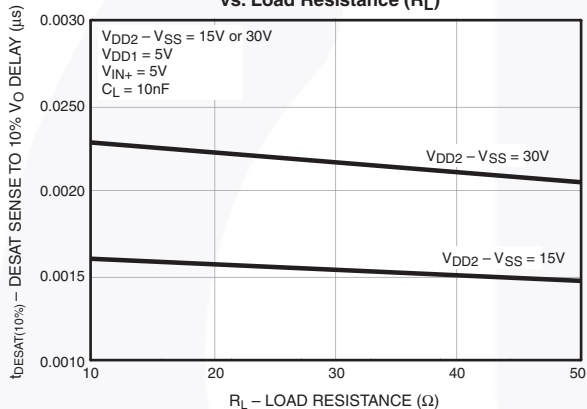
**Figure 25. DESAT Sense to Low Fault Signal Delay ( $t_{DESAT(FAULT)}$ ) vs. Temperature**



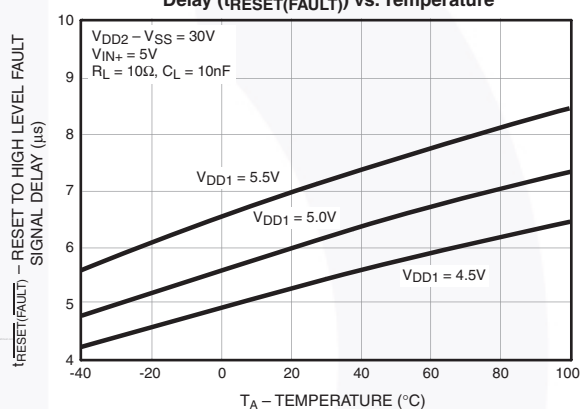
**Figure 26. DESAT Sense to 10%  $V_O$  Delay ( $t_{DESAT(10\%)}$ ) vs. Load Capacitance ( $C_L$ )**



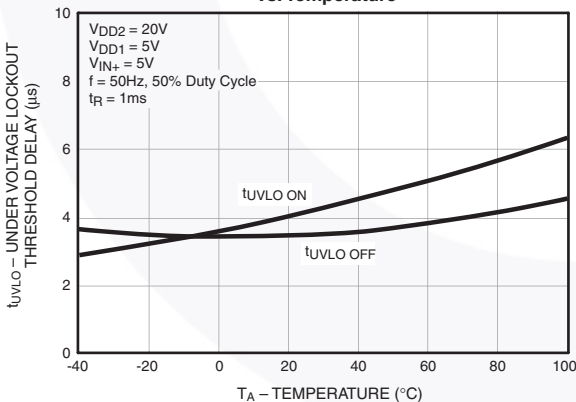
**Figure 27. DESAT Sense to 10%  $V_O$  Delay ( $t_{DESAT(10\%)}$ ) vs. Load Resistance ( $R_L$ )**



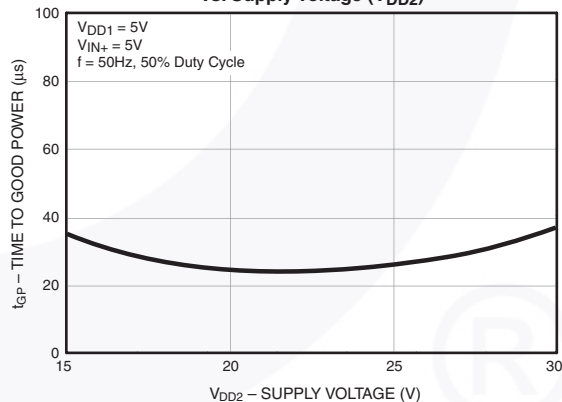
**Figure 28. RESET to High Level FAULT Signal Delay ( $t_{RESET(FAULT)}$ ) vs. Temperature**



**Figure 29. Under Voltage Lockout Threshold Delay ( $t_{UVLO}$ ) vs. Temperature**

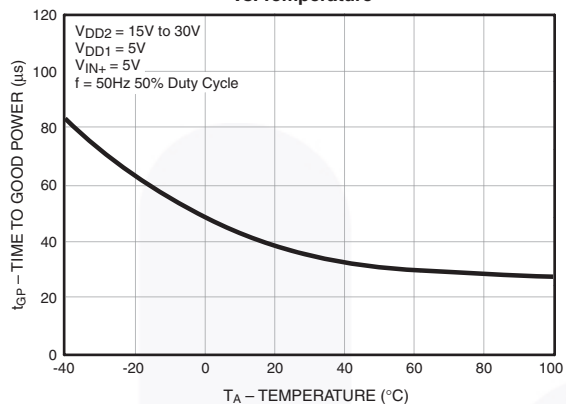


**Figure 30. Time to Good Power ( $t_{GP}$ ) vs. Supply Voltage ( $V_{DD2}$ )**

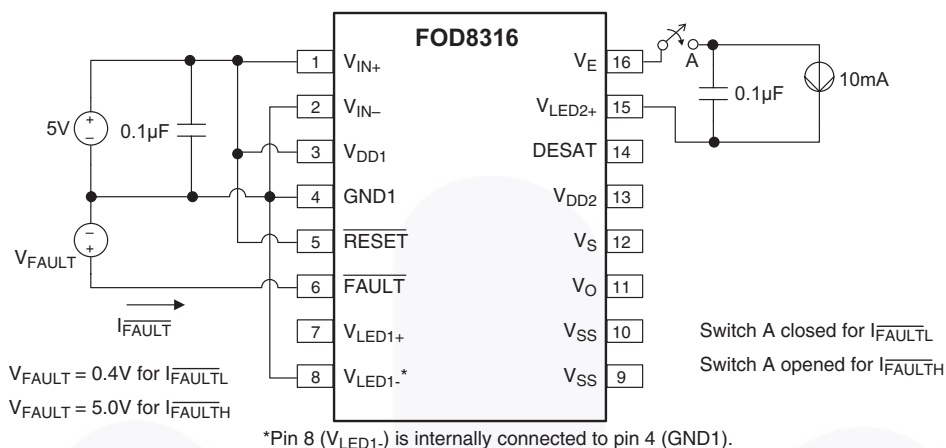


### Typical Performance Characteristics (Continued)

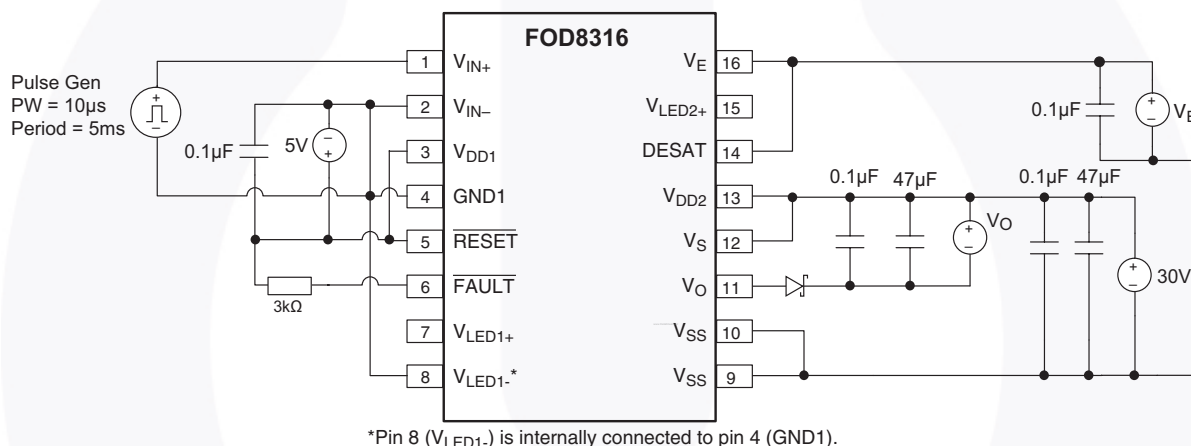
Figure 31. Time to Good Power ( $t_{GP}$ ) vs. Temperature



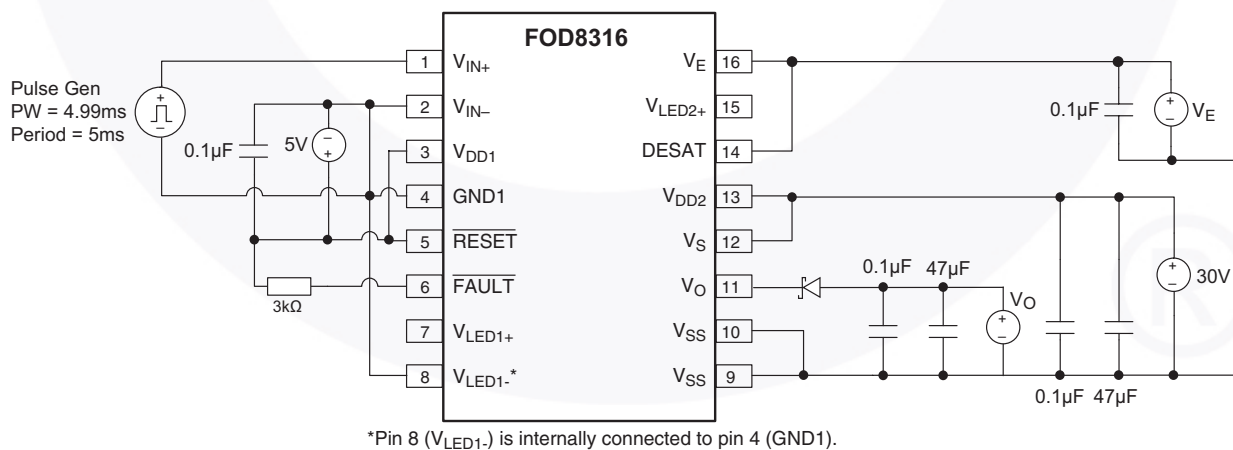
### Test Circuits



**Figure 32. Fault Output Current ( $I_{FAULTL}$ ) and ( $I_{FAULTH}$ ) Test Circuit**

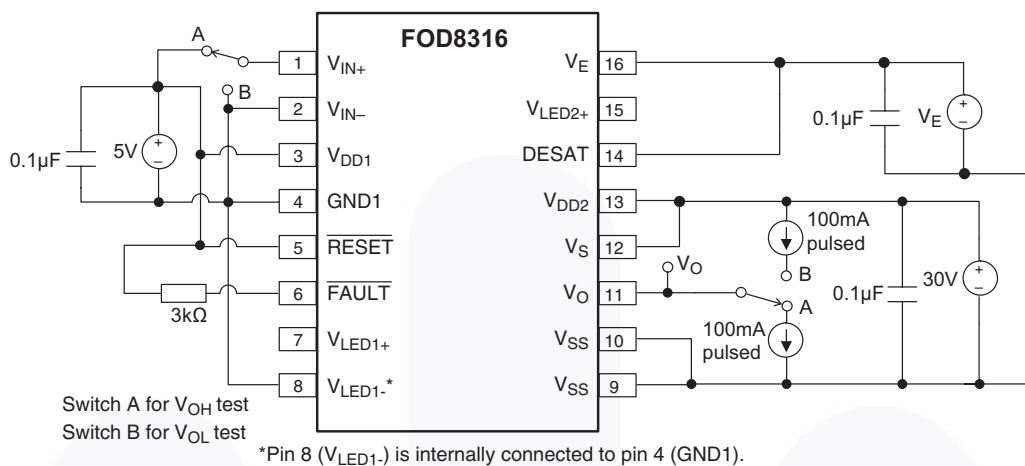


**Figure 33. High Level Output Current ( $I_{OH}$ ) Test Circuit**

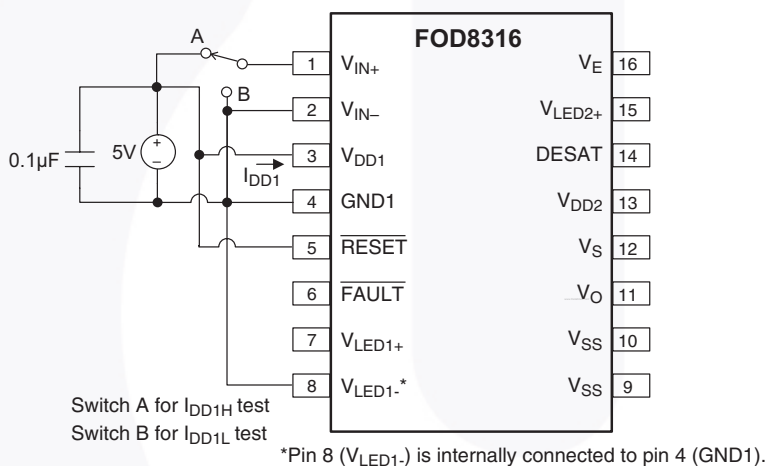


**Figure 34. Low Level Output Current ( $I_{OL}$ ) Test Circuit**

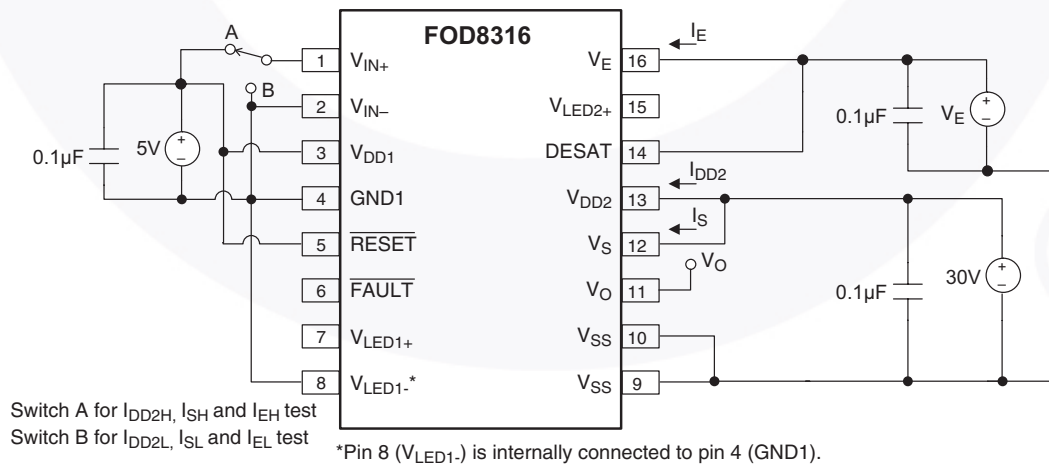
**Test Circuits** (Continued)



**Figure 35. High Level ( $V_{OH}$ ) and Low Level ( $V_{OL}$ ) Output Voltage Test Circuit**



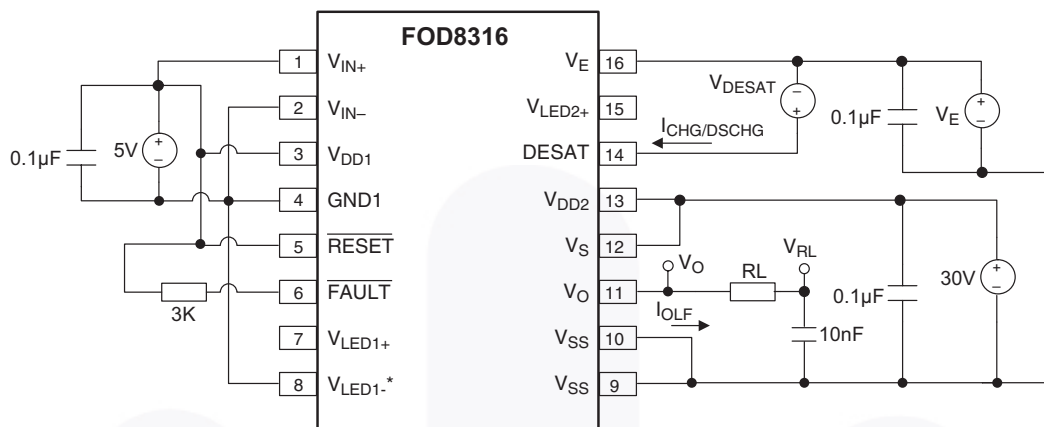
**Figure 36. High Level ( $I_{DD1H}$ ) and Low Level ( $I_{DD1L}$ ) Supply Current Test Circuit**



**Figure 37. High Level ( $I_{DD2H}$ ), Low Level ( $I_{DD2L}$ ) Output Supply Current, High Level ( $I_{SH}$ ), Low Level ( $I_{SL}$ ) Source Current,  $V_E$  High Level ( $I_{EH}$ ), and  $V_E$  Low Level ( $I_{EL}$ ) Supply Current Test Circuit**

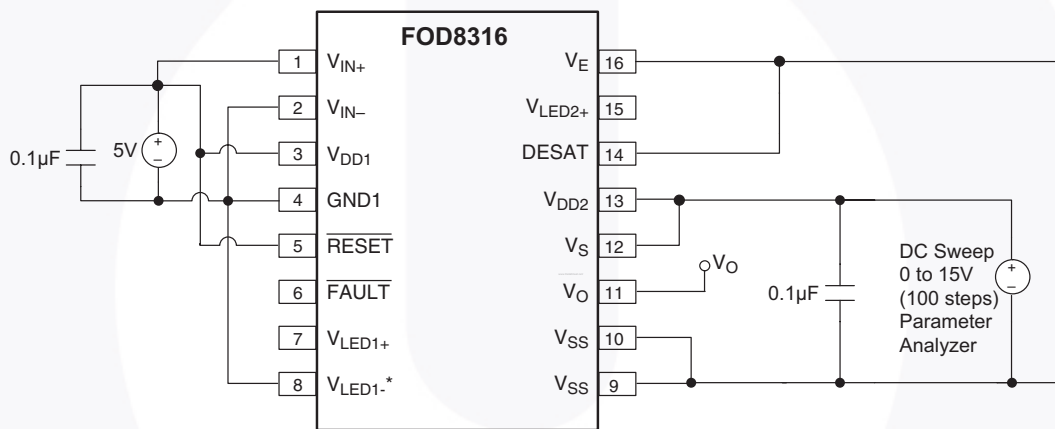


**Test Circuits** (Continued)



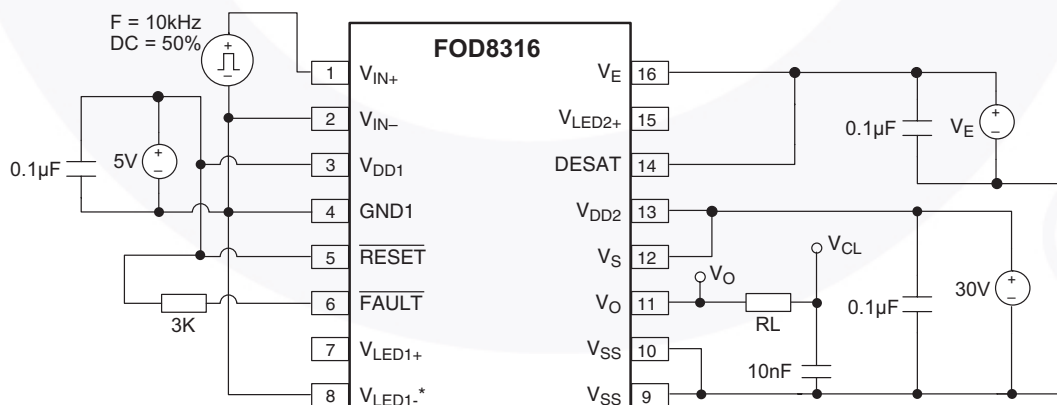
\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

**Figure 38. Low Level Output Current During Fault Conditions ( $I_{OLF}$ ), Blanking Capacitor Charge Current ( $I_{CHG}$ ), Blanking Capacitor Discharging Current ( $I_{DSCHG}$ ) and DESAT Threshold ( $V_{DESAT}$ ) Test Circuit**



\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

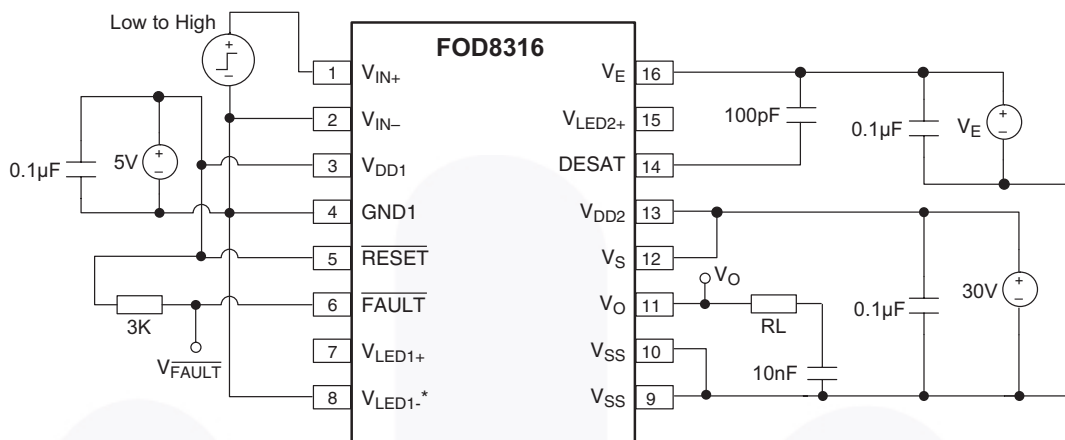
**Figure 39. Under Voltage Lockout Threshold ( $V_{UVLO}$ ) Test Circuit**



\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

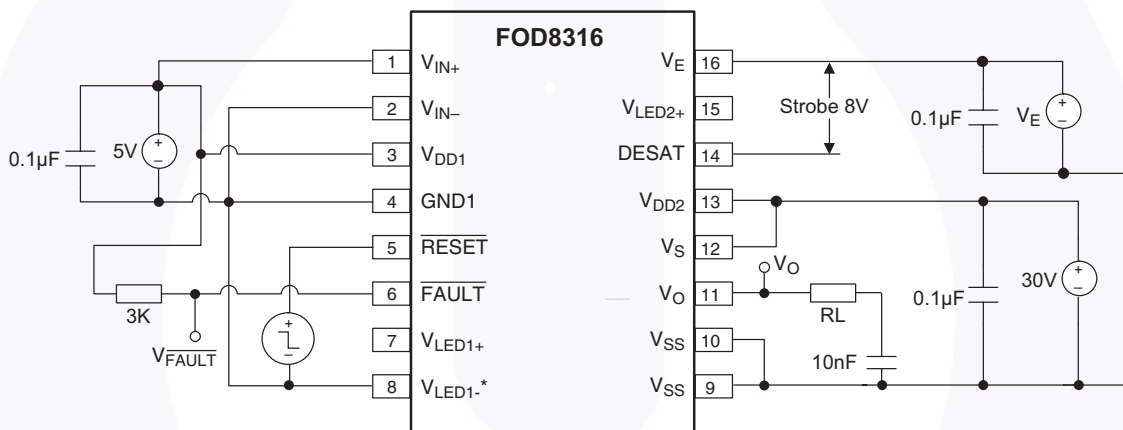
**Figure 40. Propagation Delay ( $t_{PLH}$ ,  $t_{PHL}$ ), Pulse Width Distortion (PWD), Rise Time ( $t_R$ ) and Fall Time ( $t_F$ ) Test Circuit**

**Test Circuits** (Continued)



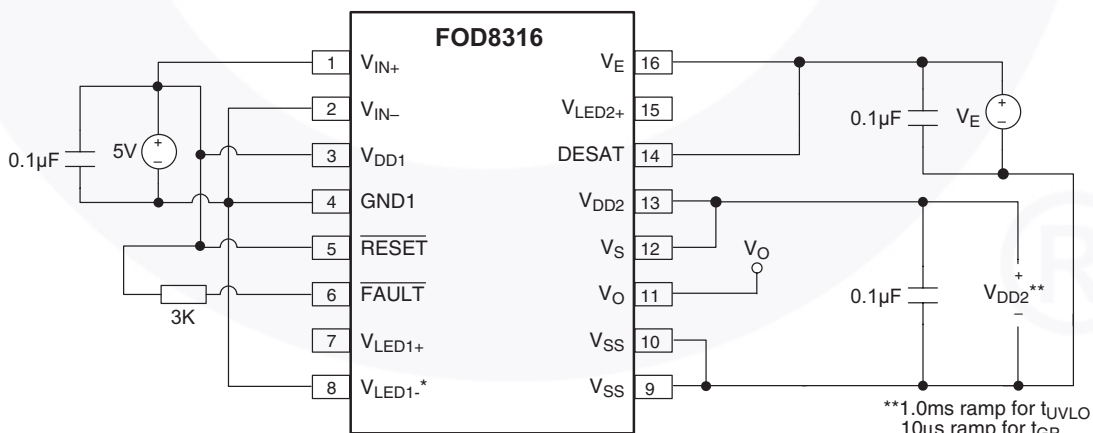
\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

**Figure 41. DESAT Sense ( $t_{DESAT(90\%)}$ ,  $t_{DESAT(10\%)}$ ), DESAT Fault ( $t_{DESAT(\overline{FAULT})}$ ), and ( $t_{DESAT(LOW)}$ ) Test Circuit**



\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

**Figure 42. Reset Delay ( $t_{RESET(\overline{FAULT})}$ ) Test Circuit**

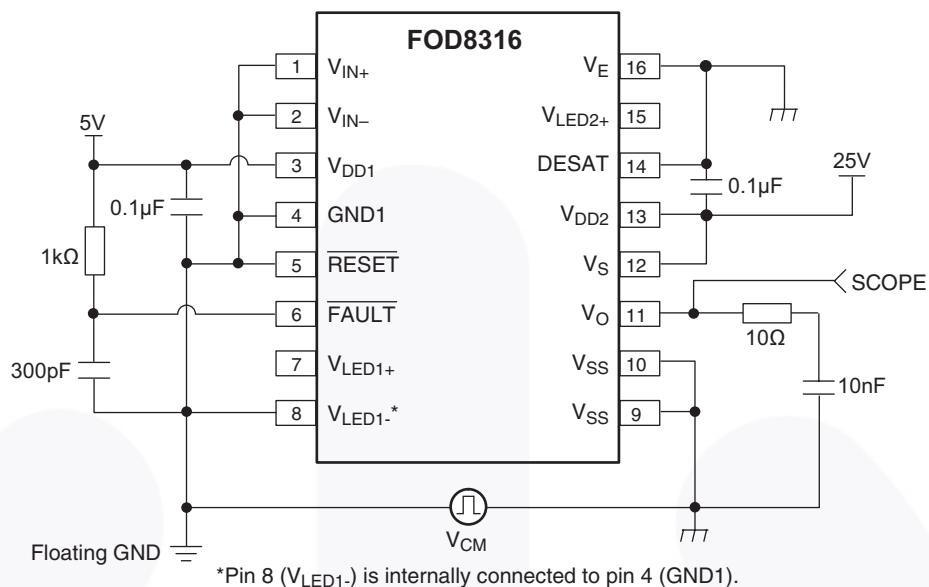


\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

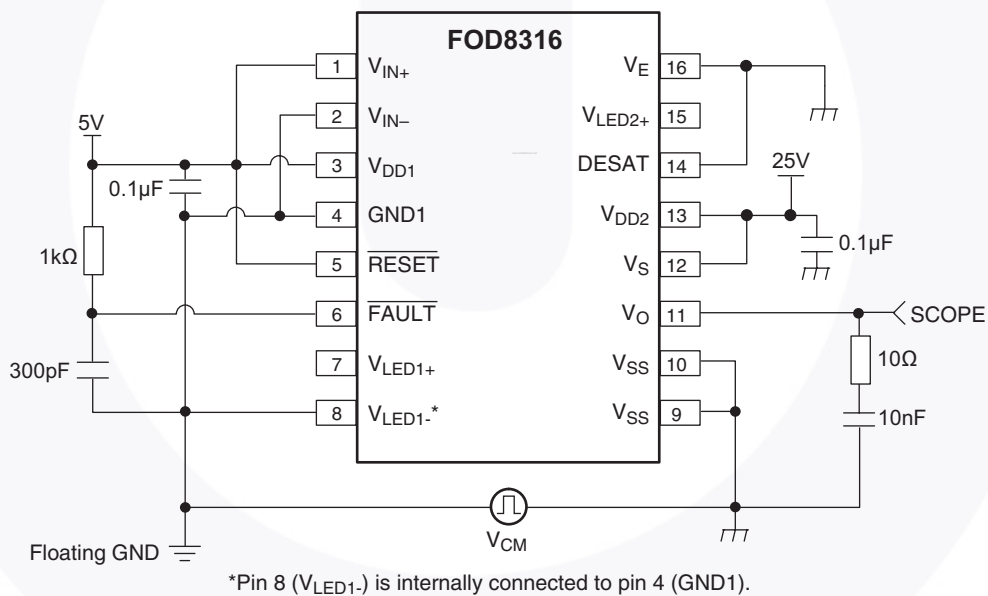
\*\*1.0ms ramp for  $t_{UVLO}$   
10µs ramp for  $t_{GP}$

**Figure 43. Under Voltage Lockout Delay ( $t_{UVLO}$ ) and Time to Good Power ( $t_{GP}$ ) Test Circuit**

**Test Circuits** (Continued)

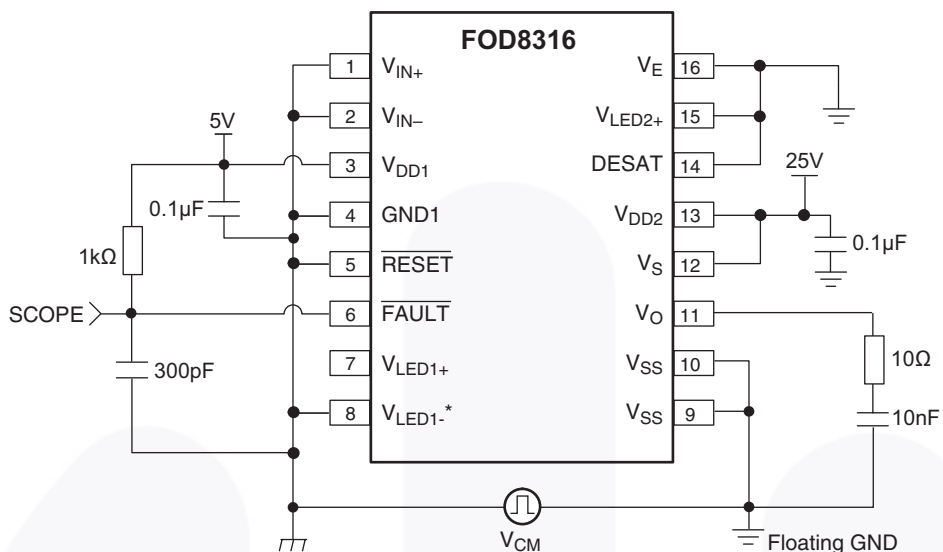


**Figure 44. Common Mode Low ( $CM_L$ ) Test Circuit @ LED1 Off**



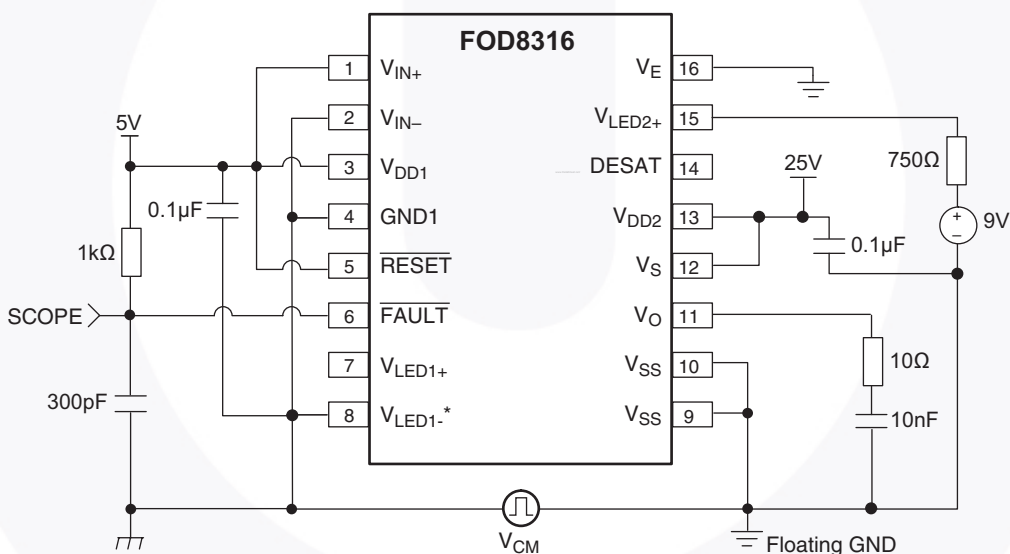
**Figure 45. Common Mode High ( $CM_H$ ) Test Circuit @ LED1 On**

**Test Circuits** (Continued)



\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

**Figure 46. Common Mode High ( $CM_H$ ) Test Circuit @ LED2 Off**



\*Pin 8 ( $V_{LED1-}$ ) is internally connected to pin 4 (GND1).

**Figure 47. Common Mode Low ( $CM_L$ ) Test Circuit @ LED2 On**

### Timing Diagrams

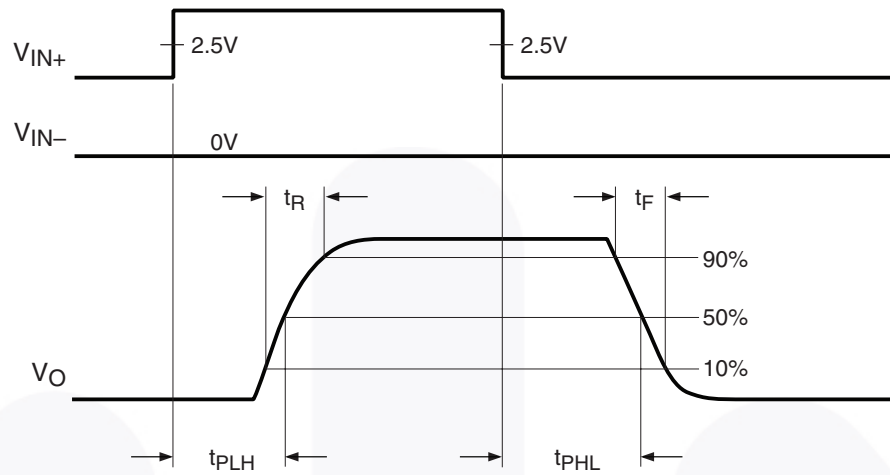


Figure 48. Propagation Delay ( $t_{PLH}$ ,  $t_{PHL}$ ), Rise Time ( $t_R$ ) and Fall Time ( $t_F$ ) Timing Diagram

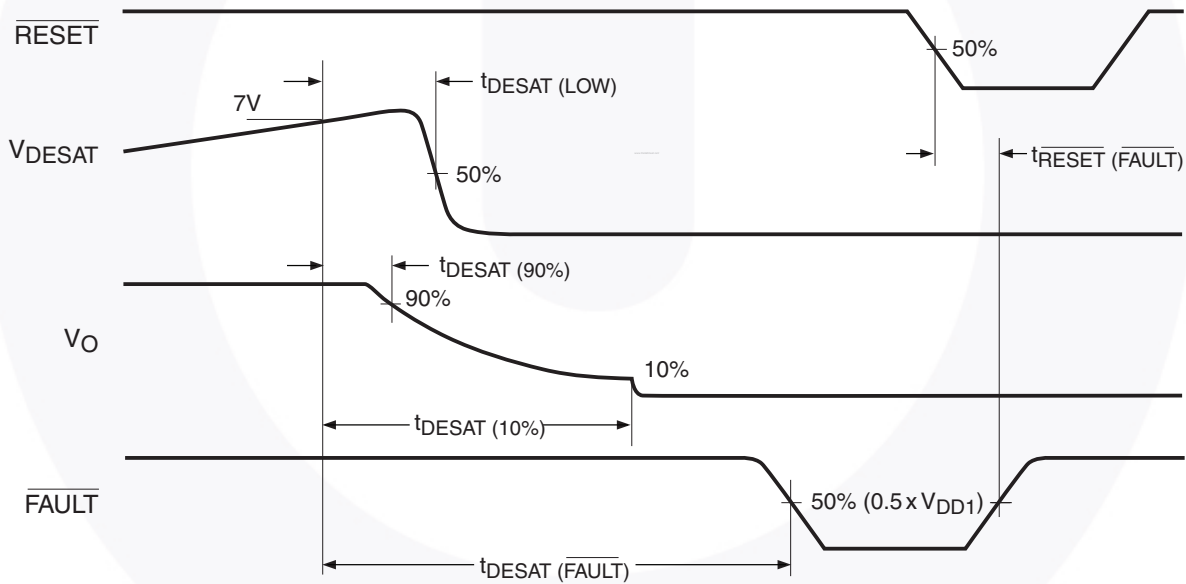


Figure 49. Definitions for Fault Reset Input ( $\overline{RESET}$ ), Desaturation Voltage Input (DESAT), Output Voltage ( $V_O$ ) and Fault Output ( $\overline{FAULT}$ ) Timing Waveforms

## Application Information

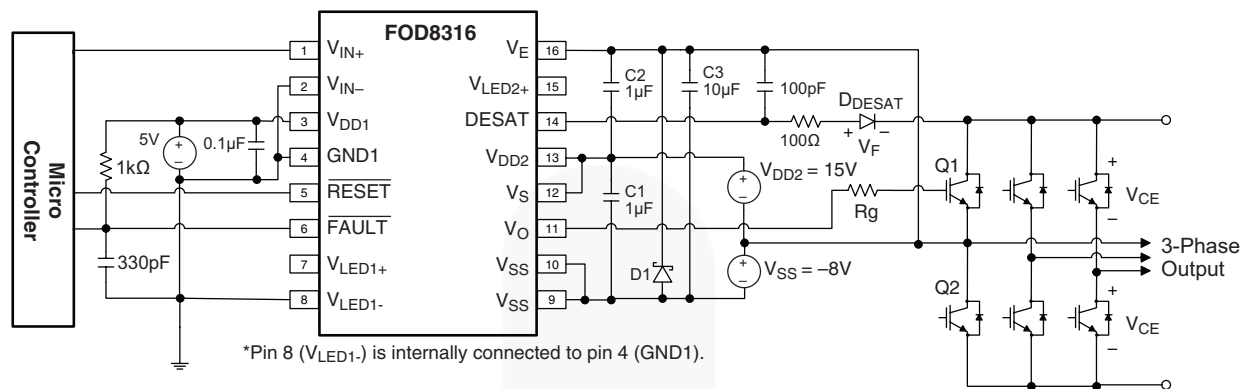


Figure 50. Recommended Application Circuit

### Functional Description

The typical application circuit is shown in Figure 50 and the functional behavioral of the FOD8316 is illustrated by the detailed internal schematic shown in Figure 51. This helps explain the interaction and sequence of internal and external signals, together with the timing diagrams.

#### 1. Non-Inverting and Inverting Inputs

There are two CMOS/TTL compatible inputs,  $V_{IN+}$  and  $V_{IN-}$  to control the IGBT, in non-inverting and inverting configurations respectively. When  $V_{IN-}$  is set to low,  $V_{IN+}$  controls the driver output,  $V_O$ , in non-inverting configuration. When  $V_{IN+}$  is set to high,  $V_{IN-}$  controls the driver output in inverting configuration.

The relationship between the inputs and output are illustrated in the Figure 52.

During normal operation, when no fault is detected, the  $\overline{FAULT}$  output, which is an open-drain configuration, will be latched to high state. This allows the gate driver to be controlled by the input logic signal.

When a fault is detected, the  $\overline{FAULT}$  output will be latched to low state. This condition will remain until the  $\overline{RESET}$  pin is also pulled low for a period longer than  $PW_{\overline{RESET}}$ . While setting the  $\overline{RESET}$  pin to a low state, the input pins must be pulled to low to ensure an output state ( $V_{IN+}$  is low or  $V_{IN-}$  is high).

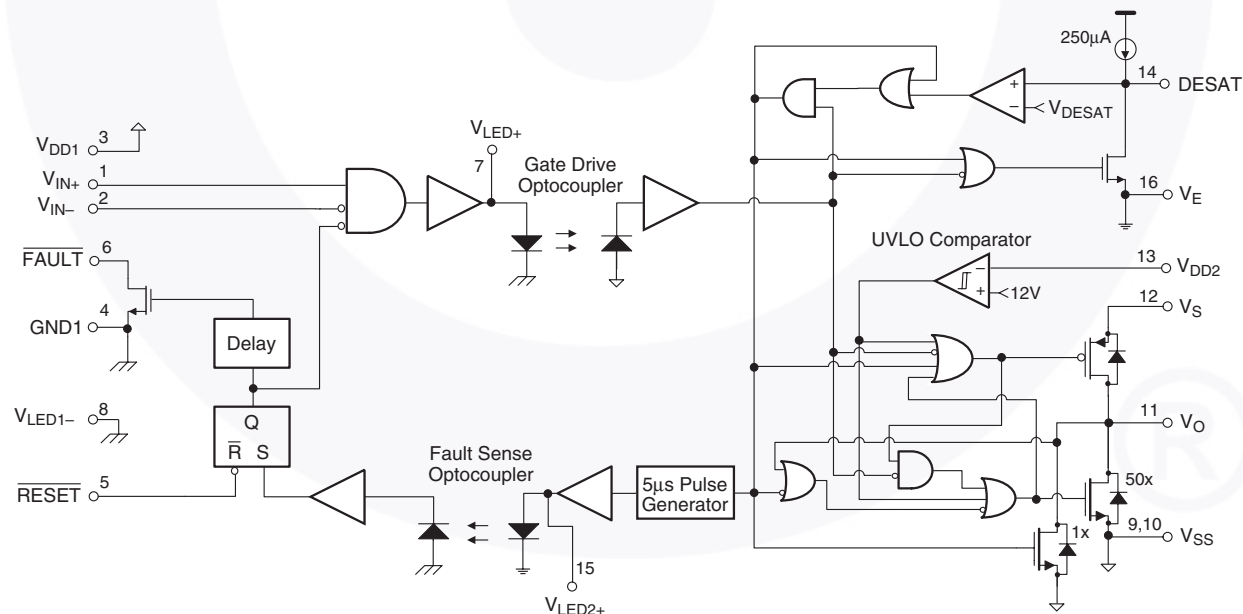


Figure 51. Detailed Internal Schematic

## 2. Gate Driver Output

A pair of PMOS and NMOS transistors make up the output driver stage, which facilitates close to rail-to-rail output swing. This feature allows a tight control of gate voltage during on-state and short circuit condition. The output driver is typically capable of sinking 2A and sourcing 2A at room temperature. Due to the low  $R_{DS(ON)}$  of the MOSFETs, the power dissipation is reduced as compared to those bipolar-type driver output stages. The absolute maximum rating of the output peak current,  $I_{O(PEAK)}$  is 3A, thus the careful selection of the gate resistor,  $R_g$ , is required to limit the short circuit current of the IGBT.

As shown in Figure 51, the gate driver output is influenced by signals from the photodetector circuitry, the UVLO comparator and the DESAT signals. Under no fault condition, normal operation resumes while the supply voltage is above the UVLO threshold, the output of the photodetector will drive the MOSFETs of the output stage.

The logic circuitry of the output stage will ensure that the push-pull devices will never be turned “ON” simultaneously. When the output of the photodetector is high, the output,  $V_O$  will be pulled to high state by turning on the PMOS. When the output of the photodetector is low,  $V_O$  will be pulled to low state by turning on the NMOS.

When  $V_{DD2}$  supply goes below  $V_{UVLO}$ , which is the designated ULVO threshold at the comparator,  $V_O$  will be pulled down to low state regardless of photodetector output.

When desaturation is detected,  $V_O$  will turn off slowly as it is pulled low by the NMOS<sup>1X</sup> device, the input to the Fault Sense circuitry will be latched to high state and turns on the LED. When  $V_O$  goes below 2V, the NMOS<sup>50X</sup> device turns on again, clamping the IGBT gate firmly to  $V_{SS}$ . The Fault Sense signal will remain latched in the high state until the LED of the gate driver circuitry turns off.

## 3. Desaturation Protection, FAULT Output

Desaturation detection protection ensures the protection of the IGBT at short circuit by monitoring the collector-emitter voltage of the IGBT in the half bridge. When the DESAT voltage goes up and reaches above the threshold voltage, a short circuit condition is detected and the driver output stage will execute a “soft” IGBT turn-off and will be eventually driven low. This sequence is illustrated in Figure 53. The  $\overline{FAULT}$  open-drain output is triggered active low to report a desaturation error. It could only be cleared by activating active low by the external controller to the  $\overline{RESET}$  input.

The DESAT fault detector should be disabled for a short time period (blinking time) before the IGBT turns on to allow the collector voltage to fall below DESAT threshold. This blinking period protects against false trigger of the DESAT while the IGBT is turning on.

## 4. “Soft” Turn-Off

The soft turn-off feature ensures the safe turn off of the IGBT under fault condition. This reduces the voltage spike on the collector of the IGBT. Without this, the IGBT would see a heavy spike on the collector and hence resulting in a permanent damage to the device when it's turned off immediately.

## 5. Under Voltage Lockout

Under voltage detection prevents the application of insufficient gate voltage to the IGBT. This could be dangerous, as it would drive the IGBT out of saturation and into the linear operation where the losses are very high and quickly overheated. This feature ensures the proper operating of the IGBTs. The output voltage,  $V_O$ , remains low irregardless of the inputs as long as the supply voltage,  $V_{DD2} - V_E$ , is less than  $V_{ULVO+}$ . When the supply voltage falls below  $V_{ULVO-}$ ,  $V_O$  will go low, as illustrated in Figure 54.

## 6. Time to Good Power

At initial power up, the LED is off and the output of the gate driver should be in the low or off state. Sometimes race conditions exist that causes the output to follow the  $V_D$  (assuming  $V_{DD2}$  and  $V_E$  are connected externally), until all of the circuits in the output IC have stabilized. This condition can result in output transitions or transients that are coupled to the driven IGBT. These transients can cause the high and low side IGBTs to conduct shoot-through current that may result in destructive damage to the power semiconductor devices. Fairchild has introduced an initial turn-on delay which is generally regarded as “time to good power”. This delay, typically 30 $\mu$ s, is only present during the initial power-up of the device. Once powered, the “time to good power” delay is determined by the delay of the UVLO circuitry. If the LED is “ON” during the initial turn-on activation, low to high transition at the output of the gate driver will only occur 30 $\mu$ s after the  $V_{DD2}$  power is applied.

## 7. Dual Supply Operation – Negative Bias at Vss

The IGBT's off-state noise immunity can be enhanced by providing a negative gate to emitter bias when the IGBT is in the off-state. This static off-state bias can be supplied by connecting a separate negative voltage source between the  $V_E$  (pin 16) and  $V_{SS}$  (pin 9 & 10). Figure 51 illustrates the two distinct grounds. The primary ground reference is the IGBT's emitter connection -  $V_E$ , pin 16. The under-voltage threshold and desaturation voltage detection are referenced to the IGBT's emitter ( $V_E$ ) ground.

The recommended application circuit, Figure 50, shows the interconnection of the  $V_{DD2}$  and  $V_E$  supplies. The IGBT's gate to emitter voltage is the absolute value sum of the  $V_{DD2}$  supply and the  $V_{SS}$  reverse bias. The negative voltage supply at  $V_{SS}$  appears at the gate drive input,  $V_O$ , when the FOD8316 is in the low state. When

the input drives the output high, the output voltage,  $V_O$ , will have the potential of the  $V_{DD2}$  and  $V_{SS}$ .

Figure 50 shows the operation with a dual or split power supply. The  $V_{SS}$  supply provides the negative gate bias, and  $V_{DD2} + V_{SS}$  supplies power to the output IC. The  $V_{SS}$  and  $V_{DD2}$  supplies require three power supply bypass capacitors. These capacitors provide the low equivalent series resistant (ESR) paths for the instantaneous gate charging and discharging currents.

Selecting capacitors with low ESR will optimize the available output current. C3 is a low ESR 1812 style, 10 $\mu$ F, multilayer ceramic capacitor. This capacitor is the primary filter for the  $V_{SS}$  and  $V_{DD2}$  supplies. C1 and C2 are also low ESR capacitors. They provide the primary gate charge and discharge paths. The Schottky diode, D1, is connected between  $V_E$  and  $V_{SS}$  to protect against a reverse voltage greater than 0.5V.

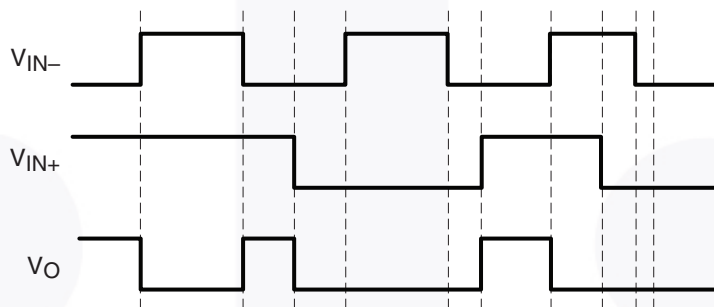


Figure 52. Input/Output Relationship

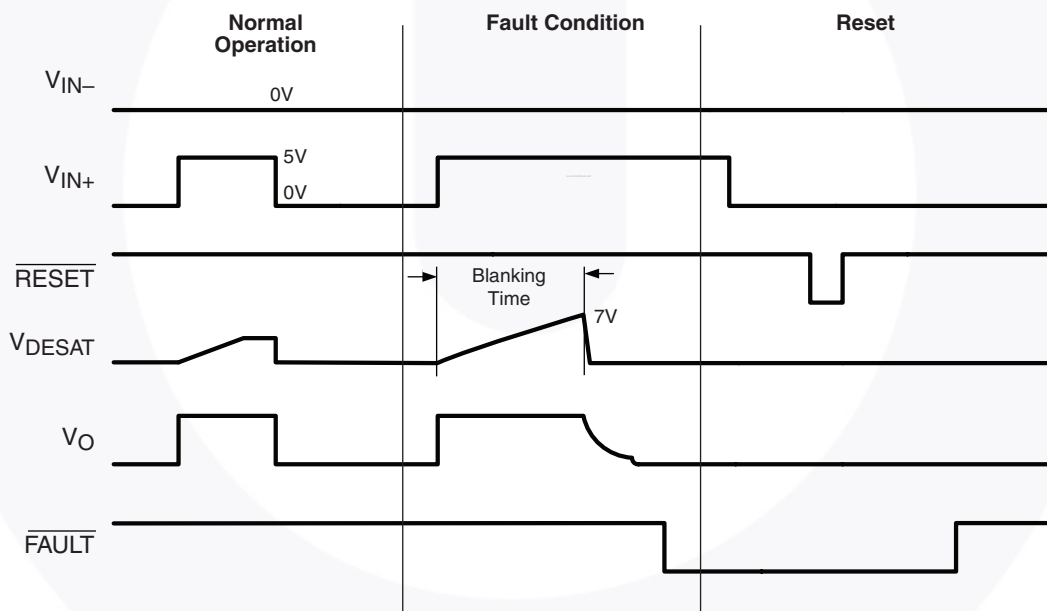


Figure 53. Timing Relationship Among Desaturation Voltage (DESAT), Fault Output ( $\overline{\text{FAULT}}$ ) and Fault Reset Input ( $\overline{\text{RESET}}$ )



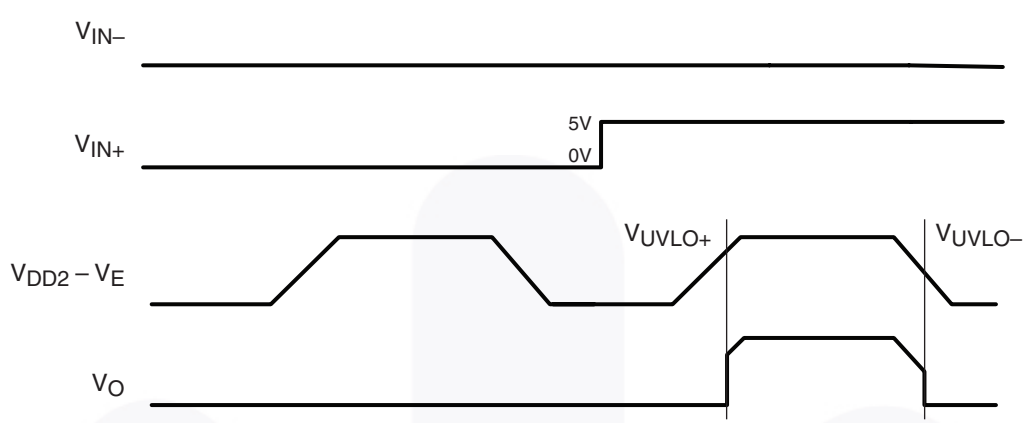



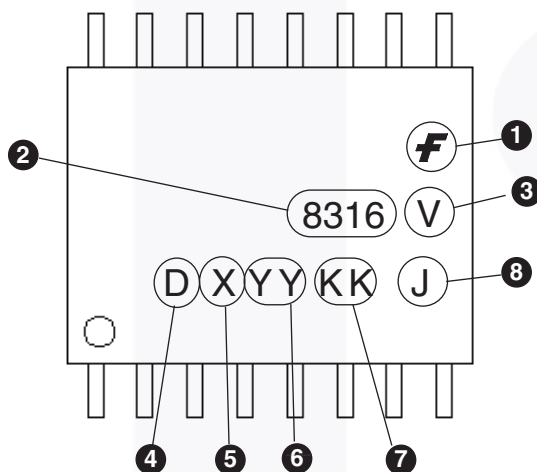
Figure 54. Under Voltage Lockout (UVLO) for Output Side

## Ordering Information

Part Number	Package	Packing Method
FOD8316	SO 16-Pin	Tube (50 units per tube)
FOD8316R2	SO 16-Pin	Tape and Reel (750 units per reel)
FOD8316V	SO 16-Pin, DIN EN/IEC 60747-5-5 option	Tube (50 units per tube)
FOD8316R2V	SO 16-Pin, DIN EN/IEC 60747-5-5 option	Tape and reel (750 units per reel)

 All packages are lead free per JEDEC: J-STD-020B standard.

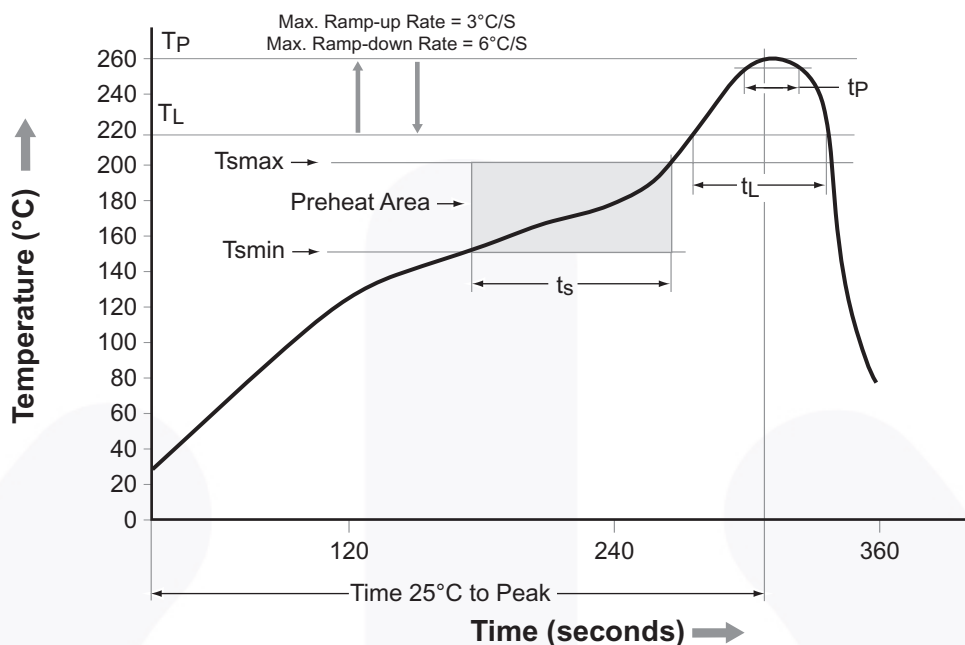
## Marking Information



### Definitions

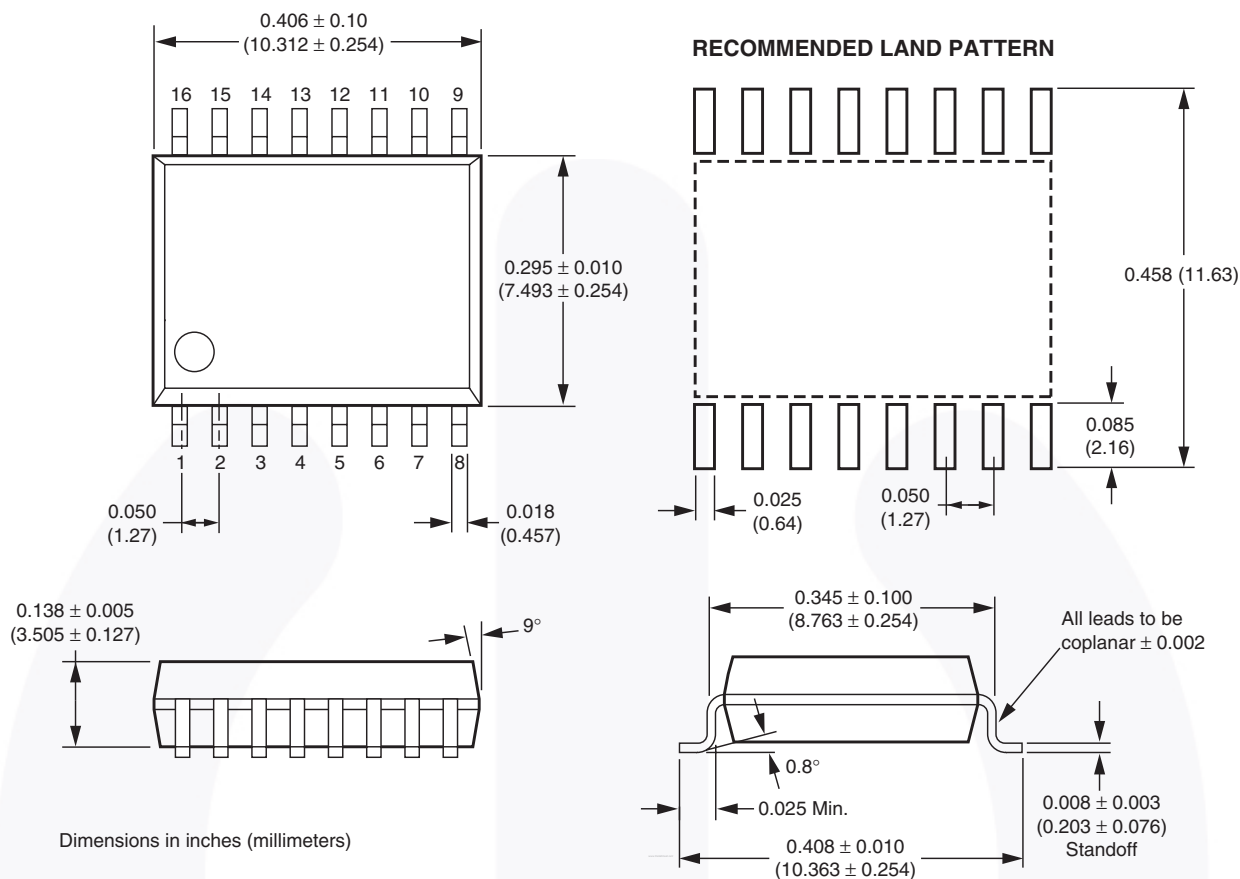
1	Fairchild logo
2	Device number, e.g., '8316' for FOD8316
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	Plant code, e.g., 'D'
5	Last digit year code, e.g., 'B' for 2011
6	Two digit work week ranging from '01' to '53'
7	Lot traceability code
8	Package assembly code, J

## Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60–120 seconds
Ramp-up Rate (tL to tP)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

## Package Dimensions






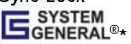
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