

Dual Operational Amplifier and Reference Regulator



General Description

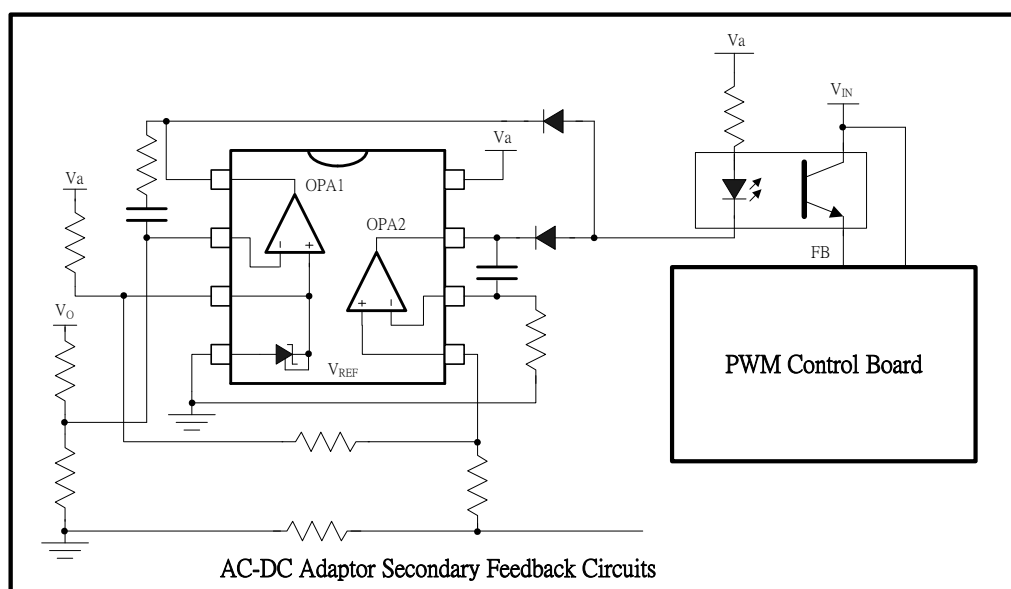
The FP103 is a single chip composed of one independent OP-AMP (OPA2) and another OP-AMP (OPA1) with a 2.5V precision voltage reference on non-inverting input. It offers space and low cost in many applications such as the secondary feedback control of power supply, DC/DC converter or adaptor.

The FP103 is designed for regulator feedback circuit with few external components. The circuit diagram for typical application is shown as below.

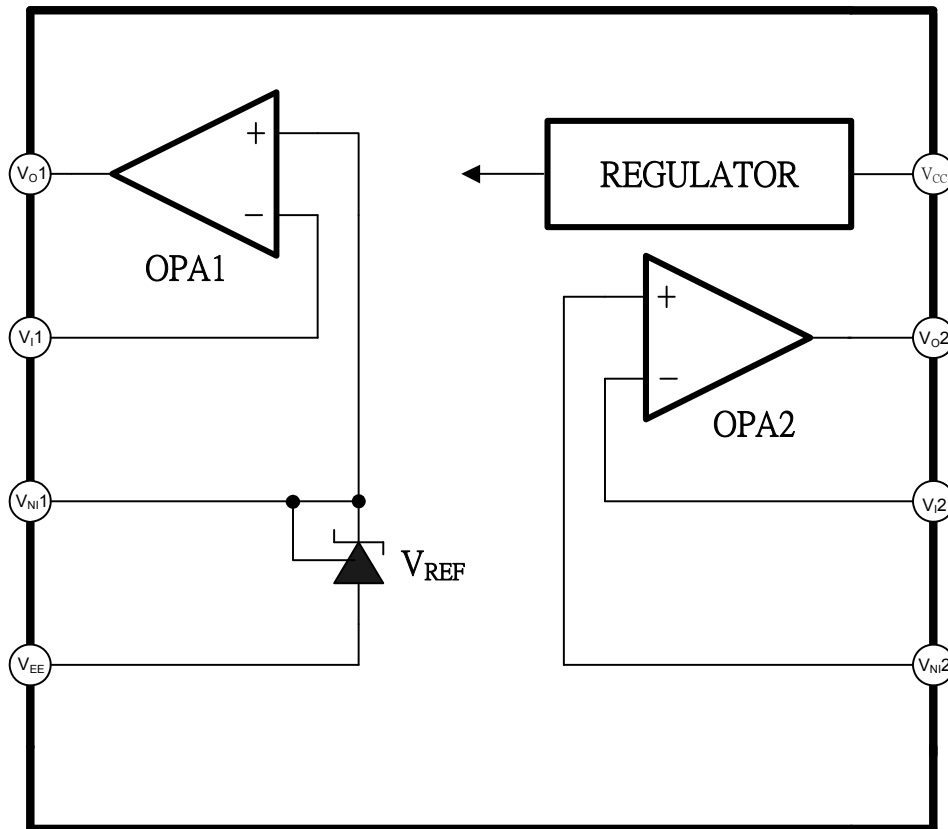
Features

- Fixed Reference Voltage: 2.5V
- Reference Voltage Precision: 1%
- Output Sink Current up to 100mA
- Low Quiescent Supply Current
- Wide Operating Voltage Range: 3~32V (+ / -16V)
- Low Input Offset Voltage
- Unit Gain Bandwidth: 0.9MHz
- Package: SOP-8L

Typical Application Circuit

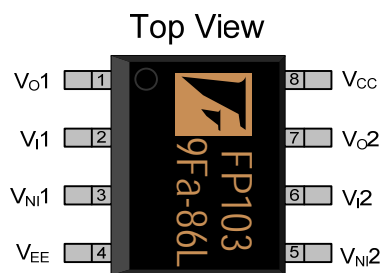


Function Block Diagram



Pin Descriptions

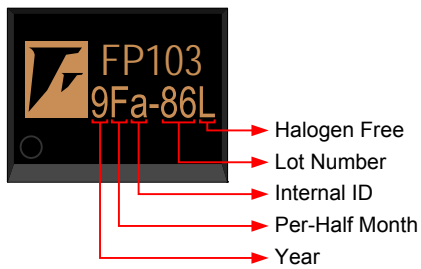
SOP-8L



Name	No.	I / O	Description
V_{O1}	1	O	OPA1 Output
V_{I1}	2	I	OPA1 Inverting Input
V_{NI1}	3	I	OPA1 Non-inverting Input
V_{EE}	4	P	IC Ground or Negative Supply Voltage
V_{NI2}	5	I	OPA2 Non-inverting Input
V_{I2}	6	I	OPA2 Inverting Input
V_{O2}	7	O	OPA2 Output
V_{CC}	8	P	Positive Supply Voltage

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Marking Information



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 1323~~86~~TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

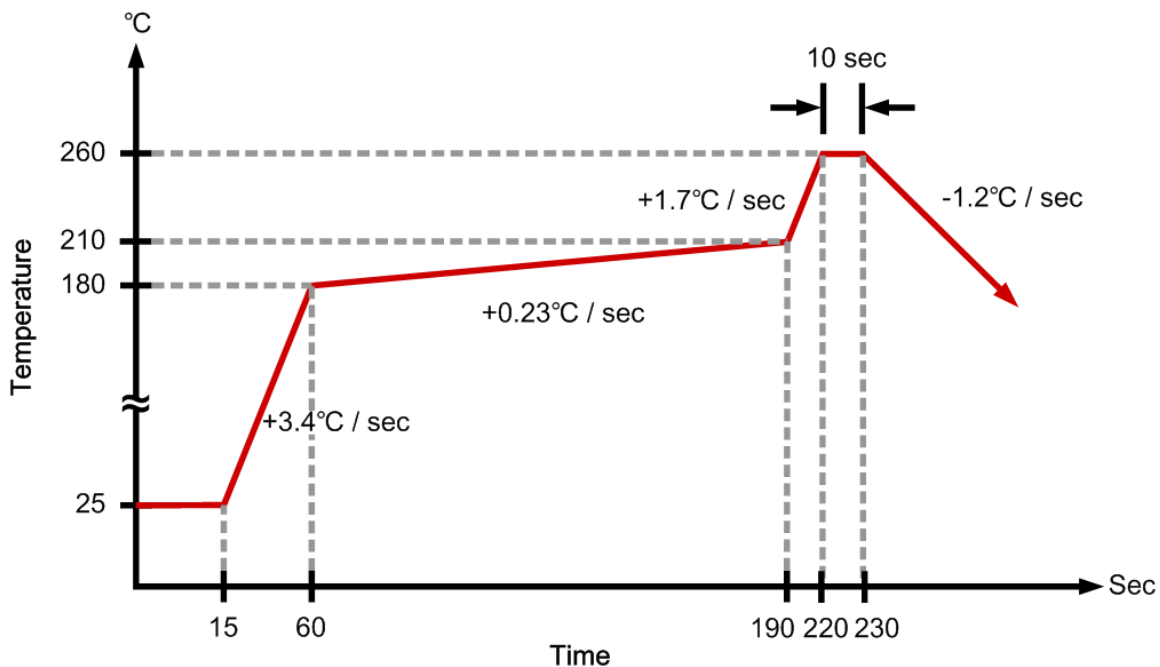
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP103DR-LF	-20°C ~ +85°C	SOP-8L	2500 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}				36	V
Differential Input Voltage	V_{ID}				36	V
Input Voltage	V_I		-0.3		36	V
Maximum Junction Temperature	T_J				150	°C
Thermal Resistance Junction to Ambient		SOP-8L Package			+175	°C / W
Power Dissipation (SOP-8L package)		$T_A=25^\circ\text{C}$			650	mW
		$T_A=70^\circ\text{C}$			550	mW
Operating Temperature		($T_{MIN} \sim T_{MAX}$)	-25		+85	°C
Storage Temperature Range			-65		+150	°C
Lead Temperature		(Soldering, 10 sec)			+260	°C

Suggested IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3		30	V
Operating Temperature			-20		85	°C

DC Electrical Characteristics

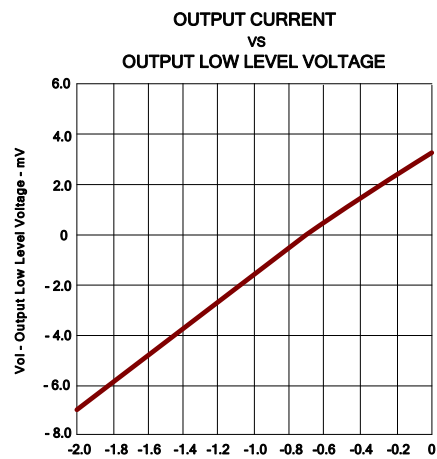
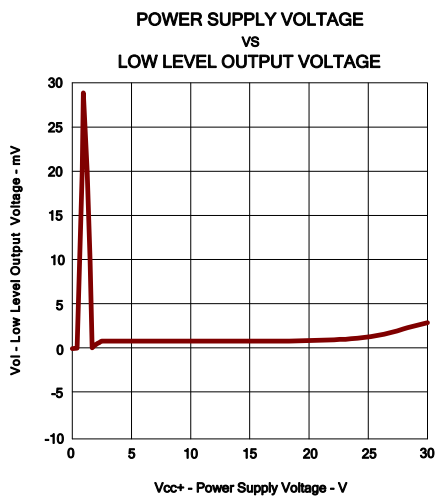
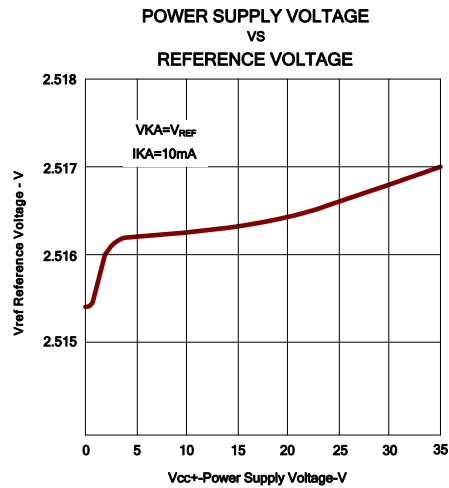
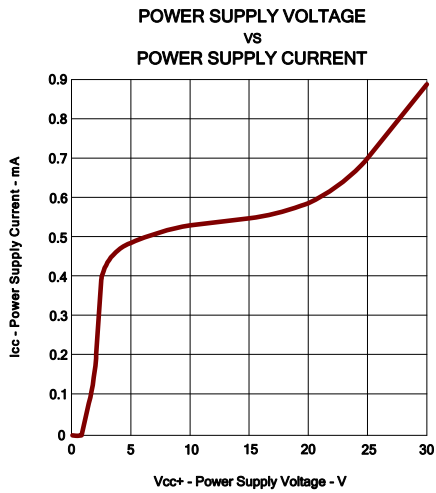
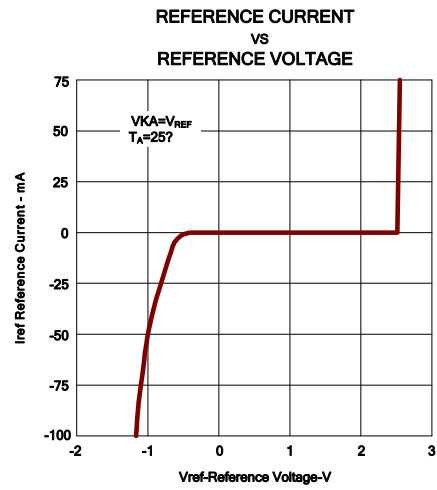
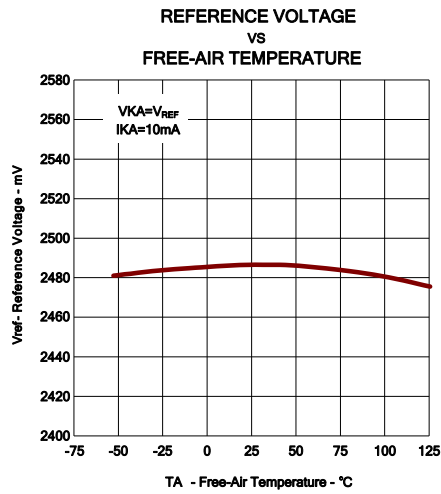
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Amplifier1						
Input Offset Voltage	V_{io}	$T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	4 5	mV
Input Offset Voltage Drift	DV_{io}	$T_{AMB}=25^{\circ}C$		7		$\mu V / ^{\circ}C$
Input Bias Current (negative input)	I_{ib}	$T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		20		nA
Large Signal Voltage Gain	A_{vd}	$V_{CC}=15V$ $V_{ICM}=0V, R_L=2K$		100		V / mV
Supply Voltage Rejection Ratio	SVR	$V_{CC}=5V$ to $30V$ $V_{ICM}=0V$	65	100		dB
Output Current Source	I_{source}	$V_{CC}=15V$ $V_{id}=+1V, V_O=2V$	30	50		mA
Short Circuit to Ground	I_o	$V_{CC}=15V$		50	70	mA
Output Current Sink	I_{sink}	$V_{CC}=15V$ $V_{id}=-1V, V_O=2V$	8	10		mA
High Level Output Voltage	V_{OH}	$V_{CC}=30V, R_L=10K$ $T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	27 27	28		V
Low Level Output Voltage	V_{OL}	$R_L=10K, T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		3	20 20	mV
Slew Rate at Unity Gain	SR	$V_{CC}=15V, V_i=0.5$ to $2V$ $R_L=2K, C_L=100pF$ Unity Gain	0.2	0.4		V / μS
Gain Bandwidth Product	GBP	$V_{CC}=30V, R_L=2K$ $C_L=100pF, f=100kHz,$ $V_{in}=10$ mV	0.5	0.9		MHz
Total Harmonic Distortion	THD	$V_{CC}=30V, R_L=2K$ $C_L=100pF, f=1kHz,$ $A_v=20dB, V_O=2V_{PP}$		0.02		%
Operating Amplifier2						
Input Offset Voltage	V_{io}	$T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		1	4 5	mV
Input Offset Voltage Drift	DV_{io}	$T_{AMB}=25^{\circ}C$		7		mv / °C
Input Offset Current	I_{io}	$T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		2	30 50	nA
Input Bias Current	I_{ib}	$T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		20	150 200	nA
Large Signal Voltage Gain	A_{vd}	$V_{CC}=15V, R_L=2K,$ $V_O=1.4V$ to $11.4V$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	50 25	100		V / mV

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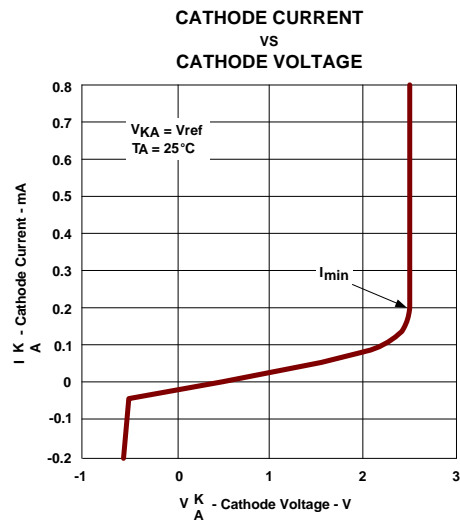
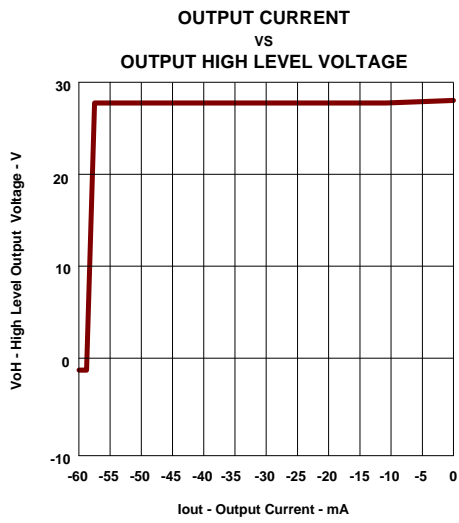
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage Rejection Ratio	SVR	$V_{CC}=5V$ to $30V$	65	100		dB
Input Common Mode Voltage Range	V_{icm}	$V_{CC}=30V$, $T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	0 0		$V_{CC}-1.5$ $V_{CC}-2$	V
Common Mode Rejection Ratio	CMRR	$T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	70 60	85		dB
Output Current Source	I_{SOURCE}	$V_{CC}=+15V$, $V_O=2V$, $V_{id}=+1V$	30	50		mA
Short Circuit to Ground	I_o	$V_{CC}=+15V$,		50	70	mA
Output Current Sink	I_{SINK}	$V_{ID}=-1V$, $V_{CC}=+15V$, $V_O=2V$	7	10		mA
High Level Output Voltage	V_{OH}	$V_{CC}=30V$ $T_{AMB}=25^{\circ}C$, $R_L=10K$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	27 27	28		V
Low Level Output Voltage	V_{OL}	$R_L=10K$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		3	20 20	mV
Slew Rate at Unity Gain	SR	$V_{CC}=15V$, $V_i=0.5$ to $3V$, $R_L=2K$, $C_L=100pF$, Unity Gain	0.2	0.4		V / μS
Gain Bandwidth Product	GBP	$V_{CC}=30V$, $R_L=2K$ $C_L=100pF$, $f=100kHz$, $V_{in}=10mV$	0.5	0.9		MHz
Total Harmonic Distortion	THD	$V_{CC}=30V$, $R_L=2K$, $C_L=100pF$, $f=1kHz$ $A_V=20dB$, $V_O=2V_{PP}$		0.02		%
Voltage Reference						
Cathode Current	I_k		1		100	mA
Reference Input Voltage	V_{REF}	$T_{AMB}=25^{\circ}C$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$	2.475 2.450	2.5	2.525 2.550	V
Reference Input Voltage Deviation Over Temperature Range	ΔV_{REF}	$V_{KA}=V_{REF}$, $I_K=10mA$ $T_{MIN} \leq T_{AMB} \leq T_{MAX}$		7	30	mV
Minimum Cathode Current for Regulation	I_{MIN}	$V_{KA}=V_{REF}$		0.2	1	mA
Dynamic Impedance (note 1)	$ Z_{KA} $	$V_{KA}=V_{REF}$, $\Delta I_K=1$ to $100mA$, $f < 1KHz$		0.2	0.5	Ω
Total Supply Current						
Total Supply Current, Excluding Current in the Voltage Reference	I_{CC}	$V_{CC}=5V$, no load $T_{MIN} < T_{AMB} < T_{MAZ}$ $V_{CC}=30V$, no load $T_{MIN} < T_{AMB} < T_{MAX}$		0.7 0.7	1.2 2	mA

Note 1: The dynamic impedance is defined as $Z_{KA}=\Delta V_{KA}/\Delta I_K$

Typical Operating Characteristics

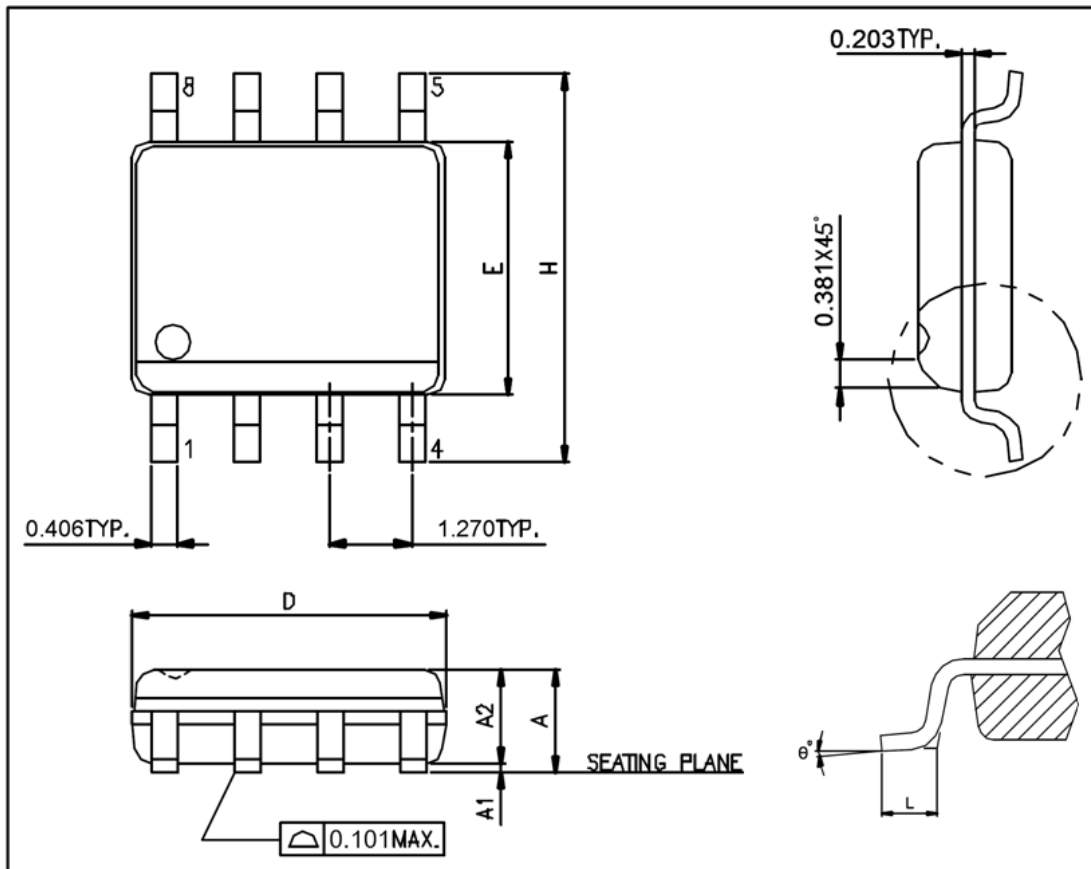


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Package Outline

SOP-8L



Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2	1.092	1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC Outline: MS-012 AA.
2. Dimension "D" does not include molding flash, protrusions or gate burrs.
3. Dimension "E" does not include inter-lead flash, or protrusions.

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