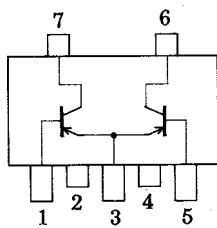


**SANYO****FP210**

NPN Epitaxial Planar Silicon Transistor

**Driver Applications****Features**

- Composite type with 2 transistors (PNP) contained in one package, facilitating high-density mounting.
- The FP210 is formed with 2 chips being equivalent to the 2SB1123, placed in one package.

**Electrical Connection**

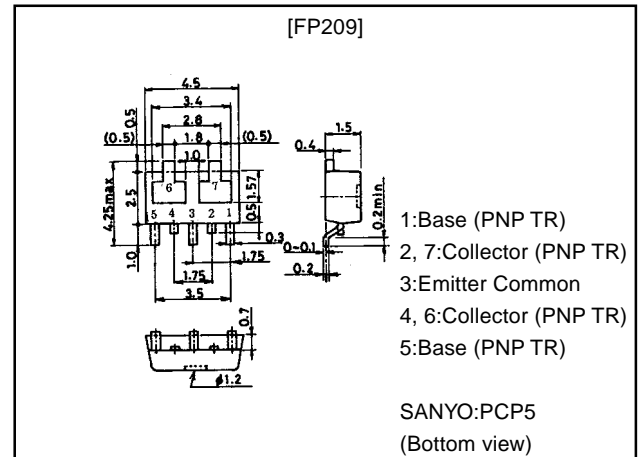
- 1:Base (PNP TR)  
2, 7:Collector (PNP TR)  
3:Emitter Common  
4, 6:Collector (PNP TR)  
5:Base (PNP TR)

(Top view)

**Package Dimensions**

unit:mm

2097A

**Specifications****Absolute Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	$V_{CB0}$		-60	V
Collector-to-Emitter Voltage	$V_{CE0}$		-50	V
Emitter-to-Base Voltage	$V_{EB0}$		-6	V
Collector Current	$I_C$		-2	A
Collector Current (Pulse)	$I_{CP}$		-4	A
Base Current	$I_B$		-400	mA
Collector Dissipation	$P_C$	Mounted on ceramic board (250mm <sup>2</sup> ×0.8mm) 1 unit	0.8	W
Total Dissipation	$P_T$	Mounted on ceramic board (250mm <sup>2</sup> ×0.8mm)	1.1	W
Junction Temperature	$T_j$		150	°C
Storage Temperature	$T_{stg}$		-55 to +150	°C

**Electrical Characteristics at Ta=25°C**

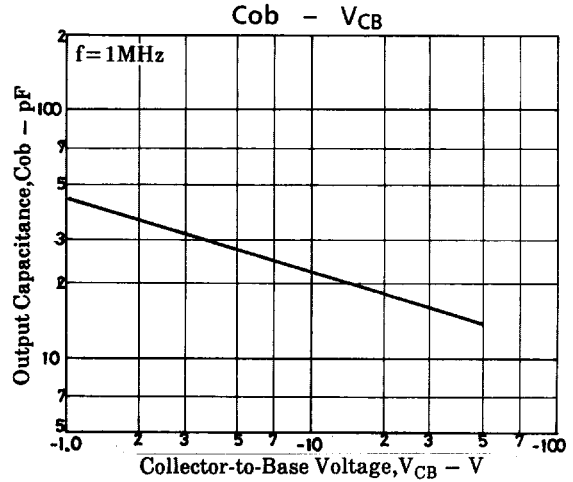
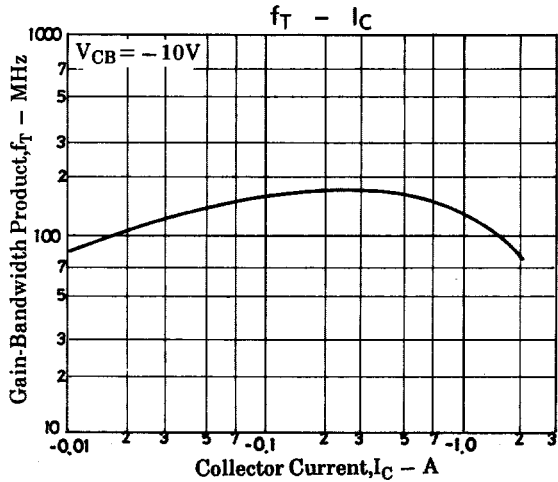
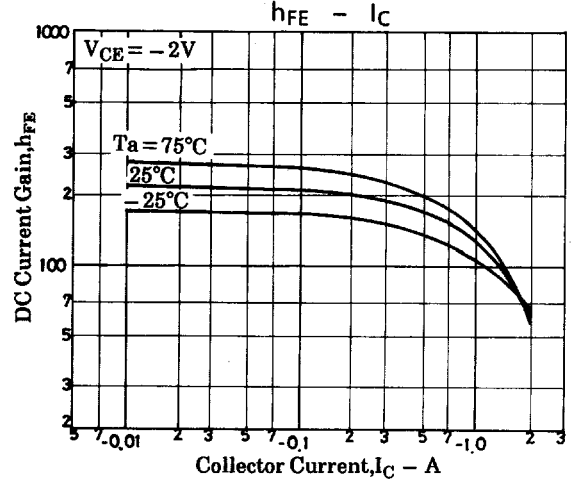
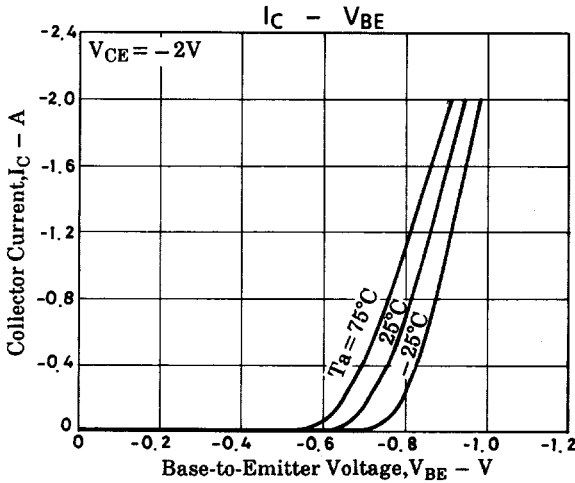
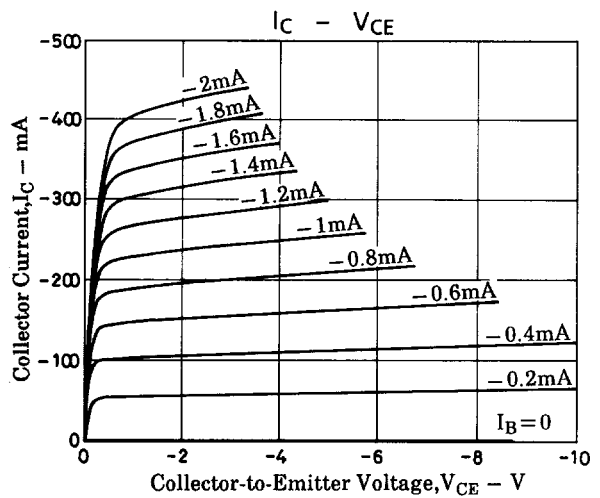
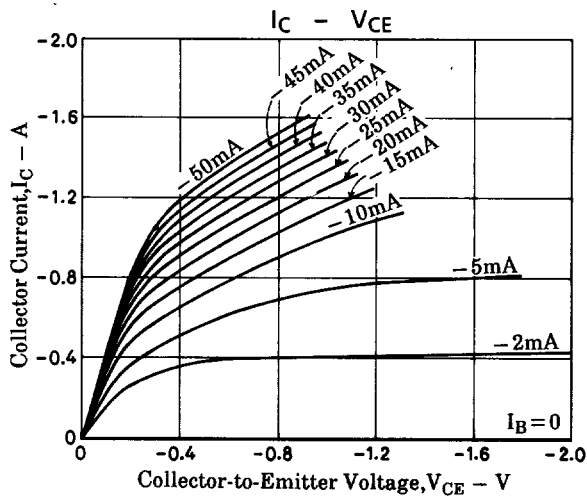
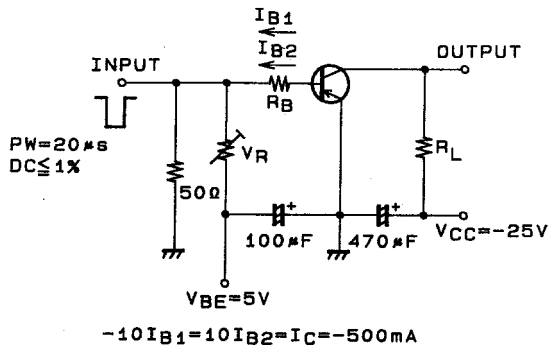
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	$I_{CBO}$	$V_{CB}=-50V, I_E=0$			-100	nA
Emitter Cutoff Current	$I_{EBO}$	$V_{EB}=-4V, I_C=0$			-100	nA
DC Current Gain	$h_{FE}$	$V_{CE}=-2V, I_C=-100mA$	140		400	
Gain-Bandwidth Product	$f_T$	$V_{CE}=-10V, I_C=-50mA$		150		MHz
Output Capacitance	$C_{ob}$	$V_{CB}=-10V, f=1MHz$		22		pF
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C=-1A, I_B=-50mA$	-0.3		-0.7	V
B-E Saturation Voltage	$V_{BE(sat)}$	$I_C=-1A, I_B=-50mA$	-0.9		-1.2	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	$I_C=-10\mu A, I_E=0$	-60			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	$I_C=-1mA, R_{BE}=\infty$	-50			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	$I_E=-10\mu A, I_C=0$	-6			V
Turn-ON Time	$t_{on}$	See specified Test Circuit		60		ns
Storage Time	$t_{stg}$	See specified Test Circuit		450		ns
Fall Time	$t_f$	See specified Test Circuit		30		ns

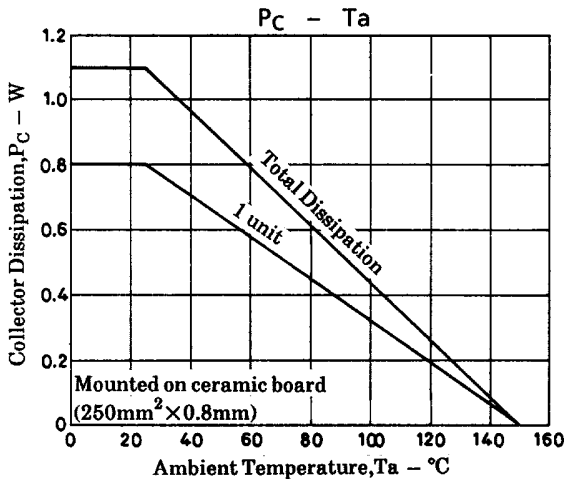
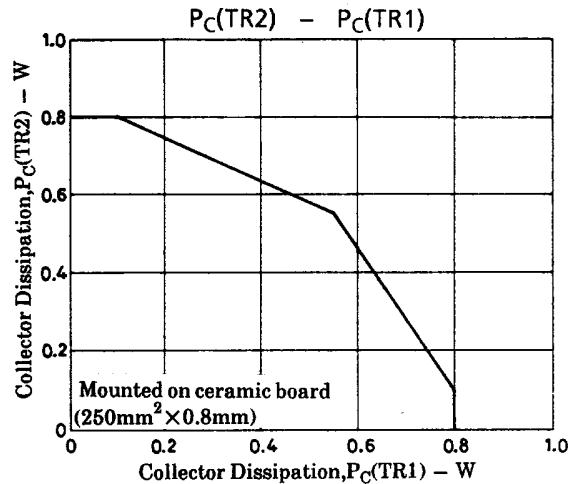
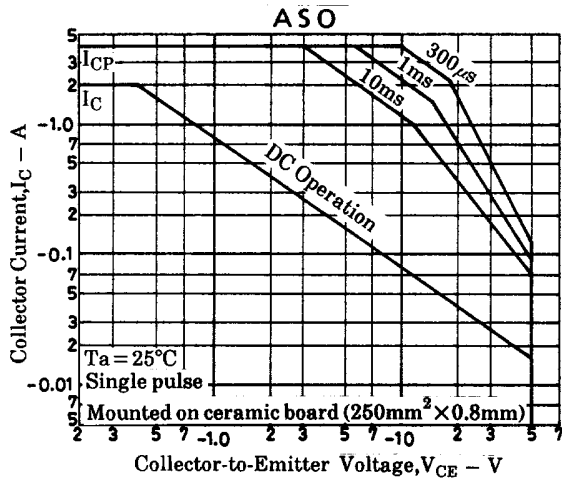
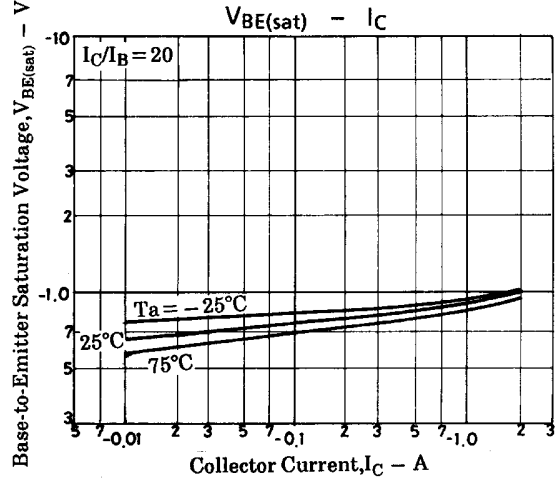
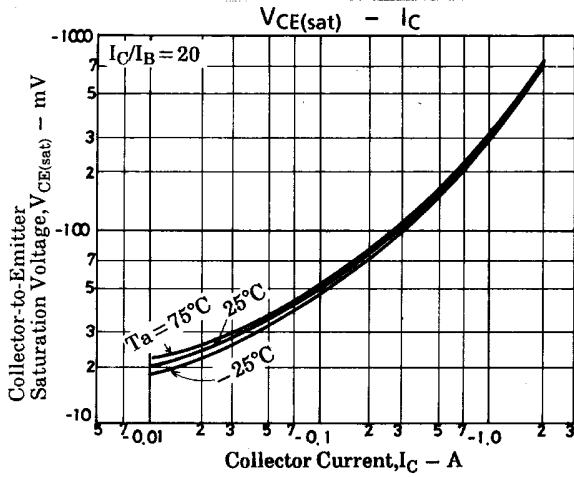
Marking:210

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Switching Time Test Circuit





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