PWM Controller With SCP / DTC Function

Halogen Free

General Description

The FP5001 is a single chip pulse -width-modulation controller composed of an open collector transistor output, an error amplifier and duty control comparators (DTC). The FP5001 contains a 1.0V precision voltage reference regulator, under-voltage lockout circuit (UVLO), short circuit protection circuit (SCP). It is applied to offer space and low cost in many applications such as the DC / DC converter and backlight inverter.

Using FP5001, it is easy to complete a power conversion regulator design with few external components. The circuit diagram of the typical application example is shown as below.

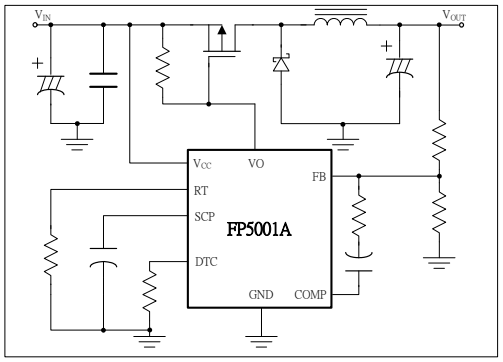
Features

- Wide Operating Voltage Range: 3.6~40V
- Reference Voltage Precision: 2%
- Oscillator Frequency: 500KHz Max.
- Output sink current up to 100mA
- Low Quiescent Supply Current
- Variable Dead-time Control (DTC)
- UVLO Protection Function
- SCP Protection Function
- Package: SOP-8L

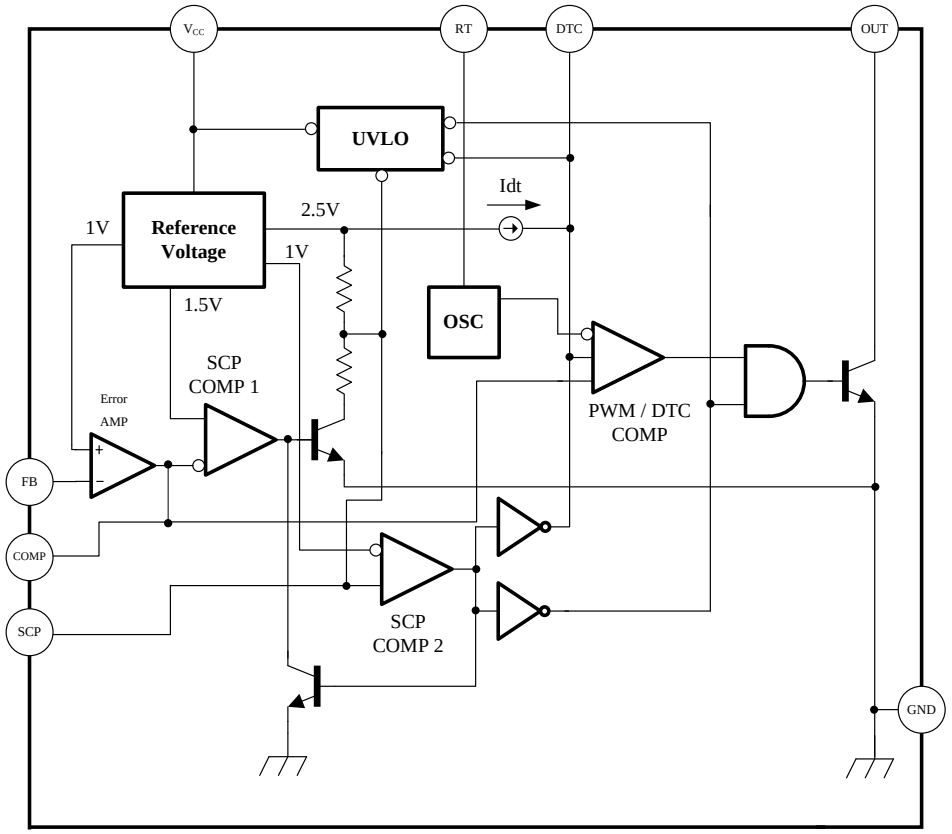
Applications

- Graphic Card
- Telecom and Datacom Applications
- High Power DC-DC Regulators

Typical Application Circuit

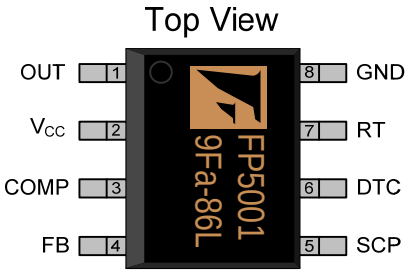


Function Block Diagram



Pin Descriptions

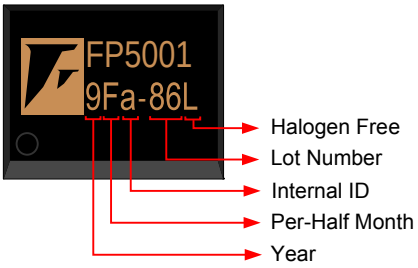
SOP-8L



Name	No.	I / O	Description
OUT	1	O	Open Collector Transistor Output
V_{CC}	2	P	IC Power Supply
COMP	3	O	Error Amplifier Output
FB	4	I	Error Amplifier Inverting Input
SCP	5	I	Short Circuit Protection Input
DTC	6	I	Duty Control Input
RT	7	I	Oscillator Frequency Control Input
GND	8	P	IC Ground

Marking Information

SOP-8L



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code n

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

Februa ry → C (Front Half Month), D(Last Half Month)

Year: Production year's last digit

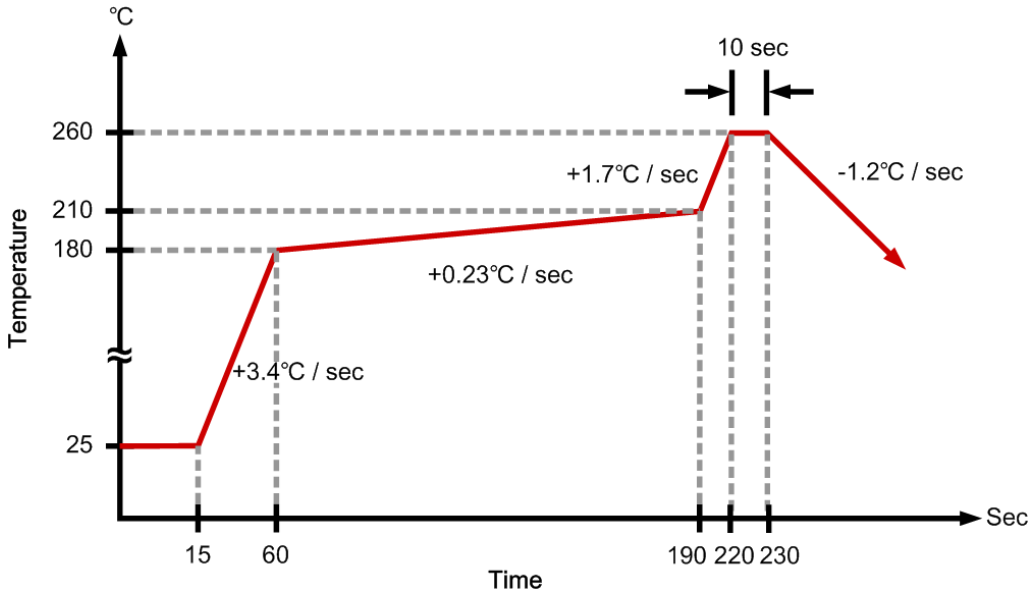
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP5001DR-LF	-20°C ~ +85°C	SOP-8L	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}				40	V
Differential Input Voltage	V_{ID}				20	V
Collector Output Voltage	Vo				40	V
Collector Output Current	Io				150	mA
Maximum Junction Temperature	T_J				150	℃
Junction to Ambient Thermal Resistance	SOP-8L Package				+175	℃ / W
Power Dissipation (SOP-8L package)		T_A=25℃			650	mW
		T_A=70℃			550	mW
Storage Temperature Range			-65		+150	°C
Lead Temperature (Soldering, 10 sec)					+260	°C

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3.6		40	V
Operating Temperature			-20		+85	°C
Operating Junction Temperature			-65		+150	°C

DC Electrical Characteristics (V_{CC}= 6V, T_A=25°C, f_{OSC}=70KHz unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference						
Output Voltage	V_{REF}	COMP Connected to FB	0.98	1	1.02	V
Input Regulation	$\triangle V_{REF}$	V_{CC} = 3.6 V to 40 V	2		12.5	mV
Output Voltage Change with Temperature	$\triangle V_{REF}$ / V_{REF}	T_A = -20℃ to 25℃	-10	-1	15	mV / V
		T_A = 25 ℃ to 85℃	-10	-2	10	mV / V
Under Voltage Lockout						
Upper Threshold Voltage	V_{upper}		3			V
Lower Threshold Voltage	V_{low}			2.8		V
Hysteresis V	hys		100	200		mV
Reset Threshold Voltage	V_{reset}		2.1	2.55		V
Short-Circuit Protection						
SCP Threshold Voltage	V_{TH}		0.95	1.00	1.05	V
SCP Voltage, Latched	V_{LATCH}	No Pullup		2.4		V
SCP Voltage, UVLO Operation	V_{OPR}		140	185	230	mV
SCP Voltage, UVLO Standby	$V_{STANDBY}$	No Pullup		60	120	mV
Input Source Current	I_{SOURCR}	T_A = 25℃	-10	-15	-20	μA
SCP Comparator 1 Threshold Voltage	$V_{COMP\ (TH)}$			1.5		V
Oscillator						
Frequency f		R_T = 100K	70			KHz
Standard Deviation of Frequency	$\triangle f$		15			KHz
Frequency Change with Voltage	$\triangle f$ / $\triangle V$	V_{CC} = 3.6V to 40V	1			KHz
Frequency Change with Temperature	$\triangle f$ / $\triangle T$	T_A = -20℃ to 25℃	-4	-0.4	4	KHz
		T_A = 25 ℃ to 85℃	-4	-0.2	4	KHz
Voltage at RT	V_{RT}			1		V

DC Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Duty Control						
Output (Source) Current	I_{SOURCE}	$V_{(DT)}$ = 1.5V	0.9×I_{RT}‡	1.2×	I_{RT}	μA
Input Threshold Voltage	V_{TH}	Duty Cycle = 0%	0.5 0.7			V
		Duty Cycle = 100%		1.3	1.5	V
Error Amplifier						
Input Voltage	V_{IN}	V_{CC} = 3.6V to 40V	0		1.5	V
Input Bias Current	V_{BIAS}			-160	-500	nA
Output Voltage Swing Positive	V_{POS}		1.5	2.3		V
Output Voltage Swing Negative	V_{NEG}			0.3	0.4	V
Open-loop Voltage Amplification	A_{VO}		80			dB
Unity-Gain Bandwidth	BW_U		1.5			MHz
Output (Sink) Current	I_{SINK}	$V_{I\ (FB)}$ = 1.2V, COMP = 1V	600 1	100		μA
Output (Source) Current	I_{SOURCE}	$V_{I\ (FB)}$ = 0.8V, COMP = 1V	-45 -70			μA
Output						
Output Saturation Voltage	V_{SAT}	I_O = 10mA		0.8	1.2	V
Off-state Current	I_{OFF}	V_O = 40V , V_{CC} = 0			10	μA
		V_O = 40V			10	μA
Short-circuit Output Current	I_{SC}	V_O = 6V		40		mA
Total Device						
Standby Supply Current Off State	$I_{STANDBY}$			1	1.5	mA
Average Supply Current	I_{AVE}	R_T = 100k		1.2	1.5	mA

Function Description

Voltage Reference

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the FP5001. A resistive divider provides 1V reference for the error amplifier and the SCP circuit.

Error Amplifier

The error amplifier compares a sample of the DC-DC converter's output voltage to the 1V reference and generates an error signal for the PWM comparator. The DC-DC converter's output voltage can be set by following expression:

Vo = (1 + R1 / R2) × (1 V)

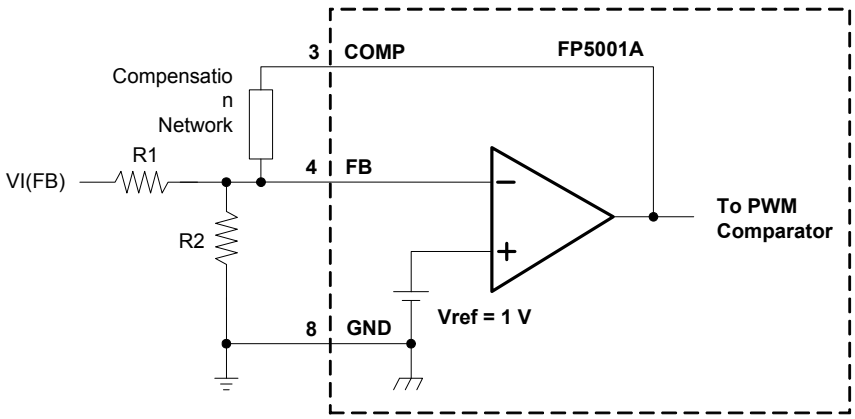


Figure 1. Error-Amplifier Gain Setting

The error amplifier's output is brought out as COMP for use in compensating the DC-DC converter's control loop for stability. Because the amplifier can only source 45 μA, the total DC load resistance should be 100 kΩ or larger.

Oscillator / PWM

The oscillator frequency (fosc) can be set from 20 kHz to 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error amplifier's output voltage and the DTC input voltage to the triangular wave. It turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

Duty Control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a maximum duty reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when V_{DT} is smaller than 0.7 V and 100% when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation. The voltage limits for the frequency in question can be found in Figure 11 (V_{osc}max and V_{osc}min are the maximum and minimum oscillator levels):

$$R_{DT} = (R_T + 1250) [D (V_{osc}max - V_{osc}min) + V_{osc}min]$$

Where

R_{DT} and R_T are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT} R_{DT} \left(1 - e^{\left(- t / R_{DT} C_{DT} \right)} \right)$$

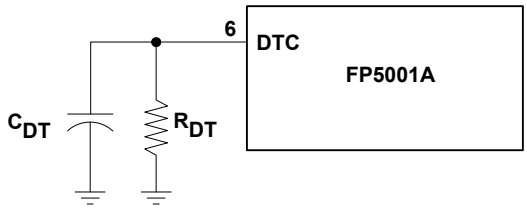


Figure 2. Soft-Start Circuit

If the DC-DC converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The FP5001 remains off when V_{DT} < 0.7 V, the minimum OSC ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

Under Voltage Lockout (UVLO) Protection

The under voltage lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V at 25°C) for proper operation.

A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

Short-circuit Protection (SCP)

The FP5001 includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5V. If the short is removed and the error-amplifier output drops below 1.5V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the FP5001 output transistor.

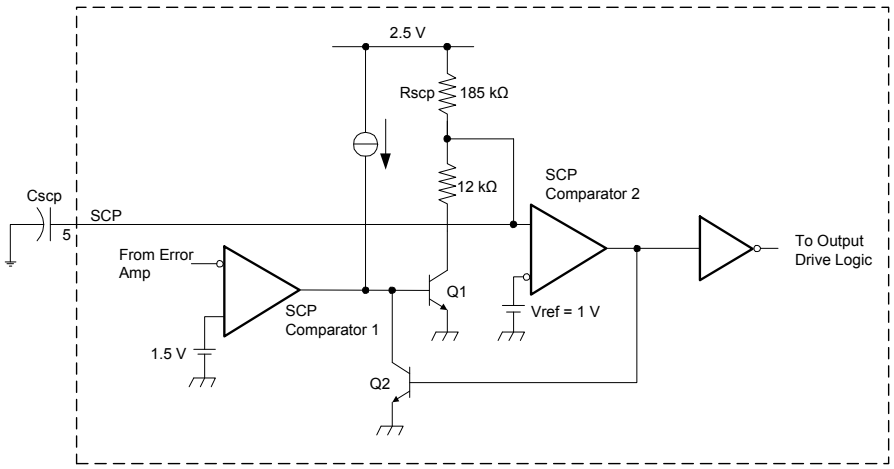


Figure 3. SCP Circuit

The timer operates by charging an external capacitor (CSCP), connected between the SCP terminal and ground, towards 2.5V through a 185-kΩ resistor (RSCP). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$V_{SCP} = (2.5 - 0.185)(1 – e^{-t/\tau}) + 0.185$

Where

$\tau = R_{SCP}C_{SCP}$

The end of the time-out period, t_{SCP}, occurs when V_{SCP} = 1 V. Solving for C_{SCP} yields:

$C_{SCP} = 12.46 \times t_{SCP}$ Where t is in seconds, C in μF.

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

Output Transistor

The output of the FP5001 is an open-collector transistor with a maximum collector current rating of 100mA and a voltage rating of 40V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

PARAMETER MEASUREMENT INFORMATION

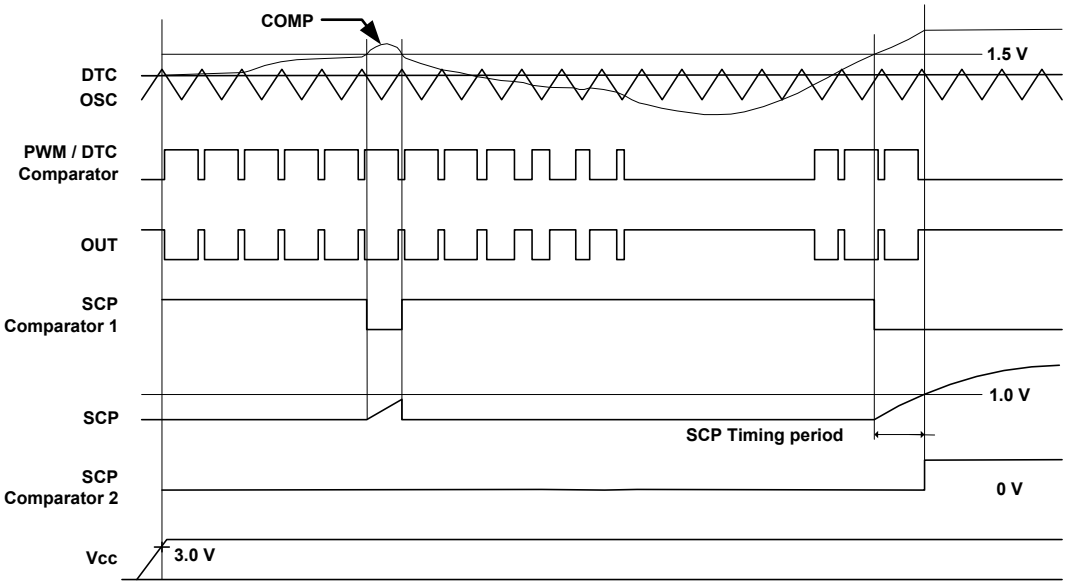


Figure 4. PWM Timing Diagram

Typical Operating Characteristics

OSCILLATOR FREQUENCY
VS
TIMING RESISTANCE

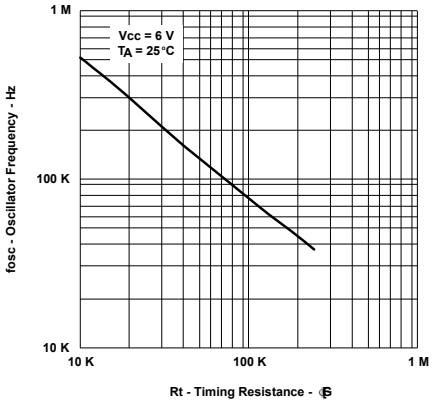


Figure 5

OSCILLATOR FREQUENCY
VS
AMBIENT TEMPERATURE

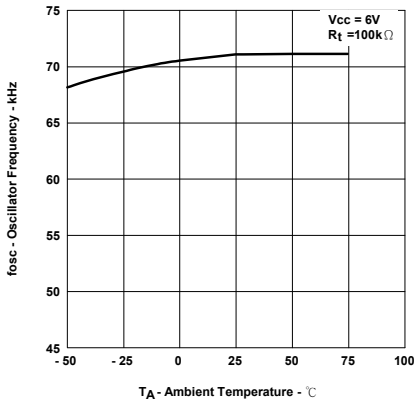


Figure 6

REFERENCE OUTPUT VOLTAGE
VS
POWER-SUPPLY VOLTAGE

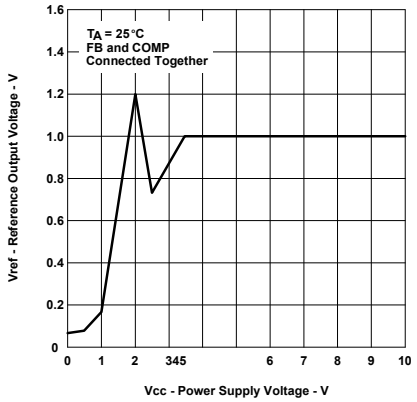


Figure 7

REFERENCE OUTPUT VOLTAGE FLUCTUATION
VS
AMBIENT TEMPERATURE

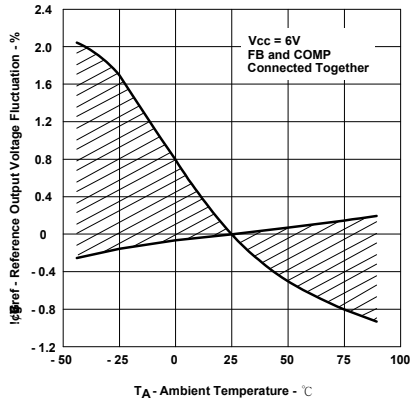


Figure 8

AVERAGE SUPPLY CURRENT
VS
POWER-SUPPLY VOLTAGE

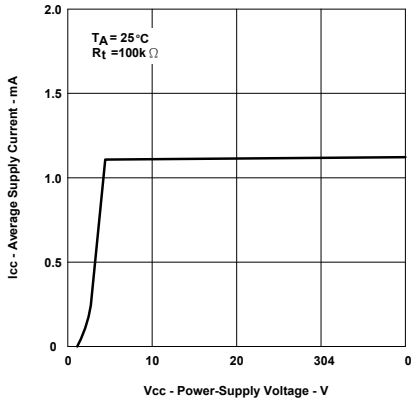


Figure 9

AVERAGE SUPPLY CURRENT
VS
AMBIENT TEMPERATURE

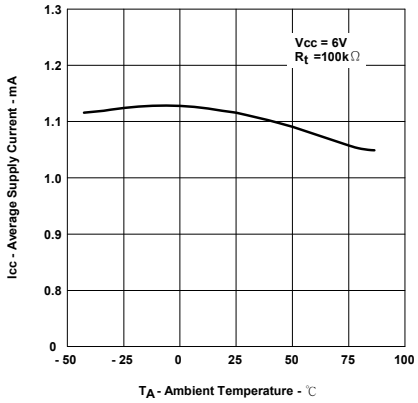


Figure 10

PWM TRIANGLE WAVE AMPLITUDE VOLTAGE
VS
OSCILLATOR FREQUENCY

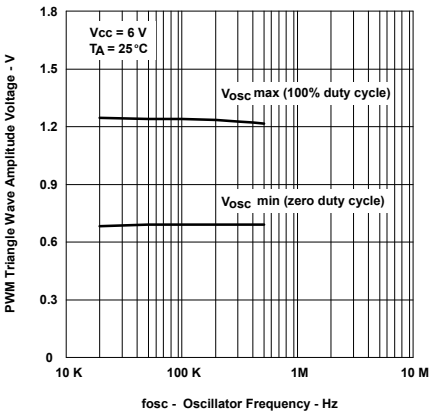


Figure 11

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
OUTPUT (SINK) CURRENT

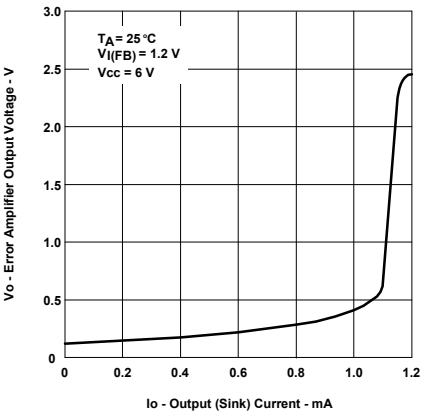


Figure 12

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
OUTPUT (SOURCE) CURRENT

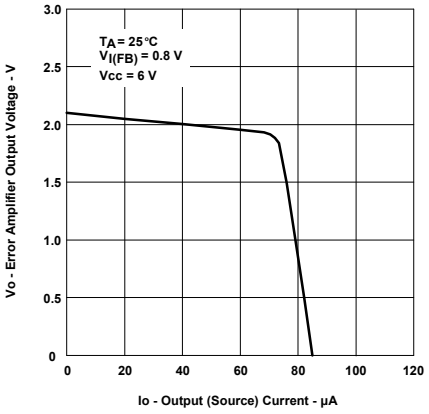


Figure 13

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
AMBIENT TEMPERATURE

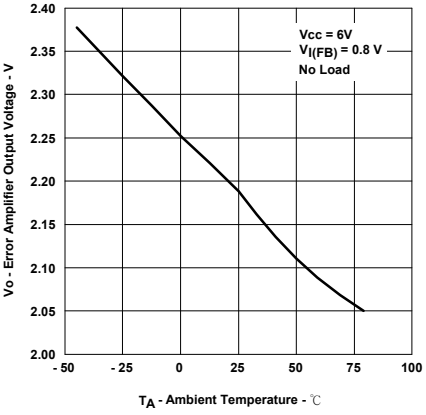


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
AMBIENT TEMPERATURE

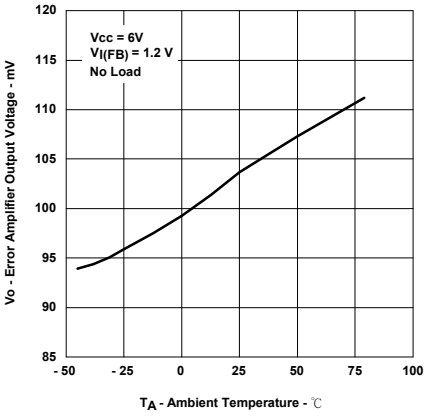


Figure 15

OUTPUT DUTY CYCLE
VS
DTC VOLTAGE

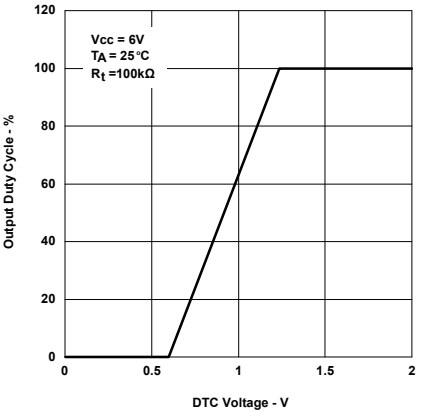


Figure 16

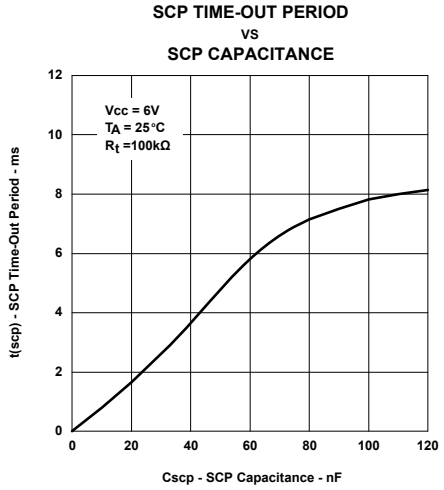


Figure 17

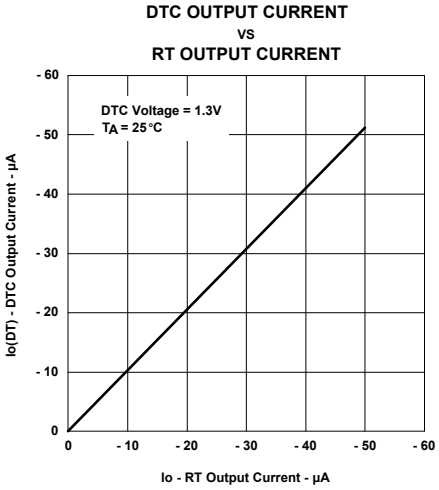


Figure 18

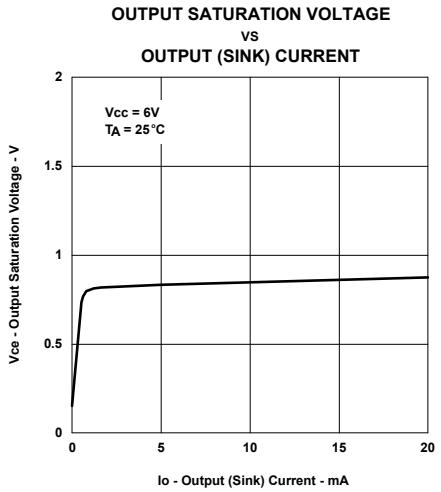
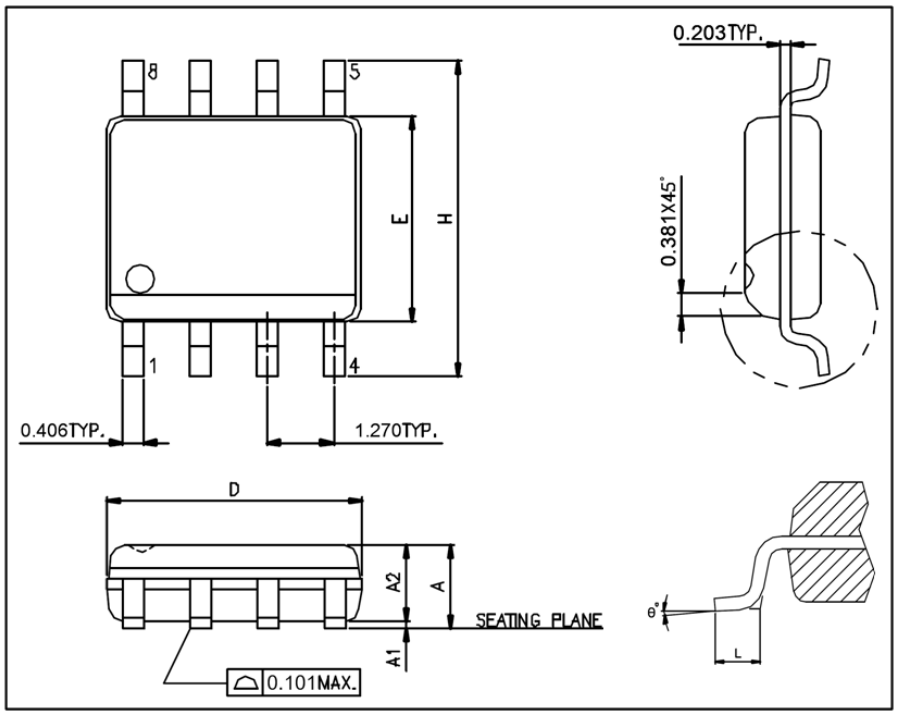


Figure 19

Package Outline

SOP-8L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A 1.346		1.752
A1 0.101		0.254
A2		1.498
D 4.800		4.978
E 3.810		3.987
H 5.791		6.197
L 0.406		1.270
θ° 0°		8°

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.