2 Channel Synchronous Buck PWM Controller

Halogen Free

General Description

The FP5148 is a dual channel synchronous buck switching controller with adjustable over-current protection for DC-DC applications. The FP5148 includes two stage 180° out of phase for driving NMOS, power down under-voltage lockout circuit (UVLO) , the inverting input of amplifier connects to a 0.8V precision reference regulator , short circuit and over current shutdown protection circuit (SCP / OCP)and programmable soft start function.

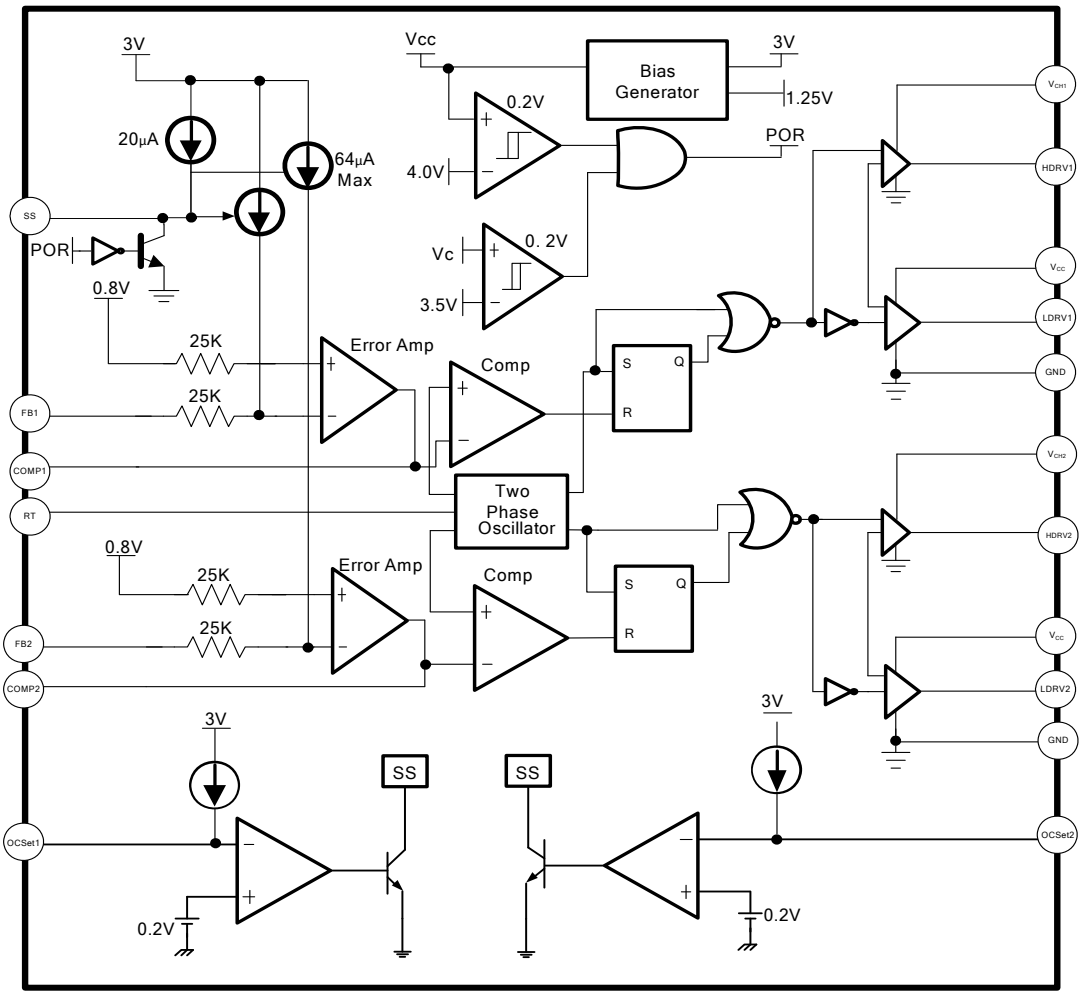
Features

- Wide Supply Voltage Operating Range: 4.2~15V
- Precision Reference Voltage: 0.8V ±2%
- Peak Output Source / Drive Capability: 500mA
- Totem-pole Output for MOS Driving
- Programming Oscillation Frequency
- Programmable Soft Start Function (SS)
- OC/SC Protection Function (OCP / SCP)
- UVLO Protection Function
- Package: SOP-16L, SOP-16L (EP)

Applications

- VGA Card
- Battery Charger
- Hard Disk Drive
- Multi-Output Application

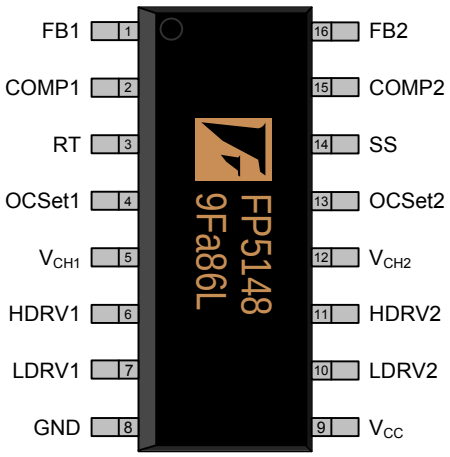
Function Block Diagram



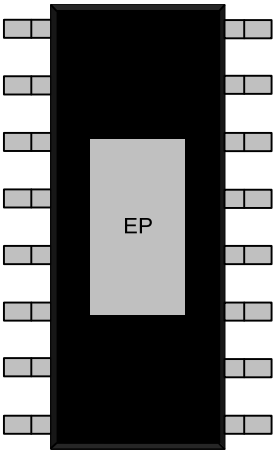
Pin Descriptions

SOP-16L & SOP-16L (EP)

Top View



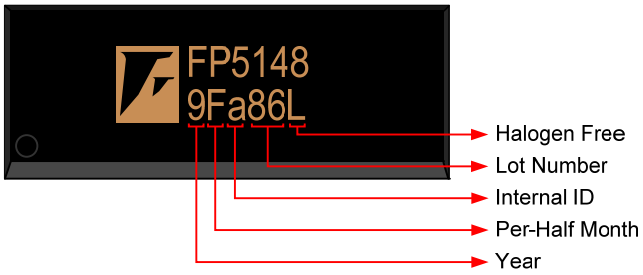
Bottom View



Name	No.	I / O	Description
FB1	1	I	Error Amplifier 1 Inverting Input
COMP1	2	O	Error Amplifier 1 Compensation Output
RT	3	O	Oscillator Resistor
OCSet1	4	I	Over-current Protection 1
V_{CH1}	5	P	Supply Voltage for Output Driver 1
HDRV1	6	O	Output Driver 1 for High Side NMOS
LDRV1	7	O	Output Driver 1 for Low Side NMOS
GND	8	P	IC Ground
V_{CC}	9	P	IC Power Supply
LDRV2	10	O	Output Driver 2 for Low Side NMOS
HDRV2	11	O	Output driver 2 for High Side NMOS
V_{CH2}	12	P	Supply Voltage for Output Driver 2
OCSet2	13	I	Over-current Protection 2
SS	14	I	To Connect a Capacitor for Soft-start
COMP2	15	O	Error Amplifier 2 Compensation Output
FB2	16	I	Error Amplifier 2 Inverting Input
EP	17	P	Exposed PAD - must connect to Ground

Marking Information

SOP-16L & SOP-16L (EP)



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

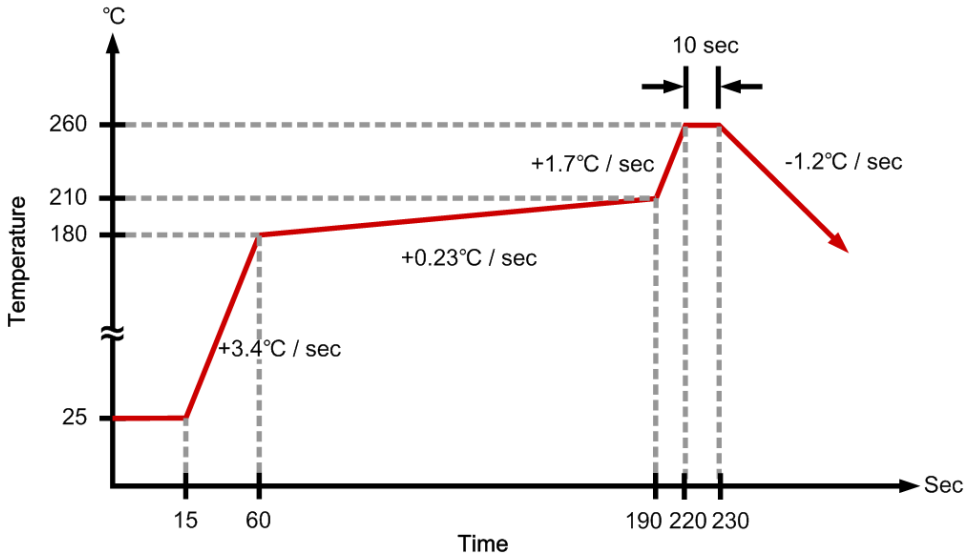
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP5148DR-LF	-10°C ~ +85°C	SOP-16L	2500EA	Tape & Reel
FP5148XR-LF	-10°C ~ +85°C	SOP-16L (EP)	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{IN}				15	V
Power Supply Voltage for High Side Driver		V_{CH1}, V_{CH2}			25	V
Output Source Current					-500	mA
Output Sink Current					500	mA
Allowable Power Dissipation		SOP-16L, $T_A \leqq +25℃$			830	mW
		SOP-16L (EP), $T_A \leqq +25℃$			650	mW
Operating Temperature			-10		+85	℃
Storage Temperature			-55		+125	℃
Operating Junction Temperature Range			+0		+125	℃
Lead Temperature SOP-16L		SOP-16L ,soldering, 10 sec			+260	℃
Lead Temperature SOP-16L (EP)		SOP-16L (EP), soldering, 10 sec			+260	℃

Suggested IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage			4.2		15	V
Operating Temperature			-10		+85	℃

DC Electrical Characteristics (V_{CC}= 5V, V_{CH1}= V_{CH2}=12V, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Under Voltage Lock-Out Section (UVLO)						
UVLO Threshold Voltage	$V_{CC\ (UVLO)}$	Sweep up V_{CC}	4.0	4.2	4.4	V
Hysteresis Voltage	$V_{CC\ (HYS)}$			0.25		V
UVLO Threshold Voltage	$V_{CH1,}V_{CH2}$ (UVLO)	Sweep up $V_{CH1,}V_{CH2}$	3.1	3.3	3.5	V
Hysteresis Voltage	$V_{CH1,}V_{CH2}$ (HYS)			0.25		V
UVLO Threshold Voltage	$V_{FB1,}V_{FB2}$ (UVLO)	Sweep down $V_{FB1,}V_{FB2}$	0.3	0.4	0.5	V
Hysteresis Voltage	$V_{FB1,}V_{FB2}$ (HYS)			0.1		V
Soft Start Section (SS)						
Input Source Current	I_{SS}	V_{SS}=0V	-10	-20	-30	μA
Oscillator Section						
Oscillation Frequency	f	RT=30KΩ	180	200	220	KHz
Frequency Change with Voltage	Δf / ΔV	V_{CC}=5V to 14V V_{CH1}=V_{CH2}=5V to 25V		2	10	%
Frequency change with temperature	Δf / ΔV	T_A = -10℃ to 85℃		5		%
Period Adjustment Section						
Maximum Duty Cycle	$T_{DUTY\ (ON)}$	V_{FB}=0.7V	85	90		%
Minimum Duty Cycle	T_{DUTY} (OFF)	V_{FB}=0.9V	0			%
Total Device Section						
Dynamic V_{CC} Supply Current	$I_{CC\ (DYN)}$	C_L=1500pF	2	5	8	mA
Static V_{CC} Supply Current	I_{CCQ}	V_{SS}=0V	1	3.3	6	mA
Dynamic V_{CH1} Supply Current	$I_{CH1\ (DYN)}$	C_L=1500pF	2	7	10	mA
Static V_{CH1} Supply Current	I_{CH1Q}	V_{SS}=0V	0.5	1	4.5	mA
Dynamic V_{CH2} Supply Current	$I_{CH2\ (DYN)}$	C_L=1500pF	2	7	10	mA
Static V_{CH2} Supply Current	I_{CH2Q}	V_{SS}=0V	0.5	1	4.5	mA

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Error Amplifier Section						
Input Threshold Voltage	V_{FB1},V_{FB2}		0.784	0.8	0.816	V
V_{FB} change with voltage	ΔV_{FB} / ΔV	V_{CC}=5V to 14V		5	20	mV
V_T change with temperature	ΔV_{FB} / ΔT	T_A = -10℃ to 85℃		1		%
Input bias current	I_{FB1}, I_{FB2}	V_{SS}=3V, V_{FB}=1V		-0.1		μA
		V_{SS}=0V, V_{FB}=1V		-64		μA
CH1 Trans-conductance	g_{m1}		450	600	750	μmho
CH2 Trans-conductance	g_{m2}		450	600	750	μmho
Output Section						
Rise Time	T_r	C_L=1500pF		50	100	ns
Fall Time	T_f	C_L=1500pF		50	100	ns
Dead Band Time	T_{db}		50	100	150	ns
Current Limit Section						
OC Threshold Set Current	I_{OCSET}		20	30	40	μA
OC Threshold Voltage	V_{OC}	Sweep down		0.2		V
OC Comp Off-Set Voltage	$V_{OC\ (OFFSET)}$		-5	0	+5	mV

Function Description

Voltage Reference

A 3.0V regulator operating from V_{CC} is used to power the internal circuitry of the FP5148. An internal resistive divider provides 0.8V reference for the error amplifier.

Error Amplifier

The error amplifier compares a sample of the dc-dc converter output voltage with the 0.8V reference and generates an error signal for the error comparator. Output voltage of dc-dc converter is setting with the resistor divider using the following equation (see figure 1):

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 0.8$$

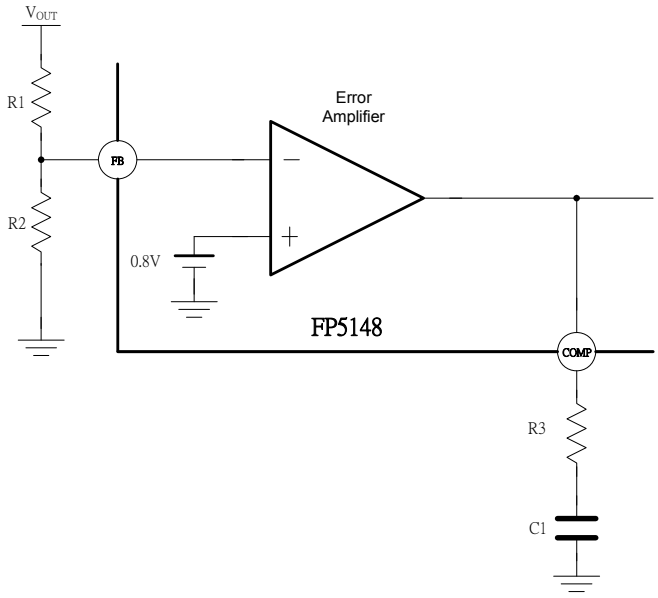


Figure 1 Error Amplifier with Feedback Resistance Divider

Oscillator

The oscillator frequency (fosc) can be set from 20KHz to 500KHz by connecting a resistor RT from RT pin to GND.

$$f = \frac{6000}{RT(K\Omega)} \quad (KHz)$$

Under Voltage Lockout (UVLO)

FP5148 has a different under voltage lockout voltage for V_{CC} (typ. 4.2V) and V_{CH1} / V_{CH2} (typ. 3.3V). The controller starts to work when supply voltage is higher than the lockout point; otherwise the output drivers of FP5148 are turned off.

Soft Start

When the V_{CC} and V_{CH1} / V_{CH2} of FP5148 are ready, the power on reset (POR) signal is turned off. The internal current source (20μA typ.) will charge the external capacitor, which is connected to the soft-start(SS) pin, to about 3V. Also, another internal current source (64μA max.) will control feedback voltage input of error amplifier and enable output driver for soft-start function. The soft-start timing can be decided by following equation:

$$Tss(ms) = 75 \times Css(uF)$$

FP5148 will be shutdown whenever a voltage under 0.5V is forced on soft-start pin.

Short-Circuit Protection

FP5148 will be shutdown immediately whenever COMP voltage is lower than 0.4V. The mean is hard to maintain the output voltage during maximum duty cycle under short-circuit, and the PWM output are off until power restart.

Output Transistor and Boost Voltage V_C

FP5148 uses four NMOS and their turn-on VGS voltage near 4.5V, the source voltage of high side NMOS is near V_{IN}, and it is necessary to supply a boost voltage higher than VIN for high side NMOS gate drive, the following figure explains the relation of MOS gate to source voltage. Application circuits can use different method to solve the boost power supply V_{CH1} / V_{CH2} for high side driver.

(**Recommend boost voltage V_{CH1} / V_{CH2} is the sum of V_{IN} and MOS V_{GS}**)

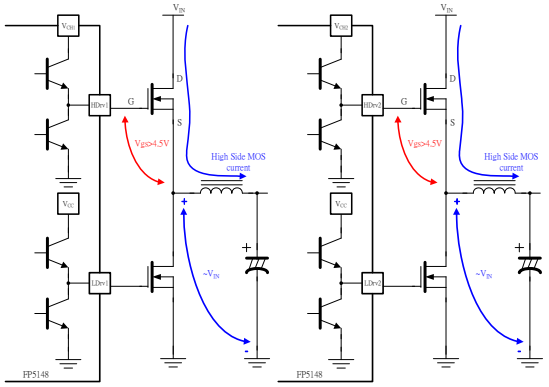
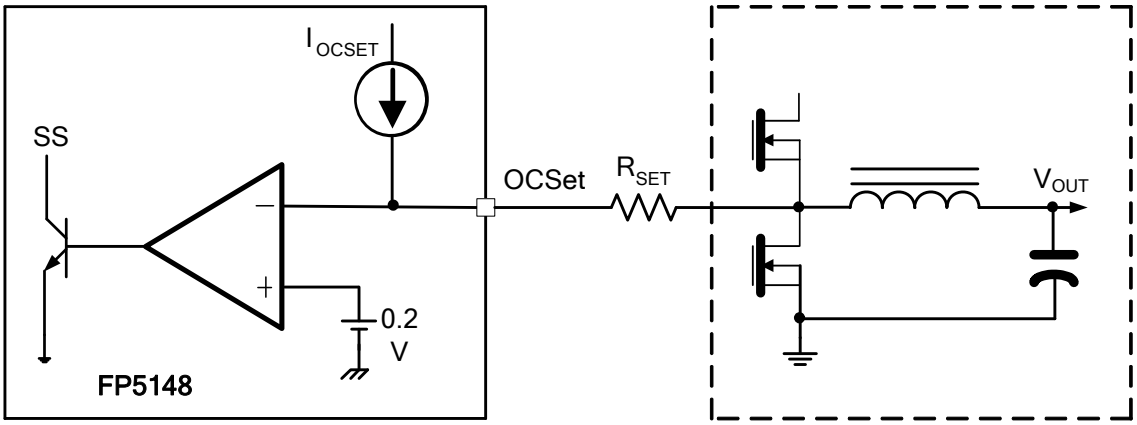


Figure 2 IC Output Stage with NMOS

Over-Current Protection

Over-current protection is achieved with a cycle by cycle scheme. It is performed by sensing current through the $R_{DS(ON)}$ of low side MOSFET. As shown in the figure below, an external resistor R_{SET} is connected between OCSet pin and the drain of low side MOSFET (Q2) to set the current limit point. The internal current source develops a voltage across R_{SET}. When the low side switch is turned on, the inductor current flows through the Q2 and results in a voltage which is given by:

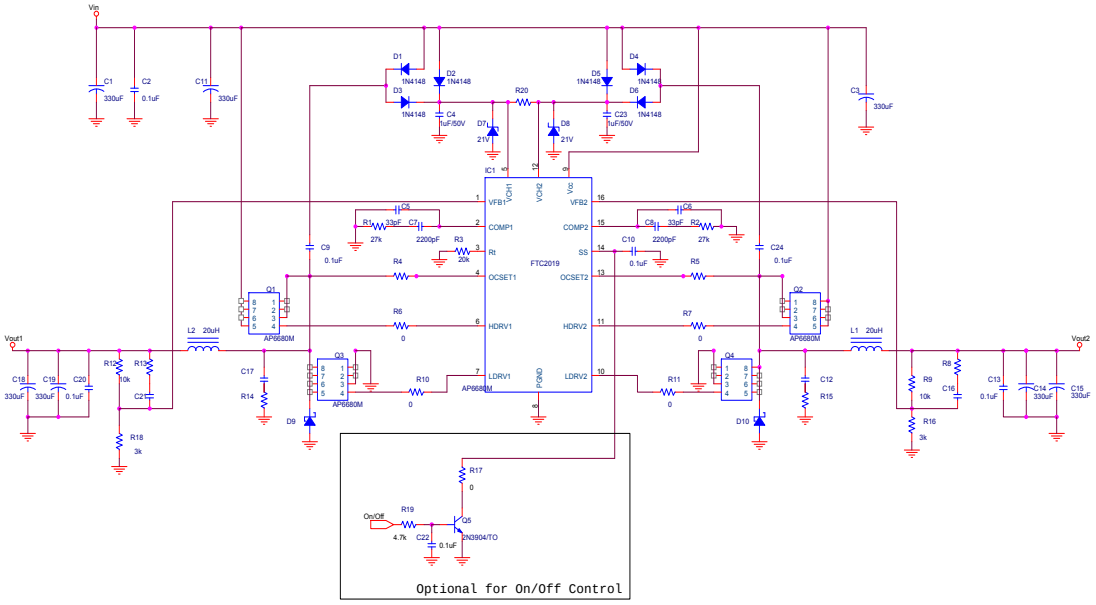


When Voltage V_{OCSET} is below 0.2V, the current sensing comparator flips and pull SS pin low. The high side MOSFET is turned off and the low side MOSFET is turned on until the inductor current reduces to below the over current setting value. The critical inductor current can be calculated by

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times I_L = 0.2$$

$$I_{SET} = I_{L(CRITICAL)} = \frac{R_{SET} \times I_{OCEST} - 0.2}{R_{DS(ON)}}$$

Application Information



Above is a simple application circuit using power supply +5V. The converting voltage is from +5V to +3.3V (dual output) , and V_{CH1} / V_{CH2} pin voltage are high enough to make high side NMOS turn-on.

The output1 voltage is set by following equation:

$$V_{OUT1} = \left(1 + \frac{R12}{R18}\right) \times V_{REF} = \left(1 + \frac{10K}{3K}\right) \times 0.8V = 3.47V$$

The output2 voltage is set by following equation:

$$V_{OUT2} = \left(1 + \frac{R9}{R16}\right) \times V_{REF} = \left(1 + \frac{10K}{3K}\right) \times 0.8V = 3.47V$$

The soft-start time can be calculated by following equation:

$$T_{SS} = 75 \times C10 = 75 \times 0.1(uF) = 7.5ms$$

The over current protection that set by R_{SET} to limit the max inductance current is:

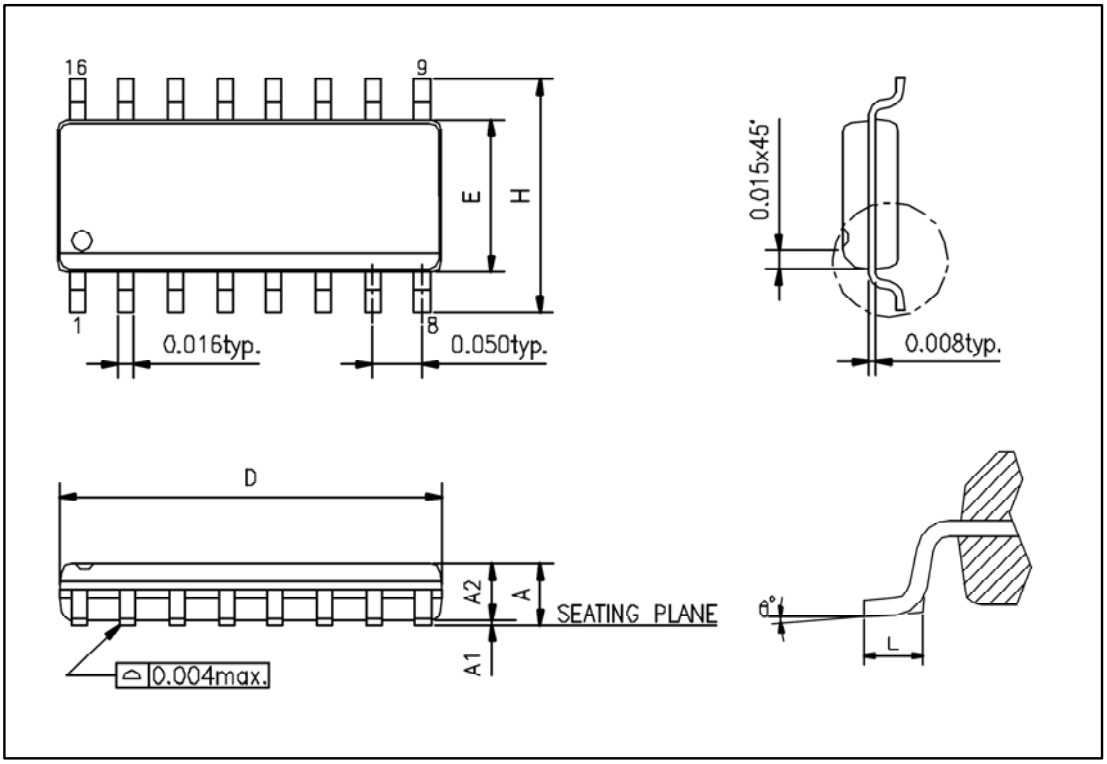
$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times I_L = 0.2$$

$$I_{SET} = I_{L(CRITICAL)} = \frac{R_{SET} \times I_{OCEST} - 0.2}{R_{DS(ON)}}$$

$$I_{SET1} = I_{L(CRITICAL)} = \frac{R4 \times I_{OCSET} - 0.2}{R_{DS(ON)}} \qquad I_{SET2} = I_{L(CRITICAL)} = \frac{R5 \times I_{OCSET} - 0.2}{R_{DS(ON)}}$$

Package Outline

SOP-16L



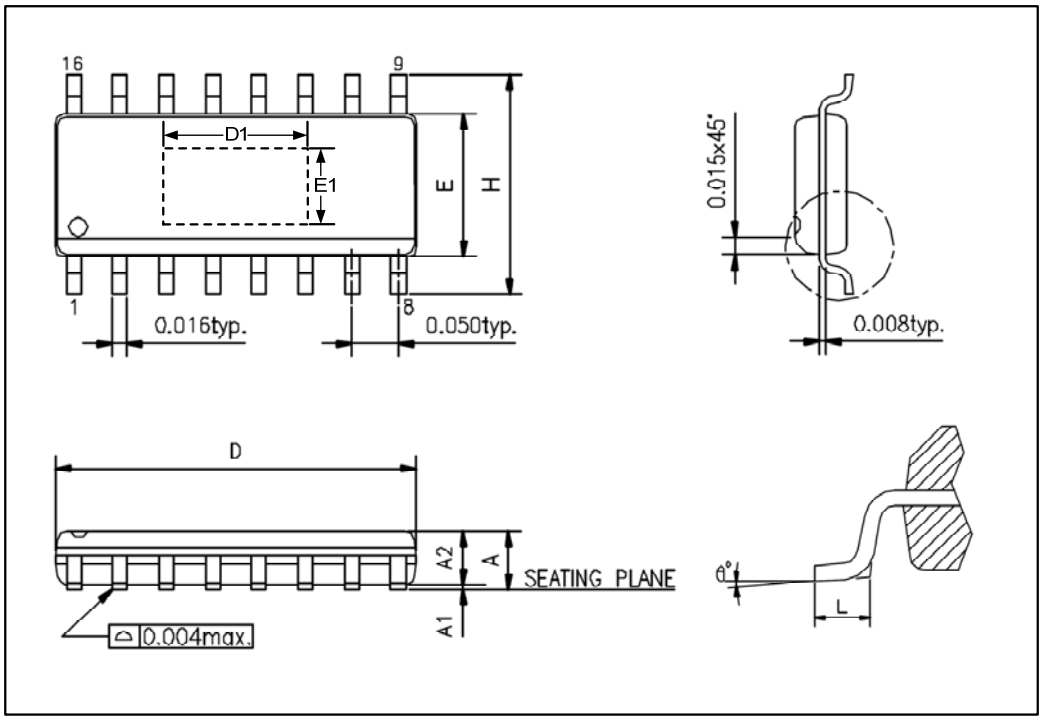
UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2	1.244	1.651
D	9.804	10.007
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AC.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.

SOP-16L (EP)



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E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	2.184 REF	
D1	4.114 REF	

Note:

1. Dimension ”D” does not include molding flash, protrusions or gate burrs.
2. Dimension “E” does not include inter-lead flash or protrusions.