120 mA Current Sinking 10-Bit I²C® DAC

Description:

The FP5503 is a single 10-bit DAC with 120mA output current sink capability. It features an internal reference and operates from a single 2.7 V to 5.5 V supply. The DAC is controlled via a 2-wire (I^2C-compatible) serial interface that operates at clock rates up to 400 kHz, then the DAC control the output sink current from 3mA to 120mA.

The FP5503 incorporates a power-on reset circuit, which ensures that the DAC output powers up to 0 V and remains there until a valid write takes place. It has a power-down feature (external pin power down or the I2C input control software power down) that reduces the current consumption of the device to 1 μA maximum.

The FP5503 is designed for auto-focus, image stabilization, and optical zoom applications in camera phones, digital still cameras, camcorders and other industrial applications.

The FP5503 has many industrial applications, such as controlling temperature (heater or cooler control), light, and movement, over the range −40°C to +85°C without derating.

The I^2C address range for the FP5503 is 0x18 to 0x1F inclusive. Only when the master device initiates the correct address, FP5503 generates an acknowledge condition and works normal.

Features:

- 2.7 V to 5.5 V power supply (or unregulated)
- 120mA current sink
- 2-wire (I^2C®-compatible) serial interface
- 10-bit resolution DAC
- Guaranteed monotonic over all codes
- Fully Integrated:
  1. Integrated current sense resistor (3.3ohms)
  2. Internal reference
  3. Power-on reset
  4. Ultra-low noise preamplifier
  5. Inductive Fly-back Protection diodes
  6. Power-down control circuit
- Power-down current to 0.5uA typical
- small size:1.55mm * 1.55 mm (9-ball WLCSP)
- Available packages:
  1. 9-ball WLCSP
  2. 8-lead TDFN
  3. COB

Consumer Applications:

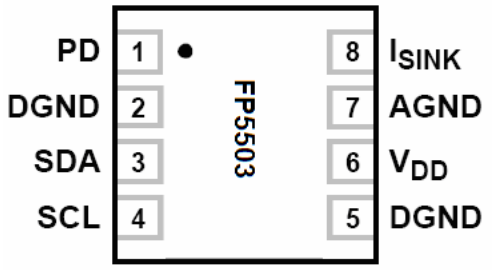
- Lens auto-focus
- Image stabilization
- Optical zoom
- Shutters Iris/exposure
- Neutral density (ND) filters
- Lens covers
- Camera phones Digital still cameras
- Camera modules
- Digital video cameras/camcorders
- Camera-enabled devices
- Security cameras
- Web/PC cameras

Industrial Applications:

- Heater control
- Fan control
- Cooler (Peltier) control
- Solenoid control
- Valve control
- Linear actuator control
- Light control
- Current loop control

Pin Assignments

8-Lead TDFN



9-Ball WLCSP

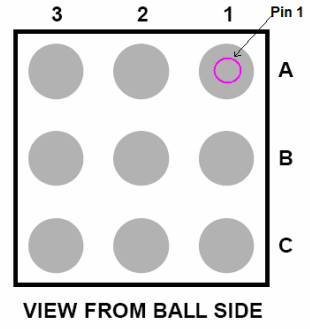


Figure 1. Pin Assignment of FP5503

Ordering Information

FP5503□□□

TR: Tape / Reel
Blank: Tube

P: Pb Free with Commerical Standard (RoHS Compliant)
G: Green Product (for WLCSP)

Package Type
WD: TDFN-8
CP: 9-Ball WLCSP
CH: COB

Part Number	Product Package Option
FP5503-CPG	9-Ball Wafer Level Scale (WLCSP)
FP5503-WDP	8-Lead TDFN
FP5503-CHP	Chip on board

Absolute Maximum Ratings: TA = 25°C, unless otherwise noted.

- V_{DD} to AGND ---------- -0.3V to +6.0V
- V_{DD} to DGND ---------- -0.3V to V_{DD}+0.3V
- AGND to DGND---------- -0.3V to +0.3V
- SCL, SDA to DGND---------- -0.3V to V_{DD}+0.3V
- PD to DGND ---------- -0.3V to V_{DD}+0.3V
- Isink to AGND ---------- -0.3V to V_{DD}+0.3V
- Power Dissipation ------- $(T_{jmax} - T_A)/\theta_{JA}$
- Θ_{JA} Thermal Impedance: ---------- 85°C/W
- Storage Temperature Range---------- - 65°C to +150°C
- ESD (Human Body Model) ---------- 4000 V

**ESD caution: ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.*

Typical Application Circuit:

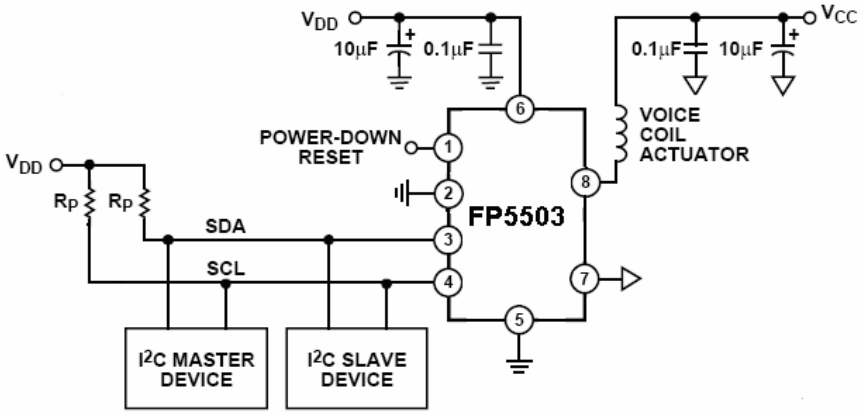


Figure 2. Typical Application Circuit of FP5503

Functional Pin Description:

Pin Name	Pin Number		I/O	Pin Function
	TDFN-8	WLCSP-9		
PD	1	A3	I/O	Power Down, Asynchronous power-down signal. PD is active high.
DGND	2	B2	P	Digital Ground Pin.
SDA	3	B3	I/O	I2C interface data signal
SCL	4	C3	I	I2C interface clock signal
DGND	5	C1	P	Digital Ground Pin.
V_{DD}	6	C2	P	Digital Supply voltage.
AGND	7	B1	P	Analog Ground Pin.
Isink	8	A1	O	Output Current Sink.
N.C	-	A2	-	No Connected.

Block Diagram

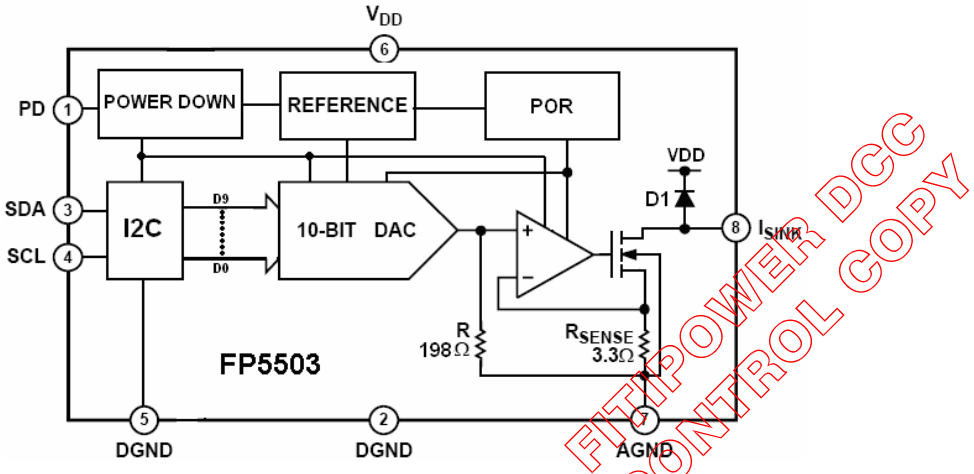


Figure 3. Block Diagram of FP5503

Recommended Operating Conditions:

- Supply Voltage, V_{DD} ---------- 2.7V ~ 5.5V
- Operation Temperature Range ---------- - 40°C to +85°C
- Junction Temperature ---------- +150°C

Electrical Characteristics Specifications:

(Unless otherwise specified, V_{DD}=2.7V to 5.5V, AGND=DGND=0V, load resistance RL=25Ω connected to V_{DD}; all specifications $T_{min.}$ to $T_{max.}$).

AC Specifications:

Parameter	Min.[1]	Typ.[1]	Max.[1]	Unit	Test Conditions/Comments
Output Current Settling Time	-	100	-	uS	V_{DD}=5V, R_L=25Ω, L_L=680uH. 1/4 scale to 3/4 scale change(0x100 to 0x300)
Slew Rate	-	1.5	-	mA/uS	
Major Code Change Glitch Impulse	-	0.15	-	nA-s	1 LSB change around major carry
Digital Feed-through[2]	-	0.06	-	nA-s	

1, Guaranteed by design and characterization; not product tested.

2, See the terminology section.

3, Temperature range is as follows: -40°C to +85°C.

Electrical Characteristics Specifications:

(Unless otherwise specified, V_{DD}=2.7V to 5.5V, AGND=DGND=0V, load resistance RL=25Ω connected to V_{DD}; all specifications $T_{min.}$ to $T_{max.}$).

Parameter	Min.[1]	Typ.[1]	Max.[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	2.7	-	5.5	v	
I_{DD} (Normal Mode) I_{DD} specification is valid for all DAC codes	-	2.5	4	mA	V_{IH}=V_{DD}, V_{IL}=GND, V_{DD}=3.6V, I_{DD} specification is valid for all DAC codes
I_{DD} (Power-Down Mode)	-	0.5	1	uA	V_{IH}=V_{DD}, V_{IL}=GND
DC PERFORMANCE (VDD=3.6V to 4.5V; Operated over 2.7V to 5.5V with reduced performance.)					
Resolution	-	10	-	Bits	117uA/LSB
Relative Accuracy[2]	-	±1.5	±4	LSB	
Differential Nonlinearity[2,3]	-	-	±1	LSB	Guaranteed monotonic over all codes
Zero Code Error[2,4]	0	1	5	mA	All 0s loaded to DAC
Offset Error @Code 16[2]	-	0.5	-	mA	
Gain Error[2]	-	-	±0.6	% of FSR	@25°C
Offset Error Drift[4,5]	-	±10	-	uA/°C	
Gain Error Drift[2,5]	-	±0.2	±0.5	LSB/°C	
LOGIC INPUTS (PD)[5]					
Input Current	-	-	±1	uA	
Input Low Voltage, V_{INL}	-	-	0.8	V	V_{DD}=2.7V to 5.5V
Input High Voltage, V_{INH}	0.7V_{DD}	-	-	V	V_{DD}=2.7V to 5.5V
Pin Capacitance	-	3	-	pF	

Electrical Characteristics Specifications (cont.):

(Unless otherwise specified, V_{DD}=2.7V to 5.5V, AGND=DGND=0V, load resistance RL=25Ω connected to V_{DD}; all specifications $T_{min.}$ to $T_{max.}$).

Parameter	Min.[1]	Typ.[1]	Max.[1]	Unit	Test Conditions/Comments
LOGIC INPUTS (SCL, SDA)[5]					
Input Leakage Current, I_{IN}	-	-	±1	uA	V_{IN}=0V to V_{DD}
Input Low Voltage, V_{INL}	-0.3	-	$0.3V_{DD}$	V	
Input High Voltage, V_{INH}	$0.7V_{DD}$	-	V_{DD}+0.3	V	
Input Hysteresis, V_{HYST}	$0.05V_{DD}$	-	-	V	
Digital Input Capacitance, C_{IN}	-	6	-	pF	
Glitch Rejection[6]	-	-	50	ns	Pulse width of spike suppressed.
OUTPUT CHARACTERISTICS					
Minimum Sink Current[4]	-	3	-	mA	VDD=3.6V to 4.5V; Device operates over 2.7 to 5.5V but specified maximum sink current might not be achieved.
Maximum Sink Current	-	120	-	mA	
Output Current During PD	-	80	-	nA	PD=1
Output Compliance[5]	0.6	-	V_{DD}	V	
Power-up Time	-	20	-	uS	To 10% of FS, coming out of power-down mode; V_{DD}=5V.

1, Temperature range is as follows: -40°C to +85°C.

2, See the terminology section.

3, Linearity is tested using a reduced code range: Codes 32 to 1023.

4, To achieve near zero output current, use the power-down feature.

5, Guaranteed by design and characterization; not product tested. Power Down is active high.

6, Input filtering on both the SCL and SDA inputs suppresses noise spikes that are less than 50ns.

I2C Interface Timing Specification:

(Unless otherwise specified, V_{DD}=2.7V to 5.5V, all specifications $T_{min.}$ to $T_{max.}$).

Parameter[1]	Limit at $T_{min.}$ to $T_{max.}$	Unit	Description
f_{SCL}	400	KHz max.	SCL clock frequency.
t_1	2.5	us min.	SCL cycle time.
t_2	0.6	us min.	t_{HIGH}, SCL high time.
t_3	1.3	us min.	t_{LOW}, SCL lowh time.
t_4	0.6	us min.	$t_{HD,STA}$ start/repeated start condition hold time.
t_5	100	ns min.	$t_{SU,STA}$ data setup time.
t_6[2]	0.9	us max.	$t_{HD,STA}$ data hold time.
	0	us min.	
t_7	0.6	us min.	$t_{SU,STA}$ setup time for repeated start.
t_8	0.6	us min.	$t_{SU,STO}$ stop condition setup time.
t_9	1.3	us min.	t_{BUF}, bus free time between a stop condition and a start condition.
t_{10}	300	ns max.	t_R, rise time of both SCL and SDA when receiving.
	0	ns min.	Maybe CMOS driven.
t_{11}	250	ns max.	t_F, fall time of SDA when receiving.
	300	ns max.	t_F, fall time of both SCL and SDA when transmitting.
	$20+0.1C_b$[3]	ns min.	
C_b	400	pF max.	Capacitive load for each bus line.

1, Guaranteed by design and characterization; not product tested.

2, A master device must provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IN,MIN}$ of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

3, C_b is the total capacitance of one bus line in pF. t_R and t_F are measured between $0.3V_{DD}$ and $0.7V_{DD}$.

I2C 2-Wire Serial Interface Timing Diagram:

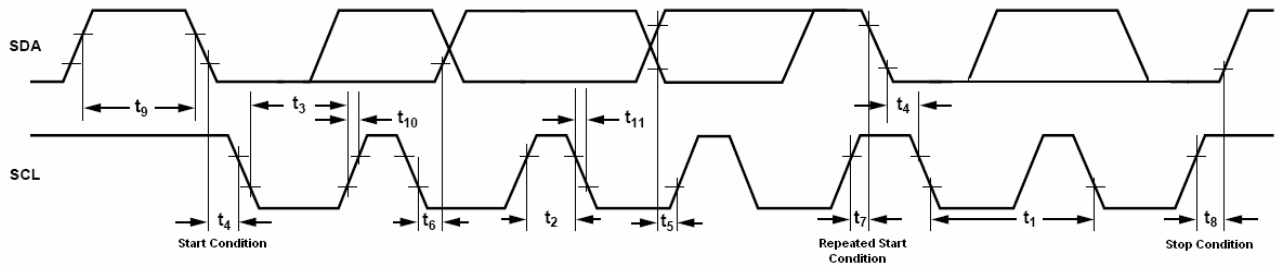


Figure 4, 2-wire serial interface timing diagram

Typical Performance Characteristics:

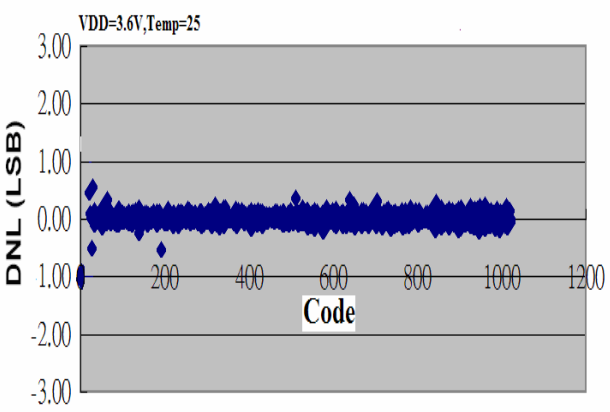


Figure 5. Typical DNL Plot

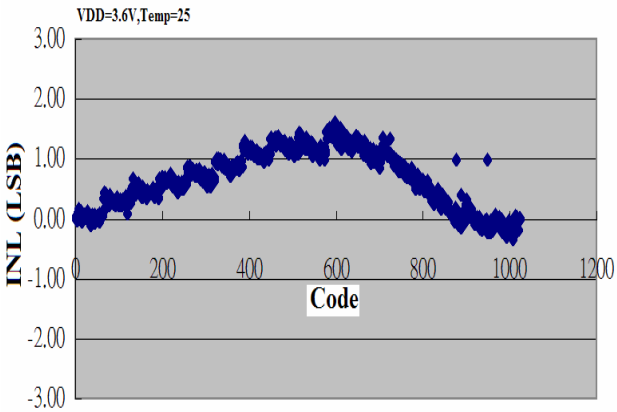


Figure 6. Typical INL Plot

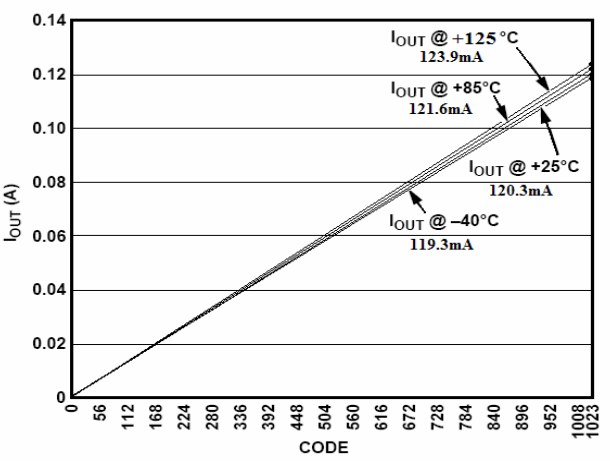


Figure 7. Sink Current vs. Code vs. Temperature (VDD=3.6V)

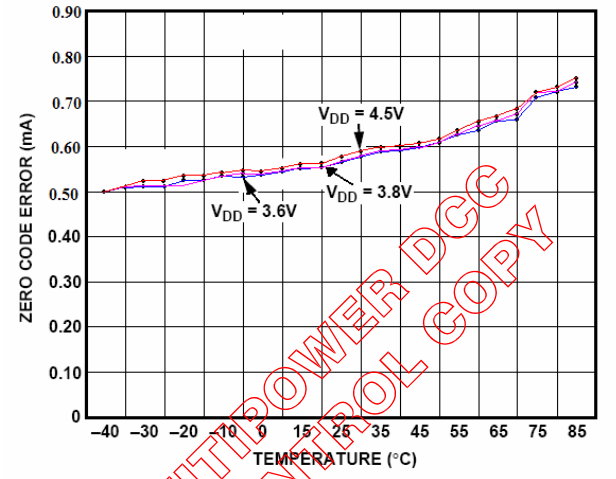


Figure 8. Zero Code Error vs. Supply Voltage vs. Temperature

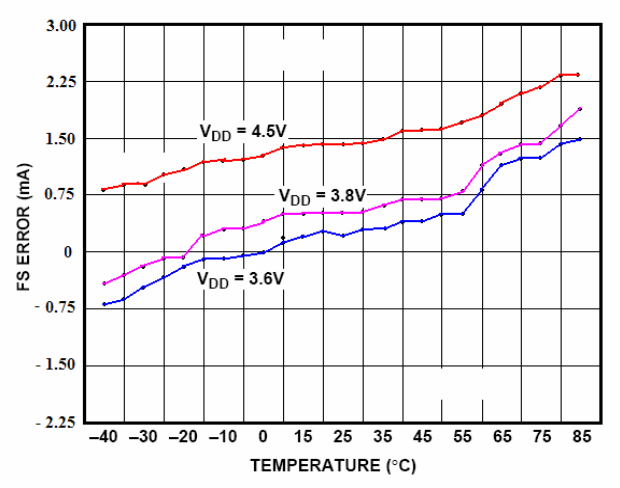


Figure 9. Full-scale Error vs. Temperature vs. Supply

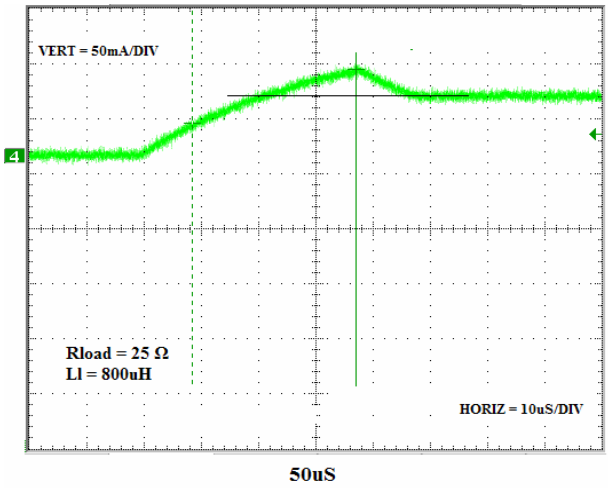


Figure 10. Settling Time for Full Swing
(From 0.25 scale to 0.75 scale, VDD=3.6V)

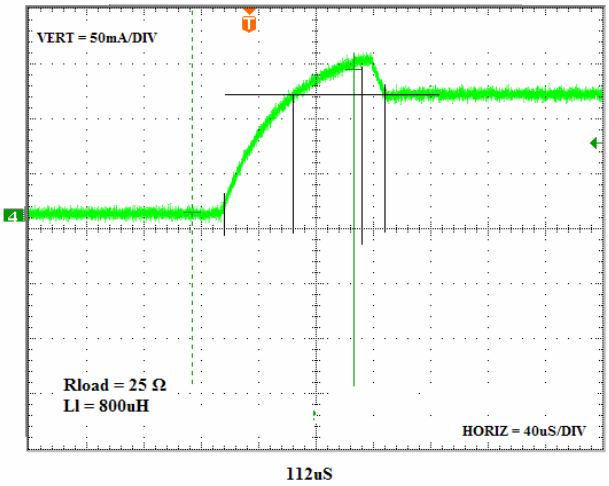


Figure 11. Settling Time for Full Swing
(From 0 scale to 1 scale, VDD=3.6V)

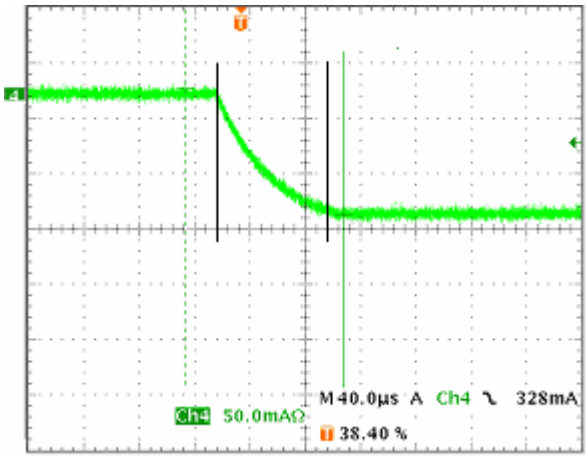


Figure 12. Isink Power-down (soft power-down or hardware pin power-down)

TERMINOLOGY:

Resolution

For the DAC, the resolution is defined by the number of distinct analog levels corresponding to the number of bits it uses. N-bit resolution -> 2^N distinct analog levels.

Sink Current

Sink current is the input current driven by the power MOS embedded in the FP5503.

Relative Accuracy (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error

Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 mA. The zero-code error is always positive in the FP5503 because the output of the DAC cannot go below 0 mA. This is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mA.

Gain Error

This is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percent of the full-scale range.

Gain Error Drift

This is a measurement of the change in gain error with changes in temperature. It is expressed in LSB/°C.

Digital to Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nA-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feed-through

Digital feed-through is a measurement of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nA-s and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Offset Error

Offset error is a measurement of the difference between ISINK (actual) and IOUT (ideal) in the linear region of the transfer function, expressed in mA. Offset error is measured on the FP5503 with Code 16 loaded into the DAC register.

Offset Error Drift

This is a measurement of the change in offset error with a change in temperature. It is expressed in μV/°C.

Theory of Operation:

The FP5503 is a fully integrated 10-bit DAC with 120 mA output current sink capability and is intended for driving voice coil actuators in applications such as lens auto-focus, image stabilization, and optical zoom. The circuit diagram is shown in Figure 3. A 10-bit current output DAC coupled with Resistor R generates the voltage that drives the non-inverting input of the operational amplifier. This voltage also appears across the R_{SENSE} resistor and generates the sink current required to drive the voice coil.

Resistors R and R_{SENSE} are interleaved and matched. Therefore, the temperature coefficient and any non-linearities over temperature are matched and the output drift over temperature is minimized. Diode D1 provides output protection, and dissipates the energy stored in the voice coil when the device is powered down.

SERIAL INTERFACE

The FP5503 is controlled using the industry-standard I2C 2-wire serial protocol. Data can be written to or read from the DAC at data rates up to 400 kHz. After a read operation, the contents of the input register are reset to all zeros.

I2C BUS OPERATION

An I2C bus operates with one or more master devices that generate the serial clock (SCL), and read/write data on the serial data line (SDA) to/from slave devices such as the FP5503. All devices on an I2C bus have their SCL pin connected to the SDA line and their SCL pin connected to the SCL line. I2C devices can only pull the bus lines low; pulling high is achieved by pull-up resistors R_P. The value of R_P depends on the data rate, bus capacitance, and the maximum load current that the I2C device can sink (3 mA for a standard device).

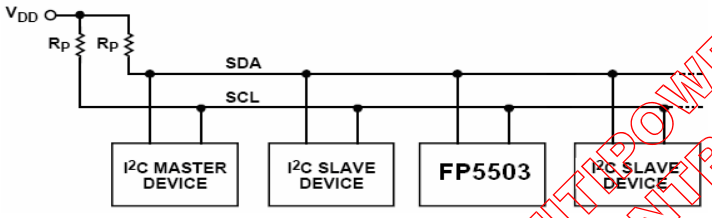


Figure 13, Typical I2C Bus

When the bus is idle, SCL and SDA are both high. The master device initiates a serial bus operation by generating a start condition, which is defined as a high-to-low transition on the SDA low while SCL is high. The slave device connected to the bus

responds to the start condition and shifts in the next eight data bits under control of the serial clock. These eight data bits consist of a 7-bit address, plus a read/write bit, which is 0 if data is to be written to a device, and 1 if data is to be read from a device. Each slave device on an I2C bus must have a unique address. The address of the FP5503 is 0001100; however, 0001101, 0001110, and 0001111 address the part because the last two bits are unused/don't care (see Figure 6 and Figure 7). Since the address plus R/W bit always equals eight bits of data, another way of looking at it is that the write address of the FP5503 is 0001 1000 (0x18) and the read address is 0001 1001 (0x19). Again, Bit 6 and Bit 7 of the address are unused, and therefore the write addresses can also be 0x1A, 0x1C, and 0x1E, and the read address can be 0x1B, 0x1D, and 0x1F (see Figure 6 and Figure 7).

At the end of the address data, after the R/W bit, the slave device that recognizes its own address responds by generating an acknowledge (ACK) condition. This is defined as the slave device pulling SDA low while SCL is low before the ninth clock pulse, and keeping it low during the ninth clock pulse. Upon receiving ACK, the master device can clock data into the FP5503 in a write operation, or it can clock it out in a read operation. Data must change either during the low period of the clock, because SDA transitions during the high period define a start condition as described previously, or during a stop condition as described in the Data Format section.

I2C data is divided into blocks of eight bits, and the slave generates an ACK at the end of each block. Since the FP5503 requires 10 bits of data, two data-words must be written to it when a write operation occurs, or read from it when a read operation occurs. At the end of a read or write operation, the FP5503 acknowledges the second data byte. The master generates a stop condition, defined as a low-to-high transition on SDA while SCL is high, to end the transaction.

DATA FORMAT

Data is written to the FP5503 high byte first, MSB first, and is shifted into the 16-bit input register. After all data is shifted in, data from the input register is transferred to the DAC register.

Because the DAC requires only 10 bits of data, not all bits of the input register data are used. The MSB is reserved for an active-high, software-controlled, power-down function. Bit 14 is unused; Bit 13 to Bit 4 corresponds to the DAC data bits, Bit 9 to Bit 0. Bit 3 to Bit 0 are unused. During a read operation, data is read in the same bit order.

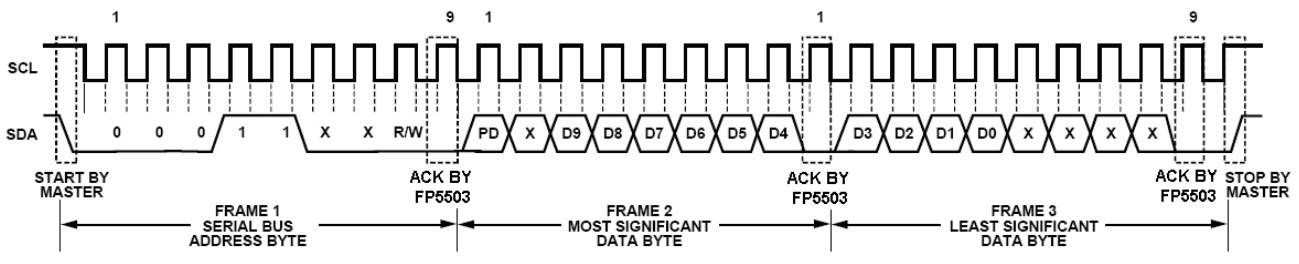


Figure 14, Write Operation

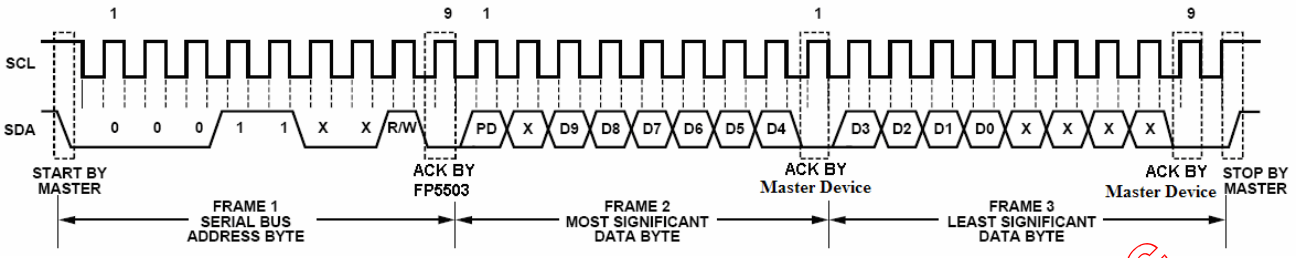


Figure 15, Read Operation

Serial Data-Words	High Byte								Low Byte							
Serial Data Bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Input Register	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Function	PD	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

1, PD=soft power-down; X=unused/don't care; D9 to D0=DAC data.

Figure 16, DATA Format[1]

Application Note:

Power Supply Bypassing and Grounding:

When accuracy is important in an application, it is beneficial to consider power supply and ground return layout on the PCB. The PCB for the FP5503 should have separate analog and digital power supply sections. Where shared AGND and DGND is necessary, the connection of grounds should be made at only one point, as close as possible to the FP5503.

Special attention should be paid to the layout of the AGND return path and track between the VCM (voice coil motor) and I_{SINK} to minimize any series resistance. Figure 17 shows the output current sink of the FP5503 and illustrates the importance of reducing the effective series impedance of AGND, and the track resistance between the motor and ISINK. The VCM is modeled as inductor LC and resistor RC. The current through the VCM is effectively a dc current that results in a voltage drop, V_C, when the FP5503 is sinking current; the effect of any series inductance is minimal. The maximum voltage drop allowed across R_{SENSE} is 400 mV, and the minimum drain to source voltage of PM1 is 200 mV. This means that the FP5503 output has a compliance voltage of 600 mV. If V_{DROP} falls below 600 mV, the output transistor, PM1, can no longer operate properly and I_{SINK} might not be maintained as a constant.

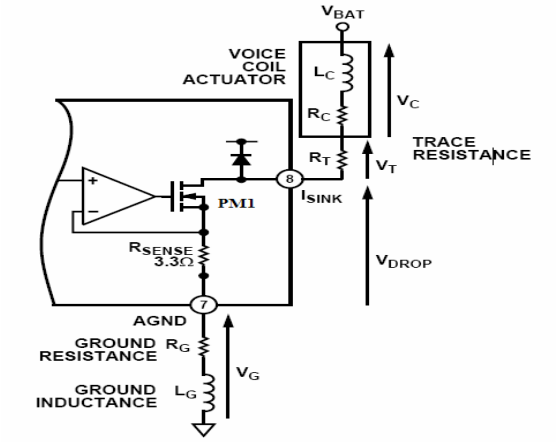


Figure 17, Effect of PCB Trace Resistance and Inductance

As the current increases through the voice coil, V_C increases and V_{DROP} decreases and eventually approaches the minimum specified compliance voltage of 600 mV. The ground return path is modeled by the components R_G and L_G. The track resistance between the voice coil and the FP5503 is modeled as R_T. The inductive effects of L_G influence R_{SENSE} and R_C equally, and because the current is maintained as a constant, it is not as critical as the purely resistive component of the ground return path. When the maximum sink current is flowing through the motor, the resistive elements, R_T and R_G, might have an impact on the voltage headroom of PM1 and could, in turn, limit the maximum value of R_C because of voltage compliance.

For example:

V_{BAT} = 3.6 V, R_G = 0.5 Ω, R_T = 0.5 Ω, I_{SINK} = 120 mA, V_{DROP} = 600 mV (the compliance voltage)

Then the largest value of resistance of the voice coil, R_C, is

$$R_C = \frac{V_{BAT} - [V_{DROP} + (I_{SINK} \times R_T) + (I_{SINK} \times R_G)]}{I_{SINK}}$$

$$\frac{3.6\ \text{V} - [600\ \text{mV} + 2 \times (120\ \text{mA} \times 0.5\ \Omega)]}{120\ \text{mA}} = 24\ \Omega$$

For this reason it is important to minimize any series impedance on both the ground return path and interconnect between the

FP5503 and the motor. The power supply of the FP5503 should be decoupled with 0.1μF and 10μF capacitors. These capacitors should be kept as physically close as possible, with the 0.1μF capacitor serving as a local bypass capacitor, and therefore should be located as close as possible to the V_{DD} pin. The 10μF capacitor should be a tantalum bead-type; the 0.1μF capacitor should be a ceramic type with a low effective series resistance and effective series inductance. The 0.1μF capacitor provides a low impedance path to ground for high transient currents.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feed-through effects through the board. The best board layout technique is to use a multilayer board with ground and power planes, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

The exposed paddle on the FP5503 should be soldered to ground to ensure the best possible thermal performance. The thermal impedance of the FP5503 TDFN package is 85°C/W when soldered in a 2-layer board. It is defined in the Absolute Maximum Ratings section.

Application Circuit:

The FP5503 is designed to drive both spring preloaded and non-spring linear motors used in applications such as lens auto-focus, image stabilization, or optical zoom. The operation principle of the spring-preloaded motor is that the lens position is controlled by the balancing of a voice coil and spring. Figure 18 shows the transfer curve of a typical spring preloaded linear motor for auto-focus. The key points of this transfer function are displacement or stroke, which is the actual distance the lens moves in mm, and the current through the motor in mA.

A start current is associated with spring-preloaded linear motors, which is effectively a threshold current that must be exceeded for any displacement in the lens to occur. The start current is usually 20mA or greater; the rated stroke or displacement is usually 0.25 mm to 0.4 mm; and the slope of the transfer curve is approximately 10μm/mA or less.

The FP5503 is designed to sink up to 120mA, which is more than adequate for available commercial linear motors or voice coils. Another factor that makes the FP5503 the ideal solution for these applications is the monotonicity of the device, which ensures that lens positioning is repeatable for the application of a given digital word. The Fig. 23 shows a typical application circuit for the FP5503.

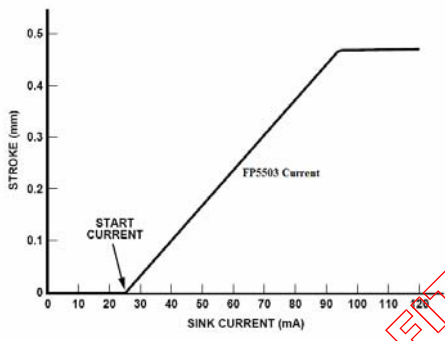


Figure 18, Spring Preloaded Voice Coil Stroke vs. Sink Current

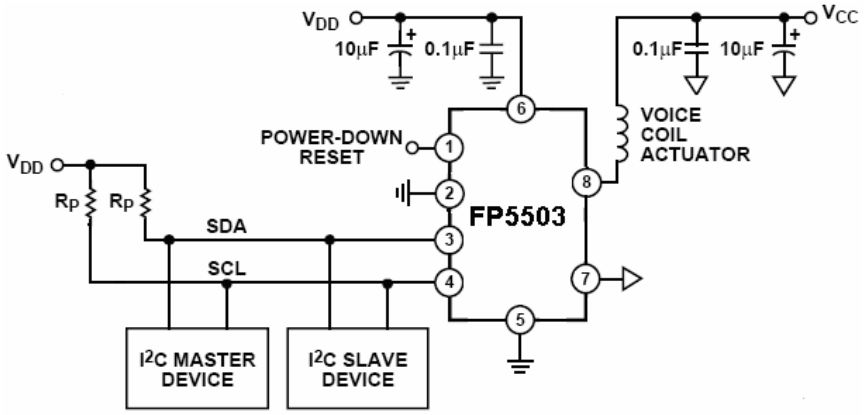


Figure 19, Typical Application Circuit

Output Current Calculations:

In figure 3, Resistors R and RSENSE are interleaved and matched on-chip. Their temperature coefficients and any nonlinearities over temperature are therefore matched, minimizing the output drift over temperature. Diode D1 provides output protection, and dissipates the energy stored in the voice coil when the device is powered down. From the figure 4, the output current can be calculated as following example.

1), 10-bit DAC resolution:

D0~D9, are used for VCM constant current control via the I2C serial data lines, SDA and SCL.

For example: R_{SENS} = 3.3Ω, the full scale voltage of R_{SENS} drop is 400mV and the Zero Code Error (I_{ZEC}) is 5mA. The LSB driving current of VCM is

$$LSB = (Vdrop – 5mA*3.3Ω)/(2^{10}*3.3Ω) = 113.6uA$$

If the input digital code is 1000000000, the driving current of VCM (I_{SINK}) is

$$I_{SINK} = I_{ZEC} + Code*LSB = 5mA + 2^{9}*113.6uA = 63.16mA$$

2), 8-bit DAC resolution:

The FP5503 can also be used as n-bit resolution (n is less than 10). For 8-bit application, DAC data, D1 and D0 are set to logic 0 only. There are 8-bit DAC data, D9~D2, are used for VCM constant current control via the two I2C serial data lines, SCL and SDA.

For example: R_{SENS} = 3.3Ω, the full scale voltage of R_{SENS} drop is 400mV and the Zero Code Error (I_{ZEC}) is 5mA. The LSB driving current of VCM is

$$LSB = (Vdrop – 5mA*3.3Ω)/(2^{8}*3.3Ω) = 455.73uA$$

If the input digital code is 10000000(D9~D2 can be programmable, and the D1~D0 are forced to logic 0), the driving current of VCM (I_{SINK}) is

$$I_{SINK} = I_{ZEC} + Code*LSB = 5mA + 2^{7}*455.73uA = 62.878mA$$

WLCSP (Wafer Level Scale) Package Application:

CSP Description:

Chip Scale Packages are defined as any package whose dimensions are no more than 20% larger than the die or chip that it contains. The Chip Scale Package represents the smallest possible footprint size in that the package is the same size as the die.

PCB Circuit Board Recommendations:

A summary of recommended PCB design parameters is shown in Table 1. Non-Solder mask defined (NSMD) pads are

preferable, because the solder spheres will encompass the pad periphery wall as well as the pad surface, thereby providing extra strength for added solder joint integrity and better reliability.

Printed Circuit Board (PCB) Surface Finish Characteristics:

Organic Solder ability Preservative (OSP) finish recommended. Electronless nickel-immersion gold finish with gold thickness ranging from 0.05 microns to 0.127 microns may also be used. Because the PCB pad layout is critical to solder ball type package's board level reliability, the PCB pad layout must match to WLCSP's ball size.

Table 1: PC Board Recommendations

Parameter	0.5mm Pitch 0.3mm Ball	0.65mm Pitch 0.35mm Ball
Pad size in PCB	0.275mm	0.300mm
Pad Shape	Round	Round
Pad Definition	Non Solder Mask Defined Pads	Non Solder Mask Defined Pads
Solder Mask Opening	0.325mm Round	0.350mm Round
Solder Stencil Thickness	0.125 - 0.150mm	0.125 - 0.150mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.330mm Round	0.360mm Round
Solder Flux Ratio	50/50 By Volume	50/50 By Volume
Solder Paste Type	No Clean	No Clean
Bond Trace Finish	OSP (Entek Cu Plus 106A)	OSP (Entek Cu Plus 106A)
Tolerance –edge to corner ball	±50µm	±50µm
Solder ball side coplanarity	±20µm	±20µm

Reflow Recommendations:

Reflow can be accomplished using Forced Convection (Convection Dominant) and Convection/IR ovens as well as with Vapor Phase and Area Conduction systems. The Ramp or Tent profile (Figure 20) is recommended for reflow of most assemblies as it is compatible with most No-Clean, RMA and OA solder paste formulations on the market. For more complex, higher mass assemblies the "Ramp-Soak-Spike" profile (Figure 21) might be required but users of OA solder pastes with Forced Convection (Convection Dominant) ovens should be careful to avoid flux dry-out. Consult solder paste manufactures specifications. The illustrated Ramp and Ramp-Soak-Spike profiles are for use with Sn63/Pb37 and Sn62/Pb36/Ag2 solder paste alloys and will serve as a general guideline in establishing a reflow profile (Figure 22) for the users process. Adjustments will be necessary for use with other solder paste alloys, especially lead-free compositions. Various PCBA geometries, densities, and oven types may require further profile adjustments.

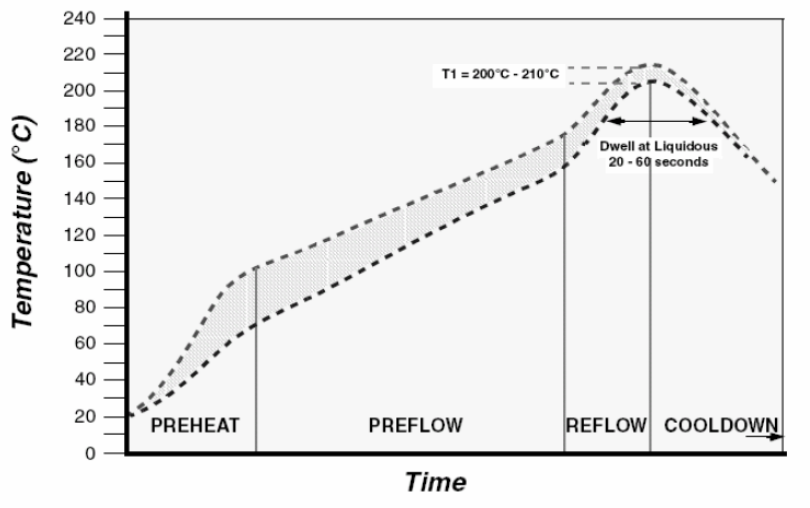


Figure 20, Eutectic Ramp or Tent Reflow Profile

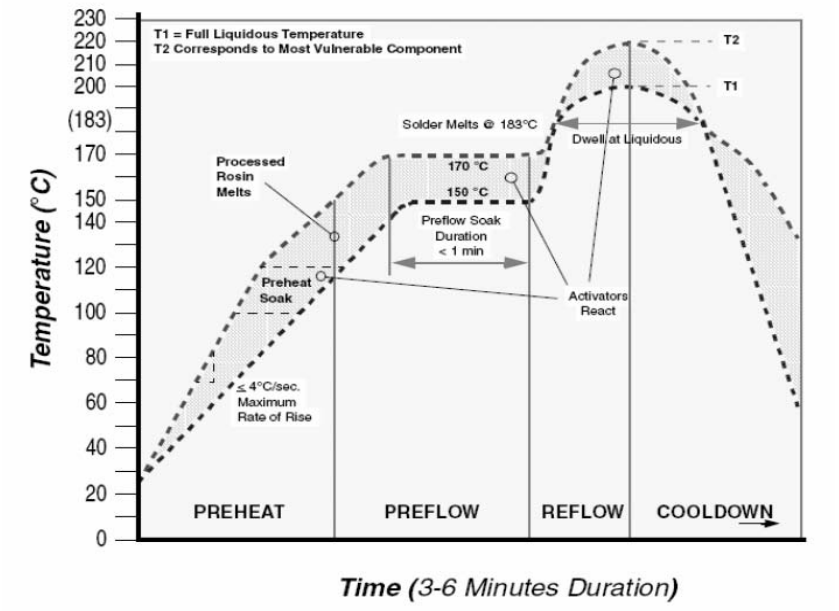


Figure 21, Ramp-Soak-Spike Profile

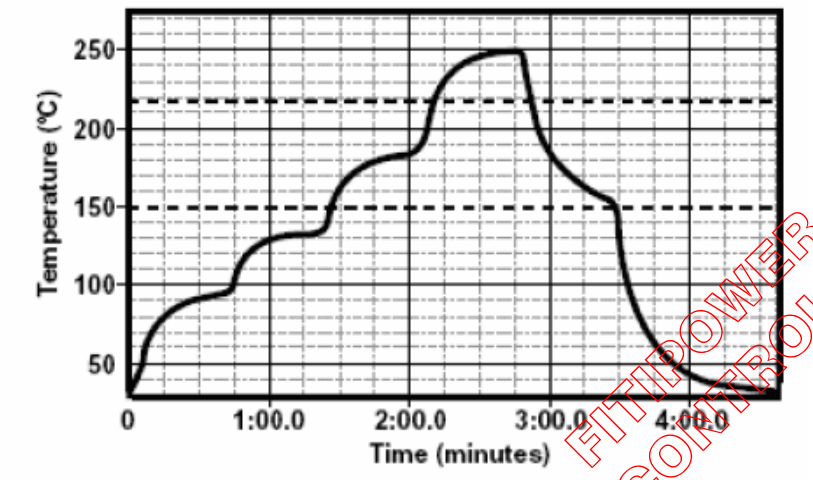


Figure 22, Reflow profile of Lead-free solder ball

Rework:

CSP devices offer great advantages to system designers due to their fine pitch and small footprint. There same characteristics make their rework more challenging. The rework process begins with the removal of the component. During this process, heat is applied to effect melting of the solder joints to that the part can be lifted from the board. Thermal profiles should be designed to match the solder paste characteristics closely. Large area bottom side pre-heaters (typically convection or infrared) are used to raise the temperature of the board. This eliminates warpage of the board and minimizes the amount of heat that must be applied directly to the component.

Top heating is applied to the component typically through a convective hot gas muzzle. Nozzle size should be selected to match the component footprint appropriately. Thermocouples or sensors at the rework location can be used to monitor the thermal conditions. After top heating has melted the solder, vacuum is applied through the pick-up muzzle, and the component is lifted from the board.

It is important that the heat is directed to the component to be removed and that adjacent components are prevented from reflowing their solder joints. For this concern, the use of shielding , control of the gas flow from the nozzle, and accurate temperature control are the most important factors to consider.

Next, the worksite must be cleaned of solder. Due to space constraints and the need for accurate temperature control, automatic tools are recommended. Typical, site scavenger consisting of controlled non-contact gas heating and vacuuming tools are used to clean the site in preparation for reapplication of a replacement component. For this operation, the goal is to remove the residual solder from the site without damaging the pads, solder mask, or adjacent components, and to prepare the site for application of a new component. While utilization of a mini-stencil and solder paste is theoretically possible, from a practical point of view their use is often difficult or impossible due to space constraints, small footprints, tight dimensions and the close proximity of neighboring components.

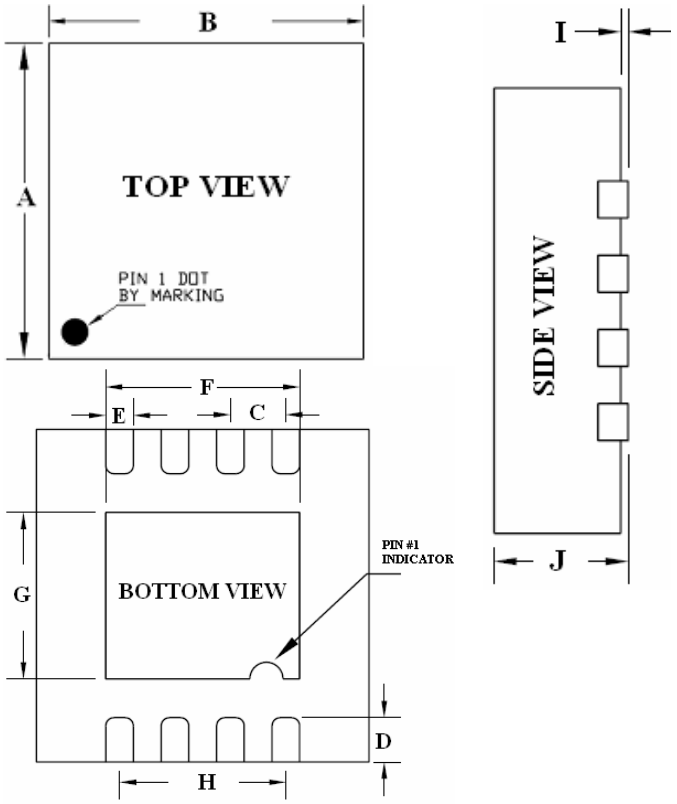
Sophisticated rework systems can dip the part in No-Clean flux, eliminating the need for a repair stencil and cleaning, and can place the part accurately, reflowing the solder joint be applying controlled heat to the component in much the same way as described for removal above. Systems are available at various levels of automation. If more manual techniques are employed, the use of soldering irons and tweezers should be avoided to be extent possible, it is advisable that the more manual approaches utilize the methodologies and techniques employed by more sophisticated automatic systems.

Under-Fill Free Excellence:

The WLCSP package has perfect solder ball reliability, so the WLCSP package needs no dispensing under-fill. But normal flip chip package must dispense under-fill.

Outline Information:

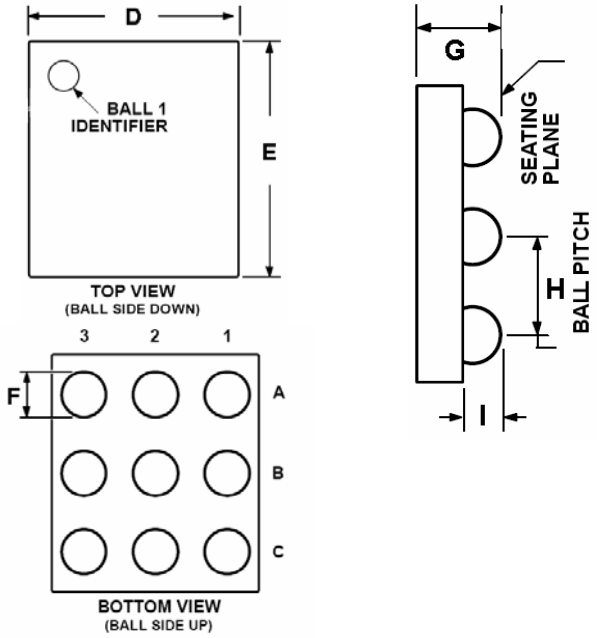
TDFN-8 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION MILLIMETER		
	MIN.	NOM.	MAX.
A	2.95	3.00	3.05
B	2.95	3.00	3.05
C		0.50 BASIC	
D	0.35	0.40	0.45
E	0.18	0.25	0.30
F	2.35	2.4	2.45
G	1.45	1.50	1.55
H		1.50 REF	
I		0.05 REF	
J	0.70	0.75	0.80

Note 1：Followed From JEDEC MO-229-0.

9-Ball WLCSP Package (Unit: mm)



SYMBOLS UNIT	DIMENSION MILLIMETER		
	MIN.	NOM.	MAX.
D	1.490	1.550	1.610
E	1.490	1.550	1.610
F	0.300	0.320	0.340
G	0.590	0.650	0.710
H		0.500 Basic	
I	0.215	0.235	0.255

Note 1：Followed From JEDEC MO-211.

Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.