2A Ultra Low Dropout Linear Regulator

Description

The FP6145B is a 2A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, control voltage for the circuitry and main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The FP6145B integrates many functions. Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. Thermal shutdown and current limit functions protect the device against thermal and current over-loads. POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The FP6145B can be enabled by other power system. Pulling and holding the EN pin below 0.4V shuts off the output.

The FP6145B is available in SOP-8 (EP) package which features small size as an exposed pad to reduce the junction-to-case resistance.

Features

- Ultra Low Dropout - 0.24V(typ.) at 2A Output Current
- Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable
- 0.8V Reference Voltage
- Fast Transient Response
- Adjustable Output Voltage by External Resistors
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Under-Voltage Protection
- Current-Limit and Thermal Shutdown Protection
- Power-OK Output with a Delay Time
- SOP-8 Exposed Pad Green Package

Applications

- LCD Monitor/TV
- PC Motherboard/NB
- Graphic Card
- DVD-Video Player
- ADSL Modem
- Printer and other Peripheral Equipment

Pin Assignment

SP Package (SOP-8 Exposed Pad)

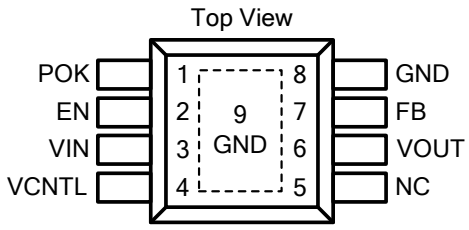
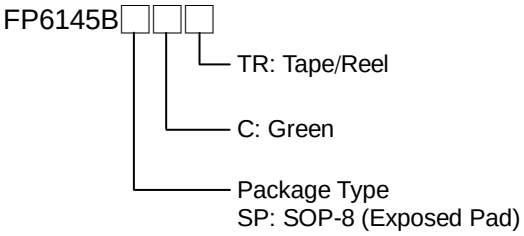


Figure1. Pin Assignment of FP6145B

Ordering Information



Typical Application Circuit

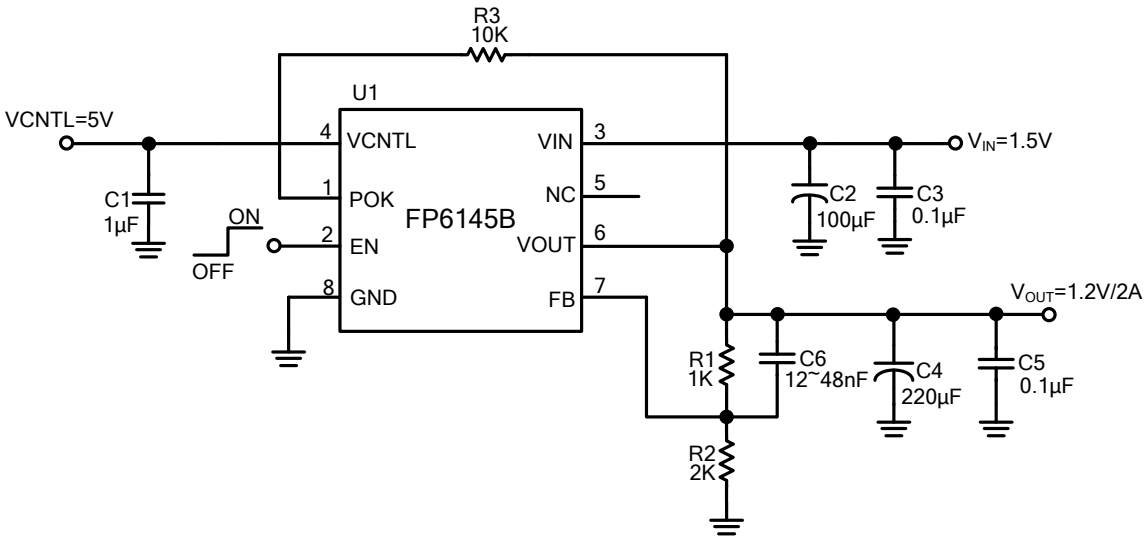


Figure 2. an EC as a Main Output Capacitor

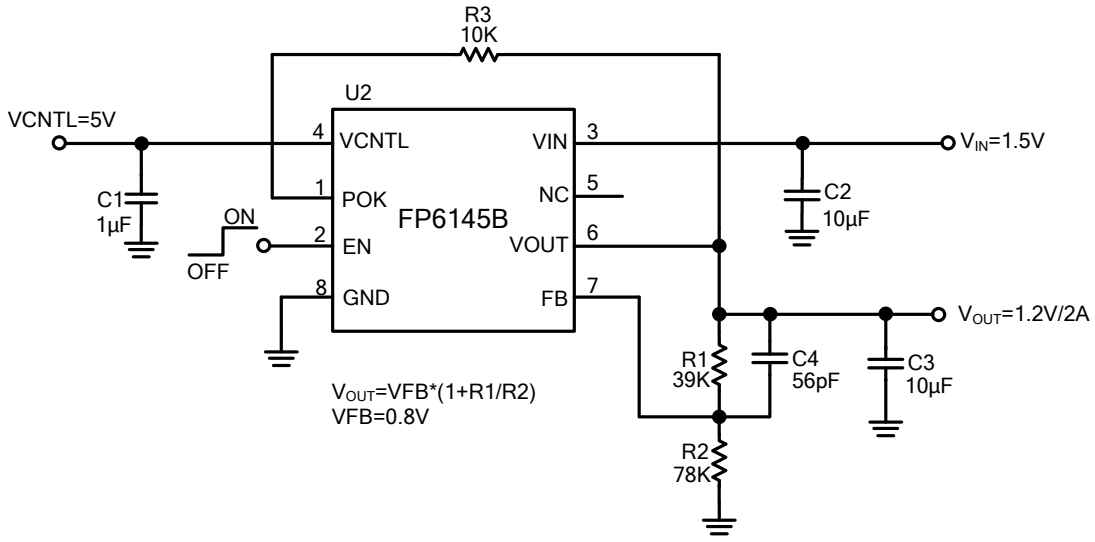


Figure 3. Using a MLCC as the Output Capacitor

Functional Pin Description

Pin Name	Pin No.	Pin Function
POK	**1**	Power OK output pin.
EN	**2**	Internal pull high. EN=High or Floating → Enable. EN=Low → Shutdown mode.
VIN	**3**	MOSFET power supply input pin.
VCNTL	**4**	Input pin for internal control circuitry.
NC	**5**	No connection.
VOUT	**6**	Output pin of the regulator.
FB	**7**	Output voltage feedback pin.
GND	**8**	GND pin.
Exposed Pad	**9**	Thermal dissipation pad. Connect exposed pad to GND.

Block Diagram

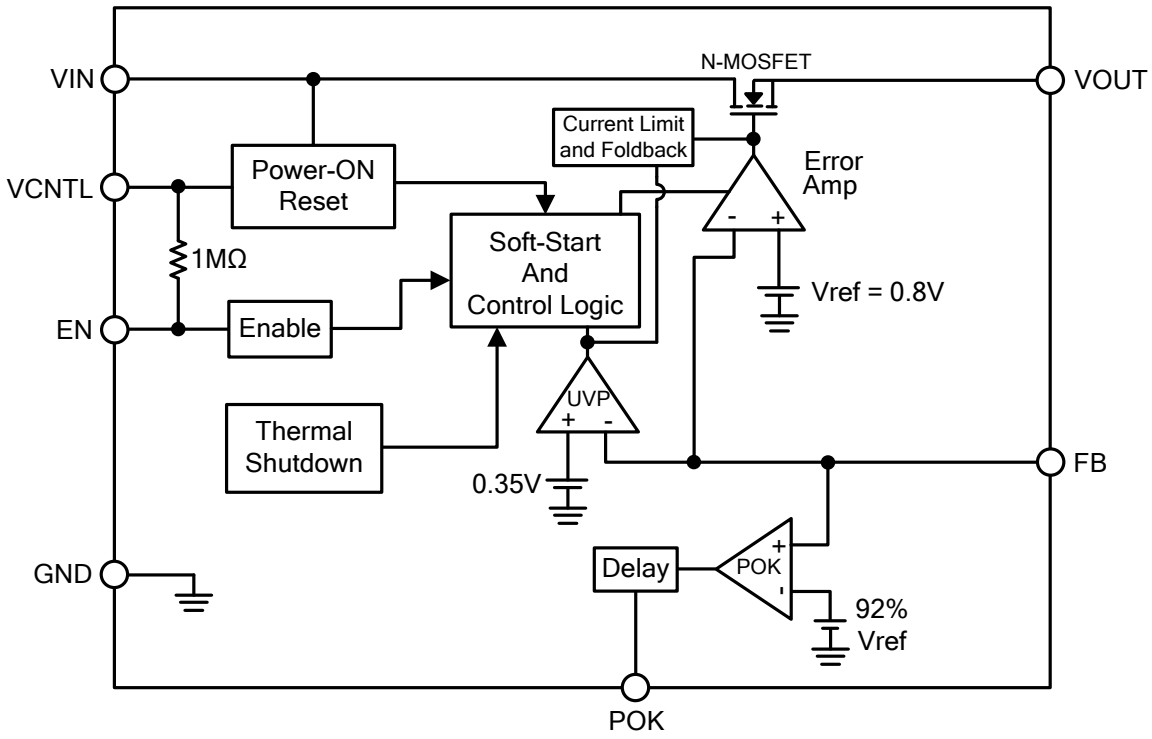


Figure 4. Block Diagram of FP6145B

Absolute Maximum Ratings

- VCNTL Supply Voltage ---------- -0.3V to +6V
- VIN Supply Voltage ---------- -0.3V to +6V
- VCNTL and VIN Pulse Voltage (15ns) ---------- -0.3V to +10V
- EN and FB Pin Voltage ---------- -0.3V to V_{CNTL}+0.3V
- Power OK Voltage ---------- -0.3V to +6V
- Power Dissipation @T_A=25°C, (P_D) (Note 1)
  - SOP-8 (Exposed Pad) ---------- 2.08W
- Package Thermal Resistance, (θ_{JA})
  - SOP-8 (Exposed Pad) ---------- 60°C/W
- Package Thermal Resistance, (θ_{JC})
  - SOP-8 (Exposed Pad) ---------- 15°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature (T_J) ---------- -40°C to 150°C
- Storage Temperature (T_{STG}) ---------- -65°C to 150°C

Note 1：θ_{JA} is measured with the PCB copper area (need connecting to Expose-Pad) of approximately 1.5 in^2 (Multi-layer)

Recommended Operating Conditions

- VCNTL Supply Voltage ---------- +3V to +5.5V
- VIN Supply Voltage ---------- +1.2V to +5.5V
- Output Voltage (Conditions: V_{CNTL}-V_{OUT}>1.9V) ---------- 0.8V to V_{IN}-V_{DROP}
- Output Current ---------- 0A to 2A
- Operating Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=1.2V, T_A=25°C unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Units
VCNTL POR Threshold		V_{CNTL}			2.5	2.7	2.9	V
VCNTL POR Hysteresis		$V_{CNTL(hys)}$			-	0.4	-	V
VIN POR Threshold		V_{IN}			0.95	1.05	1.15	V
VIN POR Hysteresis		$V_{IN(hys)}$				0.3		V
VCNTL Nominal Supply Current		I_{CNTL}	EN=V_{CNTL}		-	1	1.8	mA
VCNTL Shutdown Current		I_{SD}	EN=0V		-	10	15	μA
Feedback Voltage Regulation		V_{FB}	V_{CNTL}3.0~5.5V I_{OUT}=10mA		0.79	0.8	0.81	V
Load Regulation			I_{OUT}=10mA~2A		-	0.06	0.25	%
Dropout Voltage		V_{DROP}	I_{OUT}=2A V_{CNTL}=5V	1.2V＜V_{OUT}＜1.8V	-	0.23	0.28	V
				1.8V≦V_{OUT}＜2.5V	-	0.24	0.29	
				2.5V≦V_{OUT}＜2.8V	-	0.28	0.38	
				2.8V≦V_{OUT}＜3.1V	-	0.3	0.4	
VOUT Pull Low Resistance			EN=0V		-	85	-	Ω
Soft Start Time		T_{SS}			-	0.7	-	mS
EN Pin Logic High threshold voltage		V_{ENH}	Enable		1.2	-	-	V
		V_{ENL}	Disable		-	-	0.4	
EN Pin Pull High Resistor		I_{EN}	EN=V_{CNTL}		-	1	-	MΩ
Current Limit		I_{LIM}	V_{CNTL}=3~5.5V T_J= -40~125°C		3	4	-	A
Ripple Rejection	VIN	PSRR	F=120Hz, I_{OUT}=100mA		-	65	-	dB
	VCNTL				-	65	-	
Under-Voltage Protect Threshold			V_{FB} Falling		-	0.35	-	V
Under-Voltage Protect Current Foldback					-	120	-	mA
POK Threshold Voltage for Power OK		V_{POK}	V_{FB} Rising		89%	92%	95%	VFB
POK Threshold Voltage for Power Not OK		V_{PNOK}	V_{FB} Falling		-	89%	-	VFB
POK Low Voltage			POK sinks 1mA		-	0.25	0.4	V
POK Delay Time		T_{DELAY}			1	2	3	mS
Thermal shutdown Temp		T_{SD}			-	170	-	°C
Thermal Shutdown Hysteresis		$T_{SD(HYS)}$			-	50	-	°C

Typical Performance Curves

V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=1.2, I_{OUT}=2A

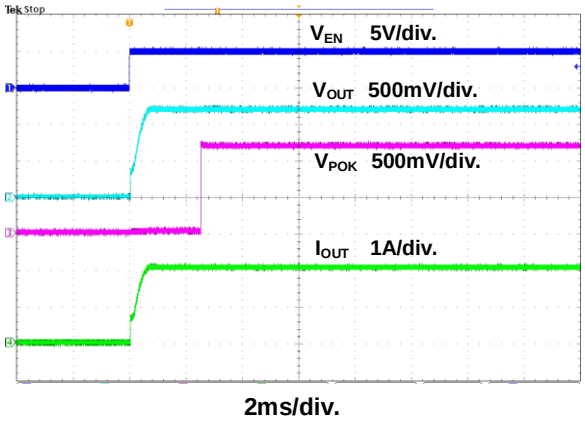


Figure 5. Start-up Response

V_{CNTL}= V_{EN}=5V, V_{OUT}=1.2, I_{OUT}=2A

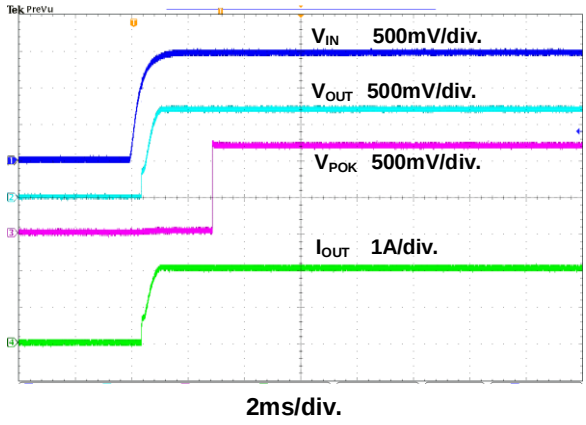


Figure 6. Power On Response

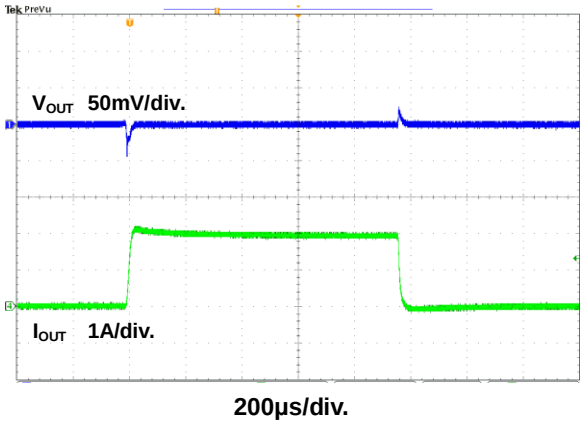


Figure 7. Load Transient Response

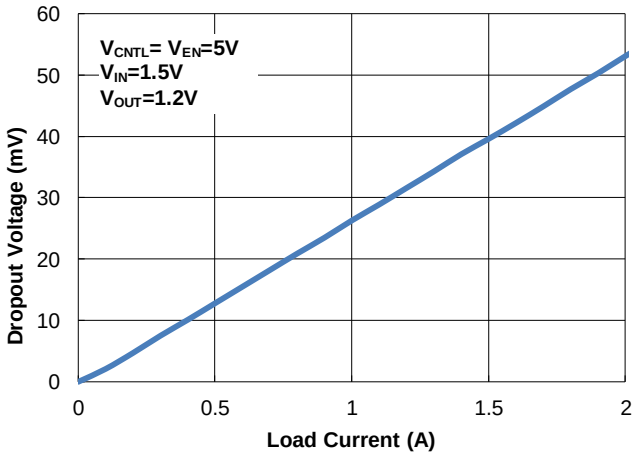


Figure 8. Dropout Voltage vs. Load Current

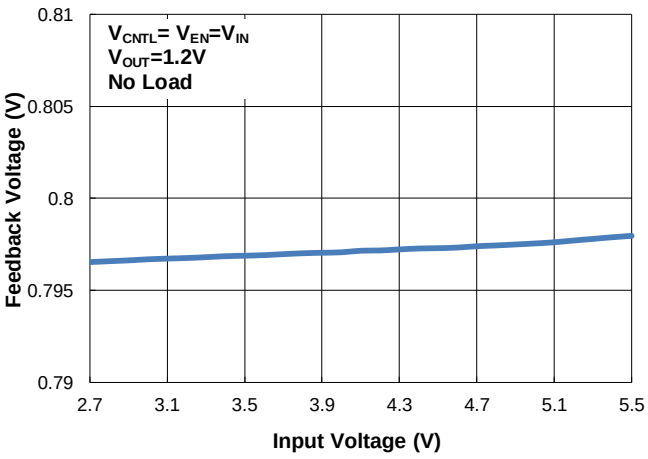


Figure 9. Line Regulation

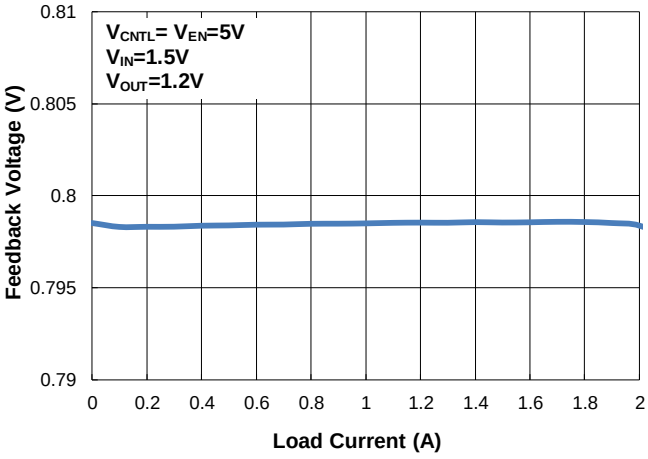


Figure 10. Load Regulation

Typical Performance Curves (Continued)

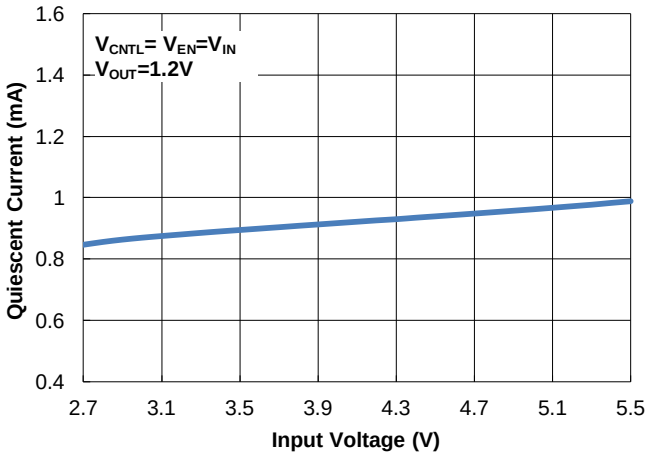


Figure 11. Quiescent Current vs. Input Voltage

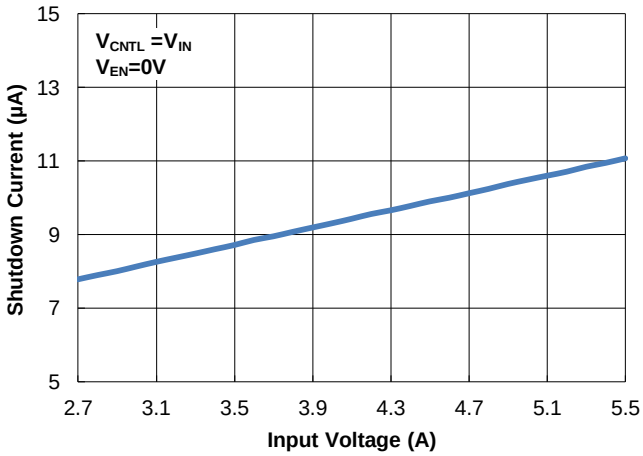


Figure 12. Shutdown Current vs. Input Voltage

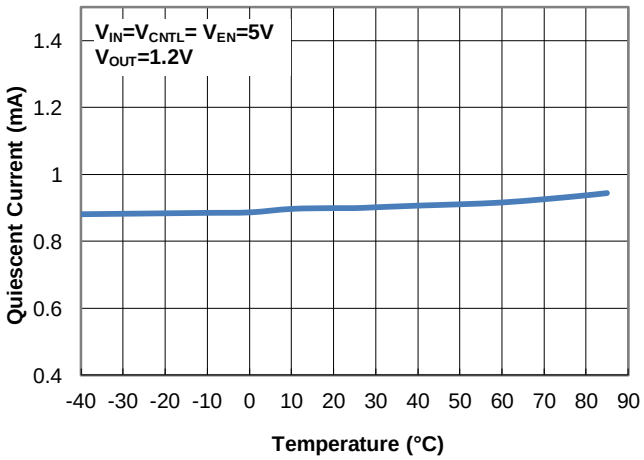


Figure 13. Quiescent Current vs. Temperature

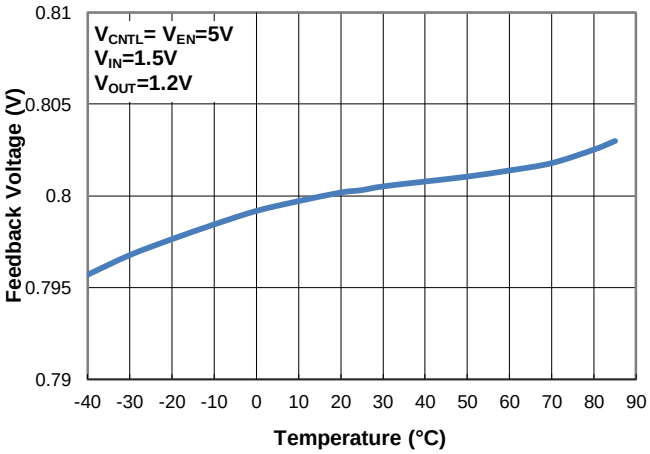


Figure 14. Feedback Voltage vs. Temperature

Function Description

FB

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT}=0.8\times\left(1+\frac{R1}{R2}\right)V$$

Where R1 is connected from VOUT to FB with Kelvin sensing, and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response. The recommended R1 and R2 are in the range of 1K~100KΩ.

VIN

MOSFET power supply input pin for power conversions. The voltage at this pin is monitored for Power-On Reset purpose.

VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

EN

Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When the IC is re-enabled, it will undergo a new soft-start cycle. When this internal pulled high to VCNTL pin is floating, it'll enable the regulator.

VOUT

Output pin of the regulator. It is necessary to connect an output capacitor with this pin for closed-loop compensation and improving transient responses.

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both supply voltages exceed their rising POR threshold voltages during powering on. The POR function will also pull low the POK pin regardless the output voltage when the VCNTL voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 0.7ms.

POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin will stop sinking current to GND when the rising FB voltage is above the V_{POK} over 2ms, and sink current again when the falling FB voltage is below the V_{PNOK}, which indicates the output is OK or not.

Output Voltage Regulation

A temperature compensated 0.8V reference error amplifier and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares V_{ref} with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from V_{IN} to V_{OUT}.

Current-Limit

The FP6145B monitors the current via the output NMOS and limits the maximum current to prevent FP6145B from damages during overload or short circuit conditions.

Under-Voltage Protection (UVP)

UVP prevents itself and load from short circuit damages by monitoring the voltage on FB pin after soft-start process finished. When the voltage on FB pin falls below 0.35V threshold, the circuit will initiate current foldback to reduce current limit to 120mA. When the FB voltage rises over 0.35V again, the current foldback will dismiss.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of FP6145B. When the junction temperature exceeds +170°C, a thermal sensor will turn off the output NMOS for cooling down the device. The regulator will regulate the output again through initiation of a new soft-start cycle after the junction temperature decreases 50°C and this will result in a pulsed output during continuous thermal overload conditions to prevent the system from damages.

Application Information

Input Capacitor

A minimum 1μF input ceramic capacitor is required. X5R or X7R is recommended. The capacitor should be placed as close to the device as possible for optimal performance.

Output Capacitor

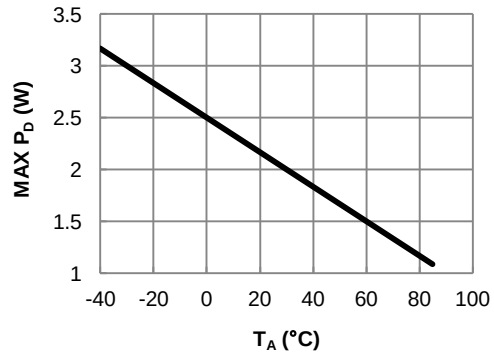
The FP6145B requires a minimum of output capacitor to maintain stability. The FP6145B is designed to be stable with low ESR ceramic capacitor. A 10μF ceramic capacitor is sufficient for most applications. X5R or X7R is recommended. The output capacitor must be placed within 1cm from the output pin of the device.

Thermal Considerations

The power dissipation of the device can be determined with the formula:

$$P_D \approx (V_{IN}-V_{OUT}) \times I_{OUT}$$

Additional copper area for heat sink is required in applications where the minimum input voltage is known and is large compared with the dropout voltage. The below figure shows the maximum allowable power dissipation of SOP-8 exposed pad package for different ambient temperatures, assuming θ_{JA} is 60°C/W and the maximum junction temperature is 125°C.

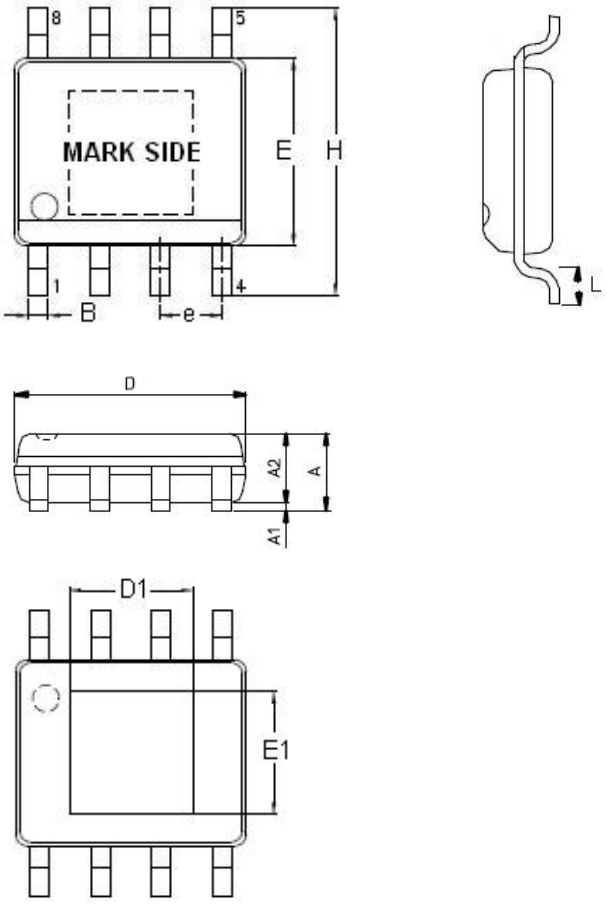


PCB Layout Consideration

1. Place the input capacitors of VIN and VCNTL as close to the device as possible.
2. Place output capacitor as close to the device as possible.
3. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. The area should be maximized to improve thermal performance.
4. Place R1, R2 and C4 close to the device to avoid noise coupling.
5. Use wide tracks for large current paths.

Outline Information

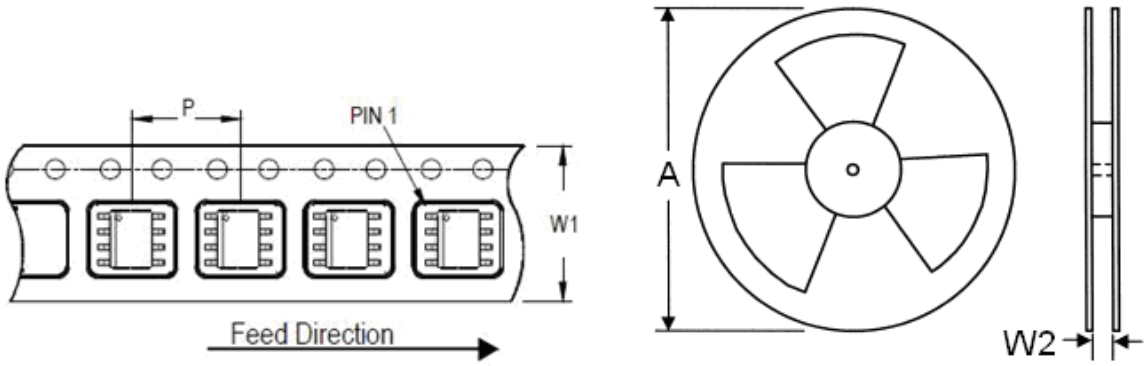
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	3.04	3.50
E	3.80	4.00
E1	2.15	2.41
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note：Followed From JEDEC MO-012-E.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

Life Support Policy
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