1.5MHz, 3A Synchronous Step-Down Regulator

Halogen Free

General Description

The FP6165 is a high efficiency current mode synchronous buck PWM DC-DC regulator. The internal generated 0.6V precision feedback reference voltage is designed for low output voltage. Low $R_{DS\ (ON)}$ synchronous switch dramatically reduces conduction loss. To extend battery life for portable application, 100% duty cycle is supported for low-dropout operation. Shutdown mode also helps saving the current consumption. The FP6165 is packaged in MSOP-10L, DFN-10L and SOP-8L to reduce PCB space.

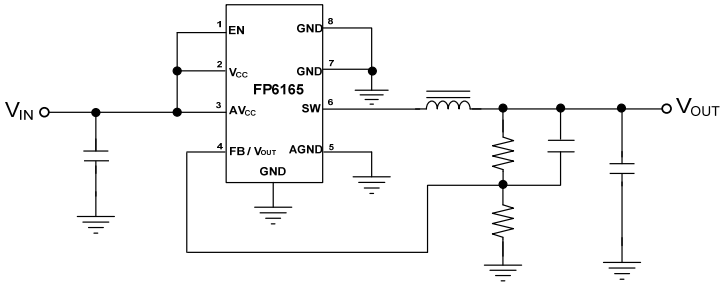
Features

- Input Voltage Range: 2.5 to 5.5V
- Adjustable Output Voltage From 0.6V to V_{IN}
- Precision Feedback Reference Voltage: 0.6V (±2%)
- Output Current: 3A (Max.)
- Duty Cycle: 0~100%
- Internal Fixed PWM Frequency: 1.5MHz
- Low Quiescent Current: 100μA
- No Schottky Diode Required
- Built-in Soft Start
- Current Mode Operation
- Over Temperature Protection
- Package: MSOP-10L (EP), DFN-10L, SOP-8L (EP)

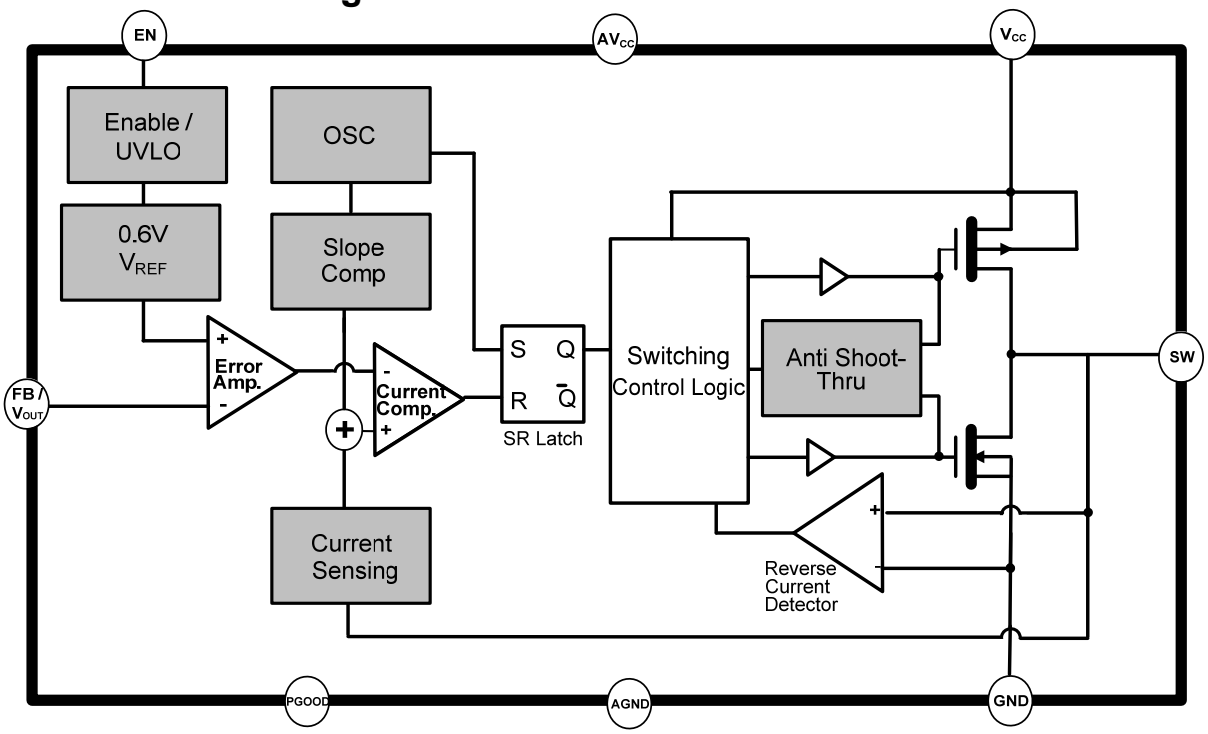
Applications

- Cellular Telephone
- Wireless and DSL Modems
- Digital Still Cameras
- Portable Products
- MP3 Players

Typical Application Circuit



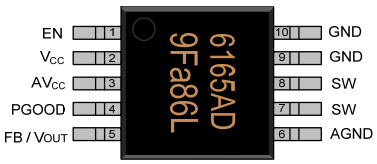
Function Block Diagram



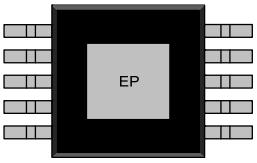
Pin Descriptions

MSOP-10L (EP)

Top View



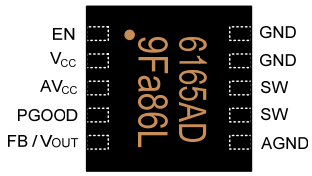
Bottom View



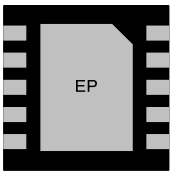
Name	No.	I / O	Description
EN	1	I	Enable / UVLO
V_{CC}	2	P	Supply Voltage
AV_{CC}	3	P	Analog Supply Voltage
PGOOD	4	O	Power Good Open Drain Output
FB / V_{OUT}	5	I	Feedback
AGND	6	P	Analog Ground
SW	7	O	Switch
SW	8	O	Switch
GND	9	P	Ground
GND	10	P	Ground
EP	11	P	Exposed PAD - Must Connect to Ground

DFN-10L

Top View



Bottom View



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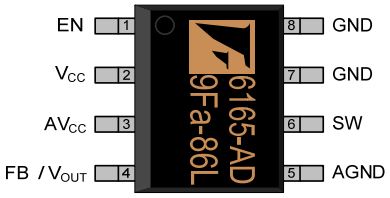
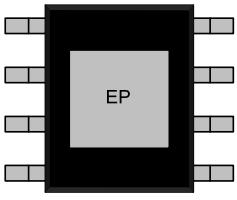
EP	11	P	Exposed PAD - Must Connect to Ground

SOP-8L (EP)

Top View



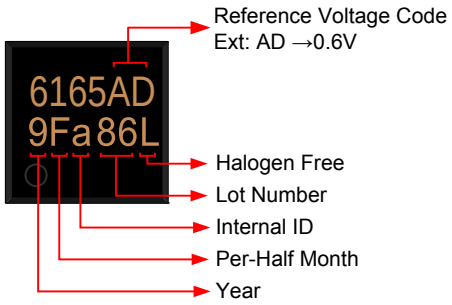
Bottom View



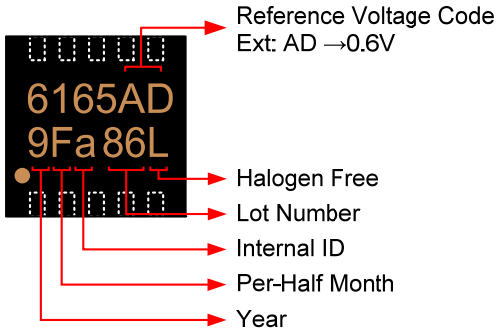
Name	No.	I / O	Description
EN	1	I	Enable / UVLO
V_{CC}	2	P	Supply Voltage
AV_{CC}	3	P	Analog Supply Voltage
FB / V_{OUT}	4	I	Feedback
AGND	5	P	Analog Ground
SW	6	O	Switch
GND	7	P	Ground
GND	8	P	Ground
EP	9	P	Exposed PAD - Must connect to Ground

Marking Information

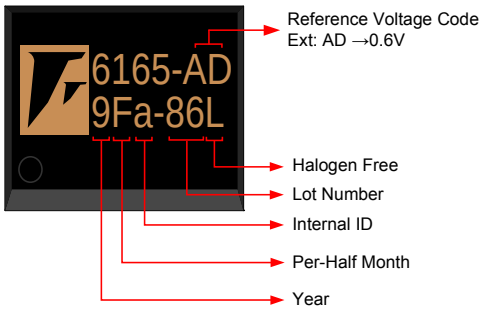
MSOP-10L (EP)



DFN-10L



SOP-8L (EP)



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

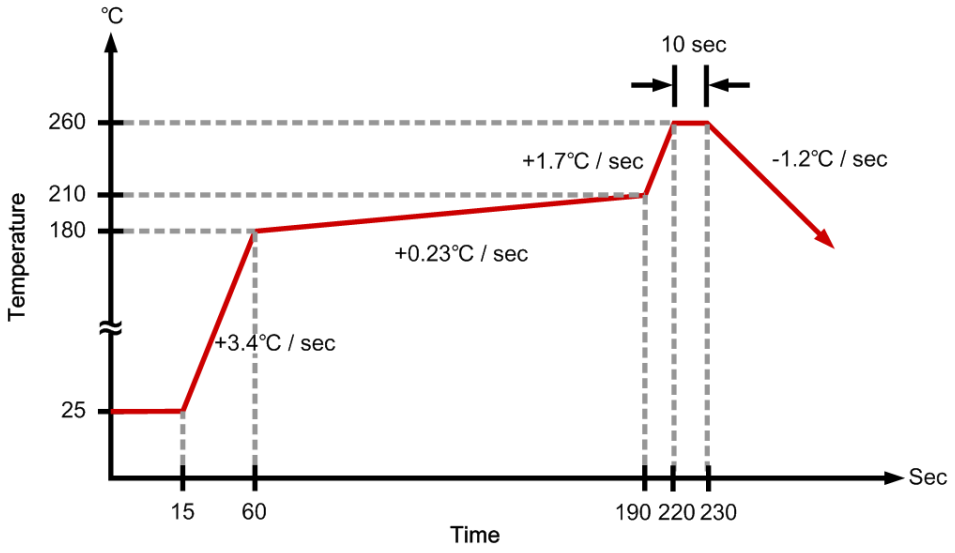
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6165ADgR-G1	-40°C ~ +85°C	MSOP-10L (EP)	3000EA	Tape & Reel
FP6165ADdR-G1	-40°C ~ +85°C	DFN-10L	2500EA	Tape & Reel
FP6165ADXR-G1	-40°C ~ +85°C	SOP-8L (EP)	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Supply Voltage	V_{IN}		-0.3		6	V
EN, V_{FB}, SW Voltage			-0.3		V_{IN}	V
P-Channel Switch Source Current (DC)					3.9	A
N-Channel Switch Source Current (DC)					3.9	A
Peak SW Switch Sink and Source Current (AC)					6	A
Thermal Resistance (Junction to Ambient)	θ_{JA}	MSOP-10L			+70	°C / W
		DFN-10L			+65	°C / W
		SOP-8L			+50	°C / W
Thermal Resistance (Junction to Case)	θ_{JC}	MSOP-10L			+10	°C / W
		DFN-10L			+10	°C / W
		SOP-8L			+10	°C / W
Junction Temperature					+150	°C
Storage Temperature			-65		+150	°C
Lead Temperature (soldering, 10 sec)					+260	°C

Suggested IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		2.5		5.5	V
Operating Temperature			-40		+85	°C

DC Electrical Characteristics (V_{IN}=3.6V ,T_A= 25°C , unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Regulated Feedback Voltage	V_{FB}	T_A=25°C	0.588	0.6	0.612	V
		-40°C~+85°C	0.582	0.6	0.618	V
Line Regulation with V_{REF}	ΔV_{FB}	V_{IN}=2.5V to 5.5V		0.04	0.4	% / V
Output Voltage LineRegulation	ΔV_{OUT}	V_{IN}=2.5 to 5.5V		0.04	0.4	% / V
RDS $_{(ON)}$ of P-Channel FET	$R_{DS\ (ON)}$ P	I_{SW}=100mA		60	90	mΩ
RDS $_{(ON)}$ of N-Channel FET	$R_{DS(ON)}$ N	I_{SW} =-100mA		60	90	mΩ
SW Leakage	I_{LSW}	V_{EN}=0V, V_{IN}=5V		±0.01	±1	μA
Peak Inductor Current	I_{PK}	V_{FB}=0.5V	3.75	5	6	A
Input Voltage Range	V_{IN}	-40°C~+85°C	2.5		5.5	V
Quiescent Current	I_{CC}	Shutdown, V_{EN}=0V		0.1	1	μA
		Active, V_{FB}=0.5V, V_{EN}=V_{IN}		100		μA
		PFM, V_{FB}=0.7V, V_{EN}=V_{IN}		80		μA
EN Threshold	V_{EN}	-40°C~ +85°C	0.3	1	1.5	V
EN Leakage Current	I_{EN}	-40°C ~+85°C		±0.01	±1	μA
Oscillator Frequency	F_{OSC}	V_{FB}=0.6V, -40°C ~+85°C	1.2	1.5	1.8	MHz

Function Description

Control Loop

The FP6165 is a high efficiency current mode synchronous buck regulator. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are built internally. With current mode operation, the PWM duty is controlled both by the error amplifier output and the peak inductor current. At the beginning of each cycle, the oscillator turn on the P-MOSFET switch to source current from V_{IN} to SW output. Then, the chip starts to compare the inductor current with the error amplifier output. Once the inductor current is larger than the error amplifier output, the P-MOSFET switch is turned off. When the load current increases, the feedback voltage FB will slightly drop. This causes the error amplifier to output a higher current level until the prior mentioned peak inductor current reach the same level. The output voltage then can be sustained at the same.

When the top P-MOSFET switch is off, the bottom synchronous N-MOSFET switch is turned on. Once the inductor current reverses, both top and bottom MOSFET will be turn off to leave the SW pin into high impedance state.

The FP6165's current mode control loop also includes slope compensation to suppress sub-harmonic oscillations at high duty cycles. This slope compensation is achieved by adding a compensation ramp to the inductor current signal.

LDO Mode

The FP6165's maximum duty cycle can reach 100%. That means the driver's main switch is turn on through out whole clock cycle. Once the duty reaches 100%, the feedback path no longer controls the output voltage. The output voltage will be the input voltage minus the main switch voltage drop.

Over Current Protection

FP6165 limits the peak main switch current cycle by cycle. When over current occurs, chip will turn off the main switch and turn the synchronous switch on until next cycle.

Short Circuit Protection

When the FB pin is drop below 300mV, the chip will tri-state the output pin SW automatically. After 300us rest to avoid over heating, chip will re-initiate PWM operation with soft start.

Power Good

The power good pin is an open-drain output. Connects a 100kΩ pull up resistor between V_{IN} and this pin to obtain a PGOOD voltage. When the output voltage is not within ±10% of setting output

voltage, the PGOOD pin will be pulled down to ground immediately. After the output voltage is within ±10% of setting output voltage for 42.7μs (typ.), the PGOOD pin pull-down is turned off. Then it can be pulled up to V_{IN} through external pull-high resister.

Connect this pin to AGND if not used.

Thermal Protection

FP6165 will shutdown automatically when the internal junction temperature reaches 150℃ to protect both the part and the system.

Application Information

Input capacitor Selection

The input capacitor must be connected to the VIN pin and GND pin of FP6165 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

In switch mode, the input current is discontinuous in a buck converter. The source current waveform of the high-side MOSFET is a square wave. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The RMS value of input capacitor current can be calculated by:

$$I_{RMS} = I_{O\_MAX}\sqrt{\frac{V_O}{V_{IN}}\left(1-\frac{V_O}{V_{IN}}\right)}$$

It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is I_{O_MAX}/2.

Inductor Selection

The value of the inductor is selected based on the desired ripple current. Large inductance gives low inductor ripple current and small inductance result in high ripple current. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current. In experience, the value is to allow the peak-to-peak ripple current in the inductor to be 10%~20% maximum load current. The inductance value can be calculated by:

$$L = \frac{(V_{IN}-V_O)}{f\times\Delta I_L}\frac{V_O}{V_{IN}} = \frac{(V_{IN}-V_O)}{f\times[2\times(10\%\sim 20\%)I_O]}\frac{V_O}{V_{IN}}$$

The inductor ripple current can be calculated by:

$$\Delta I_L = \frac{V_O}{f\times L}\times\left[1-\frac{V_O}{V_{IN}}\right]$$

Choose an inductor that does not saturate under the worst-case load conditions, which is the load current plus half the peak-to-peak inductor ripple current, even at the highest operating temperature. The peak inductor current is:

$$I_{L\_PEAK} = I_O + \frac{\Delta I_L}{2}$$

The inductors in different shape and style are available from manufacturers. Shielded inductors are small and radiate less EMI issue. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Inductor Value (μH)	Dimensions (mm)	Component Supplier	Model
2.2	8.3×8.3×4.5	FENG-JUI	TPRH8D43-2R2M
2.2	10.3×10.3×4.0	FENG-JUI	TPRH10D40-2R2M
3.3	8.3×8.3×4.5	FENG-JUI	TPRH8D43-3R3M
3.3	10.3×10.3×4.0	FENG-JUI	TPRH10D40-3R3M
4.7	8.3×8.3×4.5	FENG-JUI	TPRH8D43-4R7M
4.7	10.3×10.3×4.0	FENG-JUI	TPRH10D40-4R7M

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. The output ripple is determined by:

$$\Delta V_O = \Delta I_L \times \left(ESR_{COUT} + \frac{1}{8 \times f \times C_{OUT}} \right)$$

Where f = operating frequency, COUT= output capacitance and ΔIL = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔIL increases with input voltage.

Capacitor Value	Case Size	Component Supplier	Model
10μF	0805	Taiyo Yuden	JMK212BJ106MG
10μF	0805	TDK	C12012X5ROJ106K
22μF	0805 1206	TDK	C2012JB0J226M

Using Ceramic Input and Output Capacitors

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush current through the long wires can potentially cause a voltage spike at V_{IN}, which may large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R or X7R specification. Their dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

In the adjustable version, the output voltage is set using a resistive voltage divider from the output voltage to FB. The output voltage is:

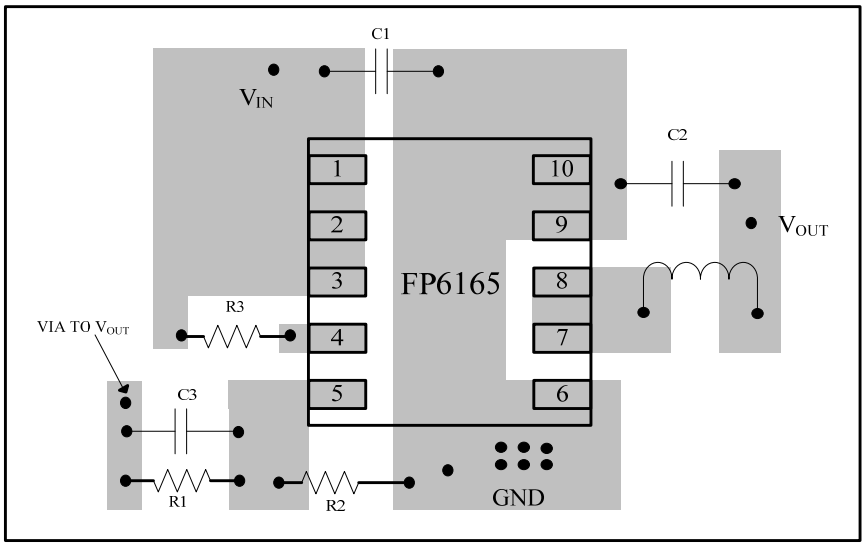
$$V_O = 0.6V \left(1 + \frac{R_1}{R_2} \right)$$

The recommended resistor value is summarized below:

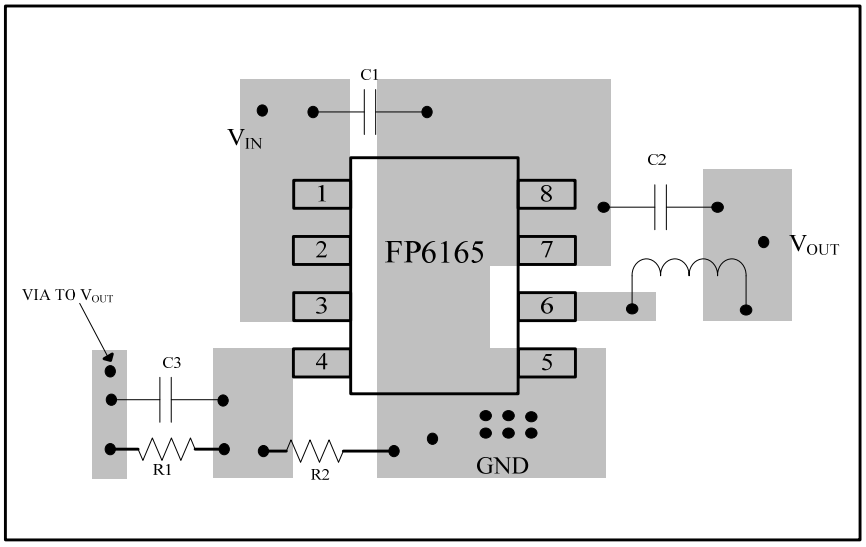
V_{OUT} (V)	R_1 (Ω)	R_2 (Ω)	C_3 (F)
0.6	200k	Not Used	Not Used
1.2	200k	200k	10p
1.5	300k	200k	10p
1.8	200k	100k	10p
2.5	270k	85k	10p
3.3	306k	68k	10p

PC Board Layout Checklist

1. The power traces, consisting of the GND, SW and V_{IN} trace should be kept short, direct and wide.
2. Place C_{IN} near V_{IN} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
3. The resistive divider R_1 and R_2 must be connected to FB pin directly and as closely as possible.
4. FB is a sensitive node. Please keep it away from switching node, SW. A good approach is to route the feedback trace on another PCB layer and have a ground plane between the top and feedback trace routing layer. This reduces EMI radiation on to the DC-DC converter its own voltage feedback trace.
5. Keep the GND plates of C_{IN} and C_{OUT} as close as possible. Then connect this to the ground plane (if one is used) with several vias. This reduces ground plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at FP6161 by giving it a low impedance ground connection.

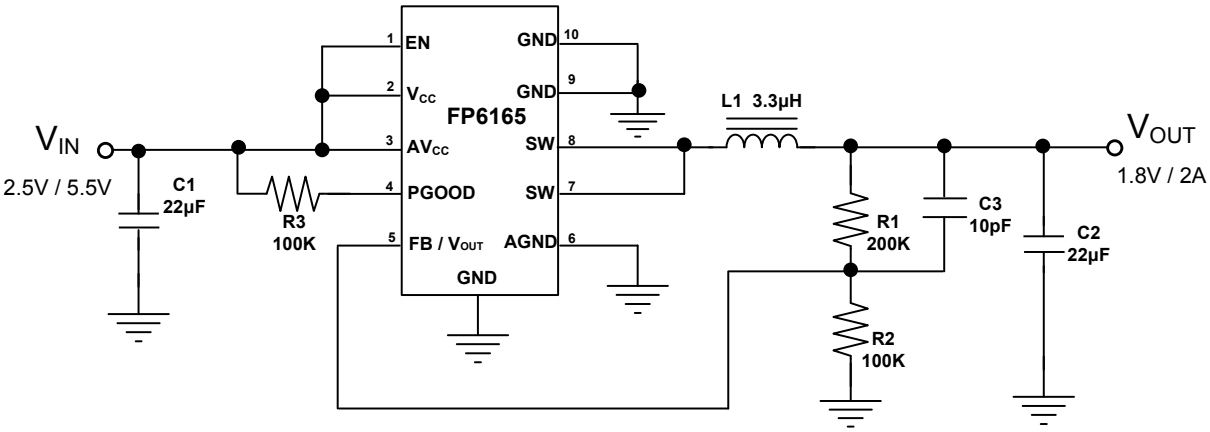


Suggested Layout for DFN-10L / MSOP-10L

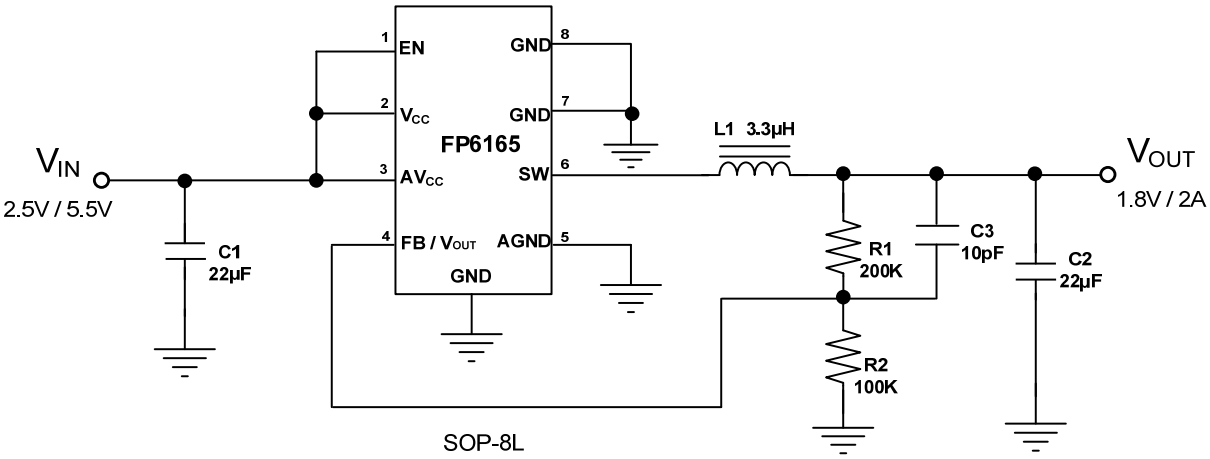


Suggested Layout for SOP-8L

Typical Application



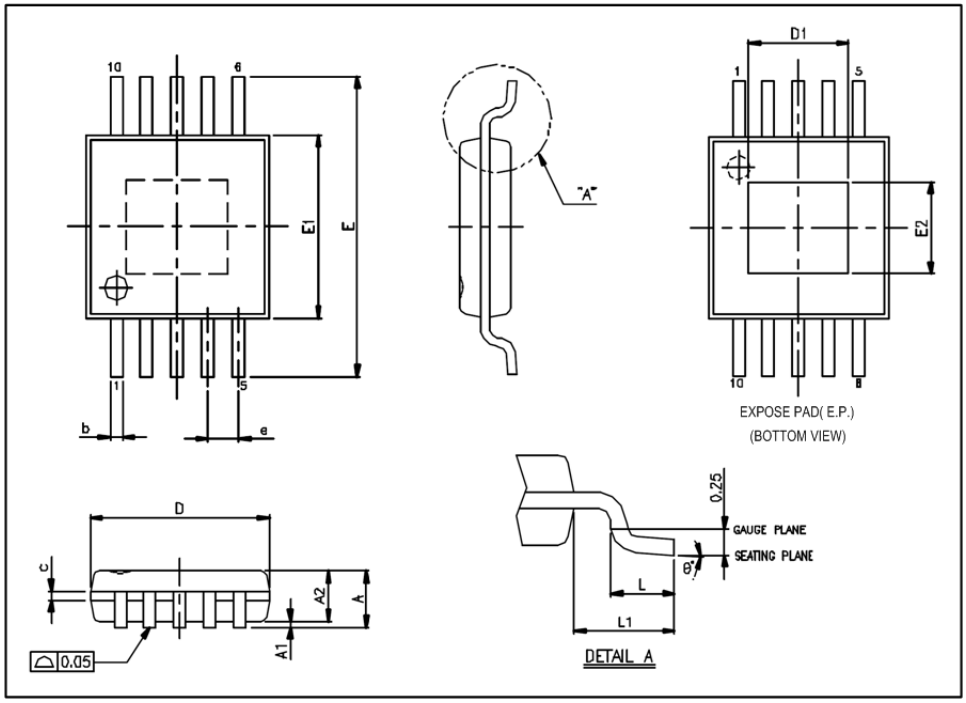
DFN-10L / MSOP-10L



SOP-8L

Package Outline

MSOP-10L (EP)



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A		1.100
A1	0.000	0.150
A2	0.750	0.950
b	0.170	0.270
c	0.080	0.230
D	3.000 BSC.	
E	4.900 BSC.	
E1	3.000 BSC.	
e	0.500 BSC.	
L	0.400	0.800
L1	0.950 REF.	
θ°	0°	8°

MSOP-10L (EP) continued

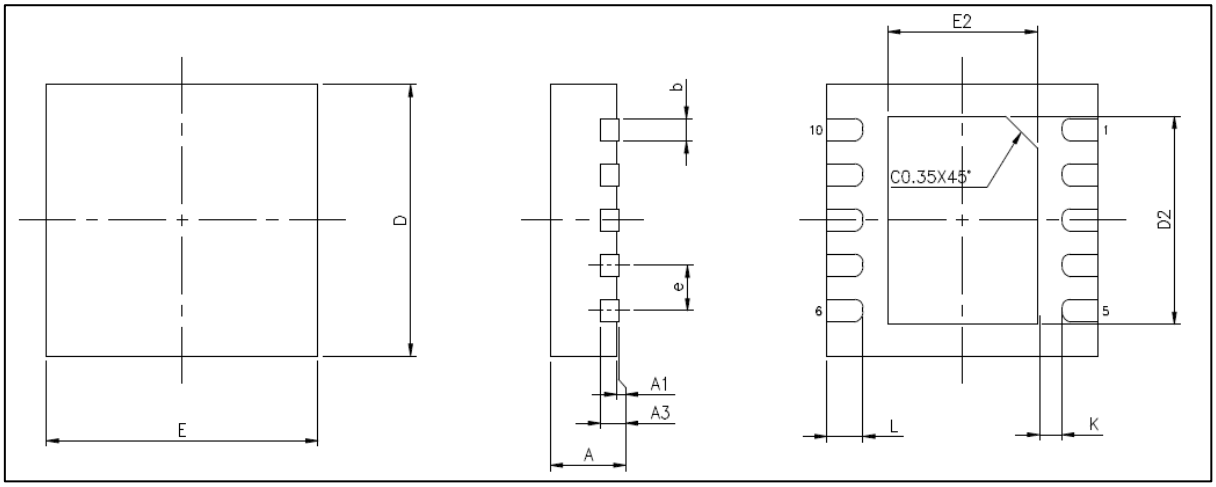
Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E2	1.715 REF	
D1	1.600 REF	

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-187 BA-T.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E1” does not include inter-lead flash or protrusions.

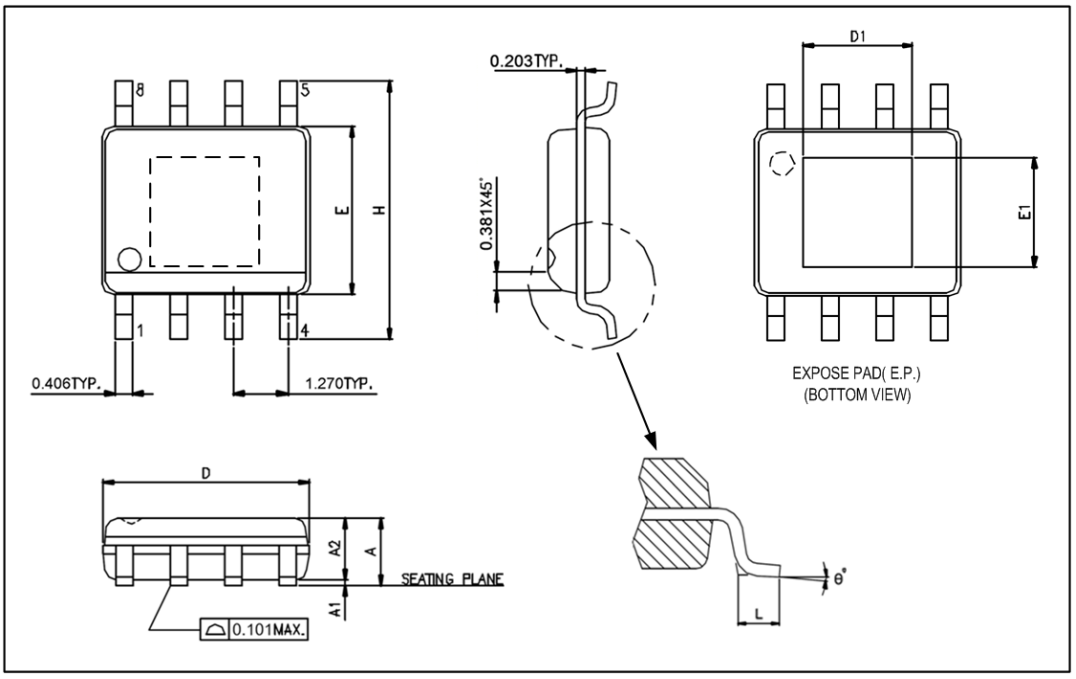
DFN-10L (EP)



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	0.700	0.800
A1	0.000	0.050
A3	0.20REF	
b	0.180	0.300
D	3.00	
E	3.00	
D2	2.200	2.700
E2	1.400	1.750
e	0.500	
L	0.300	0.500
K	0.200	

SOP-8L (EP)



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	2.184 REF	
D1	2.971 REF	

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-178 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions