## 2A, 23V, 380KHz Step-Down Converter

### General Description

The FP6187 is a buck regulator with a built-in internal power MOSFET. It can provide 2A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. The device includes cycle-by-cycle current limiting and thermal shutdown protection. The regulator only consumes 23μA supply current in shutdown mode. The FP6187 requires a minimum number of readily available external components to complete a 2A buck regulator solution.

### Features

➢ 2A Output Current

➢ 0.22Ω Internal Power MOSFET Switch

➢ Stable with Low ESR Output Ceramic Capacitors Up to 95% Efficiency

➢ 23μA Shutdown Mode Current

➢ Fixed 380KHz frequency

➢ Thermal Shutdown

➢ Cycle-by-Cycle Over Current Protection

➢ Wide 4.75 to 23V Operating Input Range

➢ Output Adjustable From 1.23 to 21V

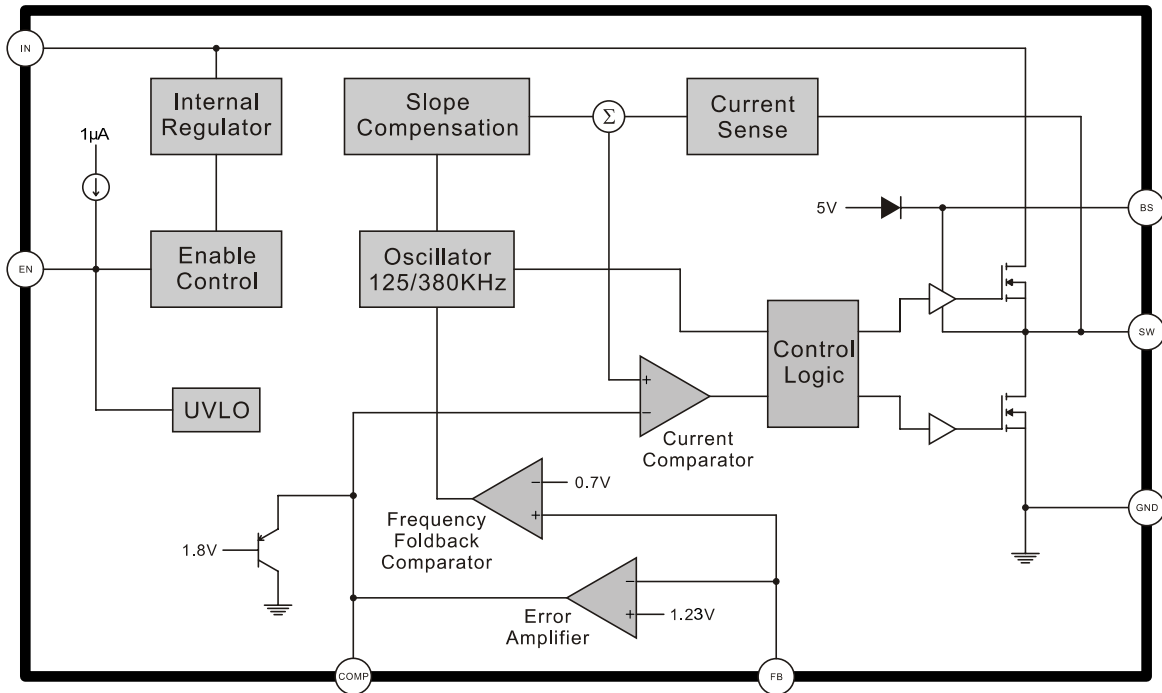➢ Available SOP-8L Package

➢ Under Voltage Lockout

### Applications

➢ Distributed Power Systems

➢ Battery Charger Network Cards

➢ Pre-Regulator for Linear Regulators
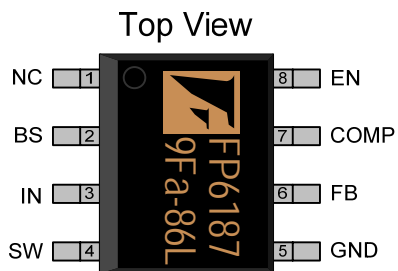
➢ DSL Modems

### Typical Application Circuit
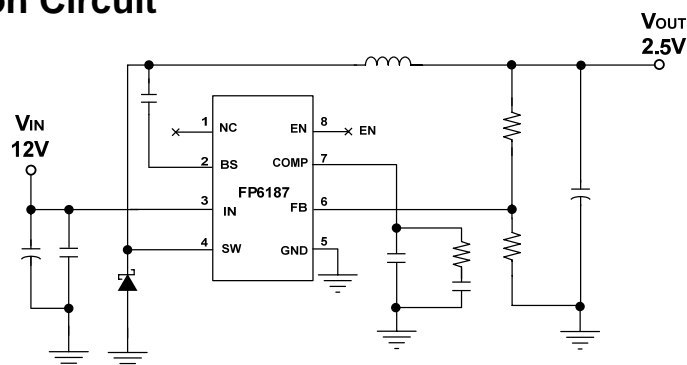
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## Function Block Diagram



## Pin Descriptions

**SOP-8L**

Top View



| Name | No. | I / O | Description |
|------|-----|-------|-------------|
| NC | 1 | | No Internal Connection |
| BS | 2 | O | Bootstrap |
| IN | 3 | P | Supply Voltage |
| SW | 4 | O | Switch |
| GND | 5 | P | Ground |
| FB | 6 | I | Feedback |
| COMP | 7 | O | Compensation |
| EN | 8 | I | EN / UVLO |

# IC Date Code Identification

FP6187
9Fa-86L
→ Halogen Free
→ Lot Number
→ Mass Production Version
→ Per-Half Month
→ Year
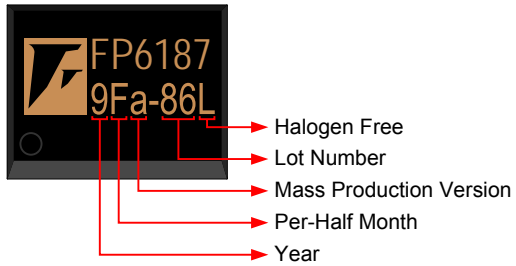
**Halogen Free**: Halogen free product indicator

**Lot Number**: Wafer lot number's last two digits

For Example: 132371TB → 71

**Mass Production Version**: Mass production mask version

**Per-Half Month**: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

**Year**: Production year's last digit

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## Ordering Information

| Part Number | Operating Temperature | Package | MOQ | Description |
|---|---|---|---|---|
| FP6187D-G1 | -40°C ~ +85°C | SOP-8L | 100EA | Tube |
| FP6187DR-G1 | -40°C ~ +85°C | SOP-8L | 2500EA | Tape & Reel |

## Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{IN}$ | | -0.3 | | 24 | V |
| Supply Voltage | $V_{sw}$ | | -1 | | $V_{IN}$ +0.3 | V |
| Bootstrap Voltage | $V_{BS}$ | | $V_{sw}$ -0.3 | | $V_{sw}$ +6 | V |
| All Other Pins | | | -0.3 | | 6 | V |
| Junction Temperature | $T_J$ | | | | +150 | °C |
| Storage Temperature | $T_S$ | | -65 | | +150 | °C |
| Allowable Power Dissipation | | SOP-8L | | | 570 | mW |
| Thermal Resistance | $\theta_{JA}$ | SOP-8L | | +110 | | °C / W |
| | $\theta_{JC}$ | | | | +55 | °C / W |
| Lead Temperature (soldering, 10 sec) | | SOP 8L | | +260 | | °C |

## Suggested IR Re-flow Soldering Curve
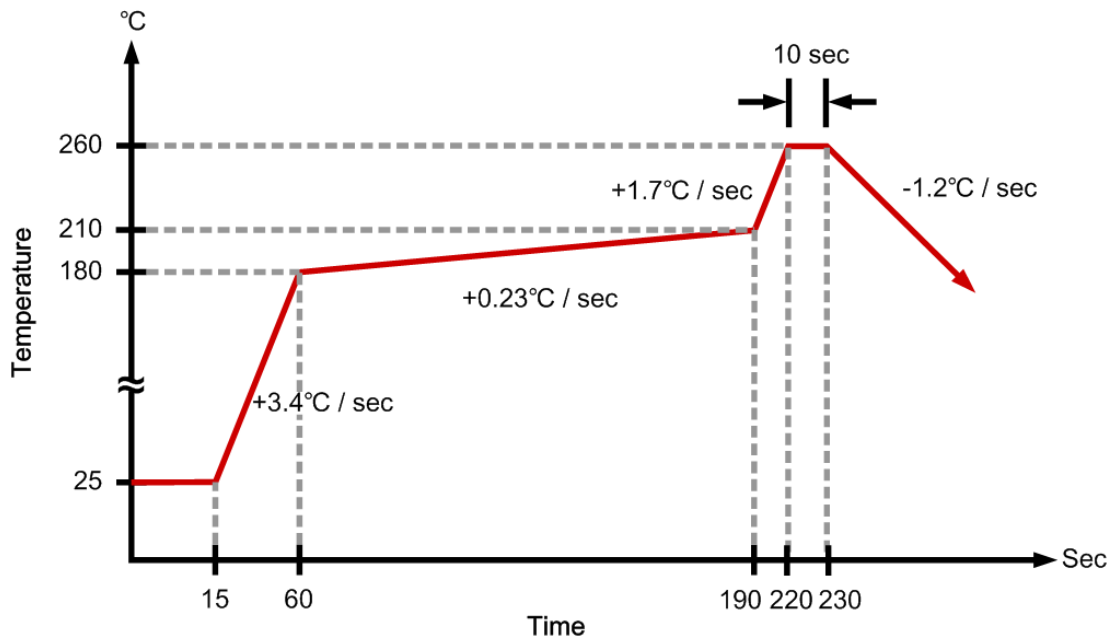
Website: http://www.feeling-tech.com.tw                                                                                            Rev. 0.6

## Recommended Operating Conditions

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{IN}$ | | 4.75 | | 23 | V |
| Operating Temperature | | | -40 | | 85 | ℃ |

## DC Electrical Characteristics ($V_{IN}$=12V, $T_A$= 25℃, unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Standby Current | $I_{SB}$ | $V_{EN} \geq$ 3V, $V_{FB} \geq$ 1.5V | | 1.0 | 1.5 | mA |
| Shutdown Supply Current | $I_{ST}$ | $V_{EN}$=0V | | 23 | 50 | μA |
| Feedback Voltage | $V_{FB}$ | $V_{COMP}$<2V | 1.17 | 1.23 | 1.27 | V |
| High Side Switch ON Resistance | $R_{ON-HS}$ | | | 0.22 | | Ω |
| Low Side Switch ON Resistance | $R_{ON-LS}$ | | | 10 | | Ω |
| High Side Switch Leakage Current | $I_{IL}$ | $V_{EN}$=0V, $V_{SW}$=0V | | 0.1 | 10 | μA |
| Current Limit | $I_{CL}$ | | 2.8 | 3.4 | 4.7 | A |
| Oscillation Frequency | $f_{OSC}$ | | 320 | 380 | 460 | KHz |
| Short Circuit Oscillation Frequency | $f_{SC}$ | $V_{FB}$=0V | | 125 | | KHz |
| Maximum Duty Cycle | $D_{MAX}$ | $V_{FB}$=1.0V | | 90 | | % |
| Minimum Duty Cycle | $D_{MIN}$ | $V_{FB}$=1.5V | | | 0 | % |
| Under Voltage Lockout Threshold | $V_{UVLO}$ | $V_{EN}$ Rising | 2.0 | 2.5 | 3.0 | V |
| Under Voltage Lockout Threshold Hysteresis | $V_{HYS}$ | | | 200 | | mV |
| EN Threshold Voltage | $V_{EN}$ | $I_{CC}$＞100μA | 0.7 | 1.0 | 1.3 | V |
| EN Pull Up Current | $I_{EN}$ | $V_{EN}$=0V | | 1.0 | | μA |
| Thermal Shutdown | $T_{TS}$ | | | +140 | | °C |

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## Typical Operating haracteristics

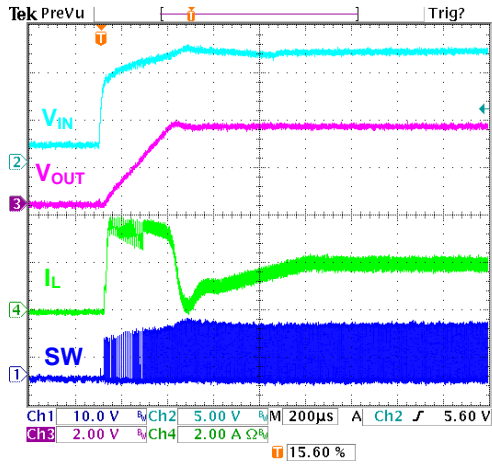($V_{IN}$=12V, $T_A$= 25°C, $V_{OUT}$=3.3V unless otherwise noted)
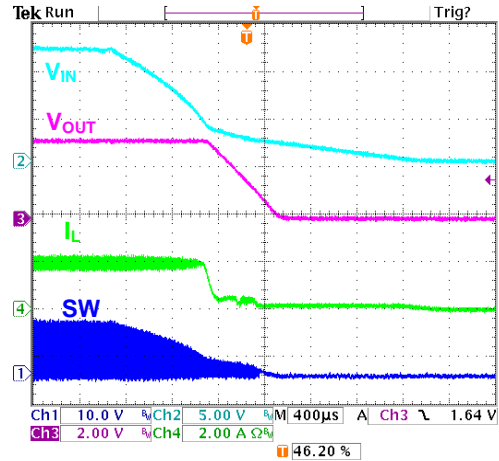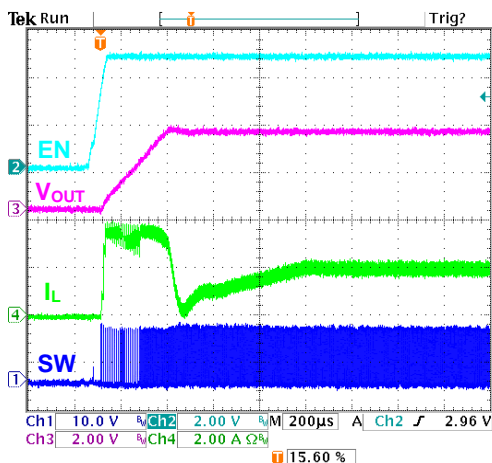


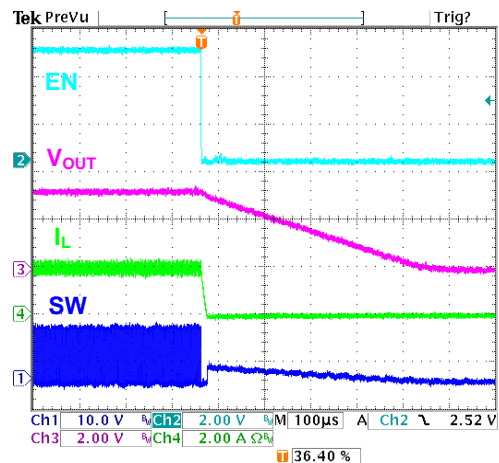**Figure 1 Power on**



**Figure 2 Power off**
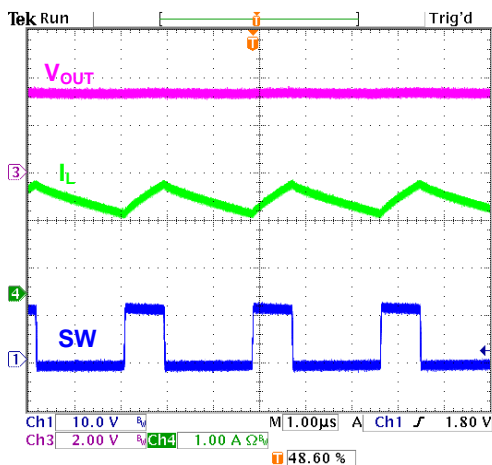


**Figure 3 EN pin Enable**



**Figure 4 EN pin Disable**



**Figure 5 Load 3A**
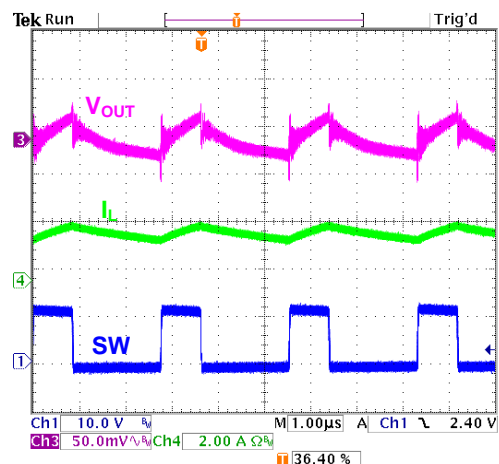


**Figure 6 Load Ripple**

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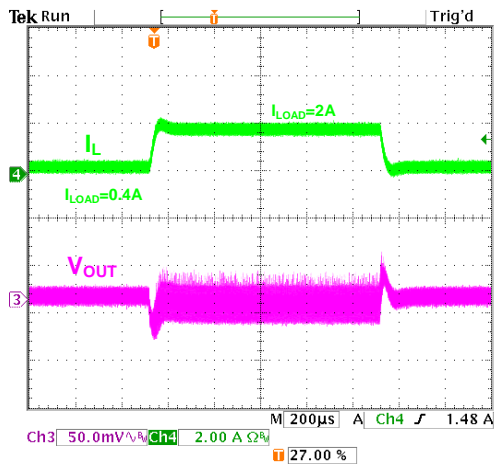Rev. 0.6

**Figure 7 Load Step**
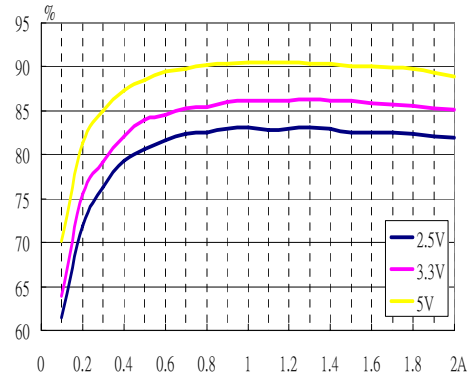


**Figure 8 Efficiency (V<sub>IN</sub>=10V)**
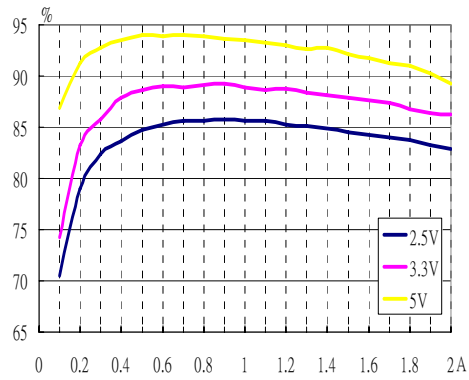


**Figure 9 Efficiency (V<sub>IN</sub>=7V)**

## Function Description

The FP6187 is a current-mode buck regulator. It regulates input voltages from 4.75V to 23V down to an output voltage as low as 1.23V with maximum 2A load current. The FP6187 uses current-mode control to regulate the output voltage. The output voltage is measured at FB pin through a resistive voltage divider and amplified by the internal error amplifier. The output current of the trans-conductance error amplifier is presented at COMP pin where a network compensates the regulation control system. The voltage at COMP pin is compared to the switch current measured internally to control the output voltage. The converter uses an internal n-channel MOSFET switch to step-down the input voltage to the regulated output voltage. Since the MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS drives the gate. The capacitor is internally charged while the switch is off. Another internal built-in 10Ω switch from SW to GND is used to insure that SW is pulled to GND when the switch is off to fully charge the BS capacitor.

### Output Voltage (V<sub>OUT</sub>)

The output voltage is set using a resistive voltage divider from the output voltage to FB. The voltage divider divides the output voltage down by the ratio:

$$V_{FB} = V_{OUT} \times \frac{R_4}{R_2 + R_4}$$

Thus the output voltage is:

$$V_{OUT} = V_{FB} \times \frac{R_2 + R_4}{R_4}$$

A typical value for $R_4$ can be as high as 100k, but a typical value is 10K.

### Enable Mode / Shutdown Mode

Drive EN pin to ground to shut down the FP6187. Shutdown mode forces the internal power MOSFET off, turns off all internal circuitry, and reduces the $V_{IN}$ supply current to 23μA (typ.). The EN Pin rising threshold is 1.0V (typ.). Before any operation begins, the voltage at EN pin must exceed 1.0V (typ.).

The EN pin input has 100mV hysteresis.

### Boost High-Side Gate Drive (BST)

Since the MOSFET requires a gate voltage greater than the input voltage, user should connect a flying bootstrap capacitor between SW and BS to provide the gate-drive voltage to the high-side n-channel MOSFET switch. The capacitor is charged by the internally regulator periodically when SW pin is pulled to ground. During startup, an internal low-side switch pulls SW pin to ground and charges

the BST capacitor to internally regulator output voltage. Once the BST capacitor is charged, the internal low-side switch is turned off and the BST capacitor voltage provides the necessary enhancement voltage to turn on the high-side switch.

**Thermal Shutdown Protection**

The FP6187 features integrated thermal shutdown protection. Thermal shutdown protection limits allowable power dissipation ($P_D$) in the device, and protects the device in the event of a fault condition. When the IC junction temperature exceeds +150°C, an internal thermal sensor signals the shutdown logic to turn off the internal power MOSFET and allow the IC cooling down. The thermal sensor turns the internal power MOSFET back on after the IC junction temperature cools down to + 110°C, resulting in a pulsed output under continuous thermal overload conditions.

# Application Information

## Input Capacitor Selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

The input capacitor can be electrolytic, tantalum or ceramic. When electrolytic or tantalum capacitors are used, a small, high quality 0.1μF ceramic capacitor should be placed beside the IC as close as possible.

When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at converter input. The input voltage ripple can be estimated by

$$C_{IN} = \frac{I_O}{f \times \Delta V_{IN}} \times D(1-D)$$

## Inductor Selection

The inductor is required to supply current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by

$$L = \frac{V_O + V_D}{I_O \gamma f} \times (1-D)$$

Where $\gamma$ is the ripple current ratio

RMS current in inductor $I_{Lrms} = I_O \sqrt{1 + \frac{\gamma^2}{12}}$

## Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f \times L \times V_{IN}} \times \left( ESR + \frac{1}{8 \times f \times C_{OUT}} \right)$$

In the case of ceramic capacitors, the output ripple is dominated by the capacitance value because of its low ESR. In the case of tantalum or electrolytic capacitors, the capacitor high ESR dominates the output ripple. Followings are equations for determining appropriate capacitor parameters.

Ⅰ. Ceramic capacitors: choose capacitance value

$$C_{OUT} = \frac{V_{OUT}}{8 \times f^2 \times L \times \Delta V_{OUT}} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Ⅱ. Tantalum or electrolytic capacitors: choose capacitor with ESR value

$$ESR = \frac{\Delta V_{OUT} \times f \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})}$$

## PC Board Layout Checklist

1. The power traces, consisting of the GND, SW and $V_{IN}$ traces, should be kept short, direct and wide.

2. Place $C_{IN}$ near IN pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.

3. The resistive divider $R_2$ and $R_4$ must be connected to FB pin directly as closely as possible.

4. FB is a sensitive node. Please keep it away from switching node SW. A good approach is to route the feedback trace on another layer and have a ground plane between the top and feedback trace routing layer. This reduces EMI radiation on to the DC-DC converter's own voltage feedback trace.
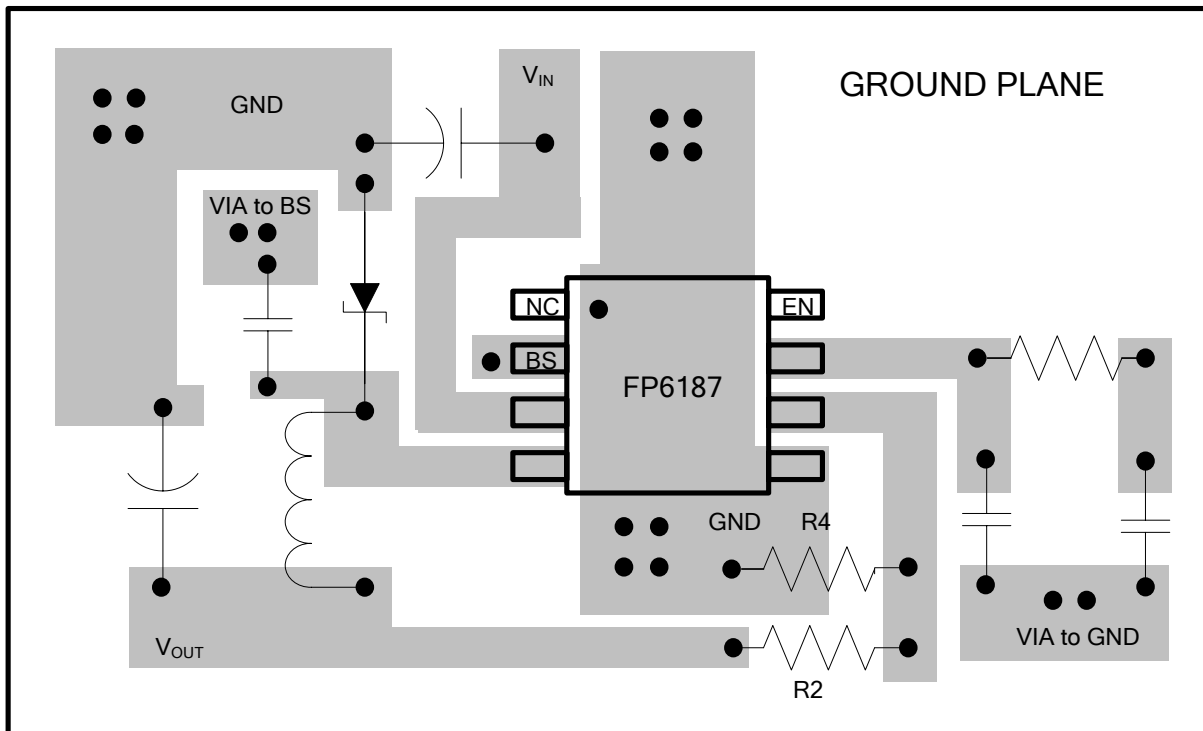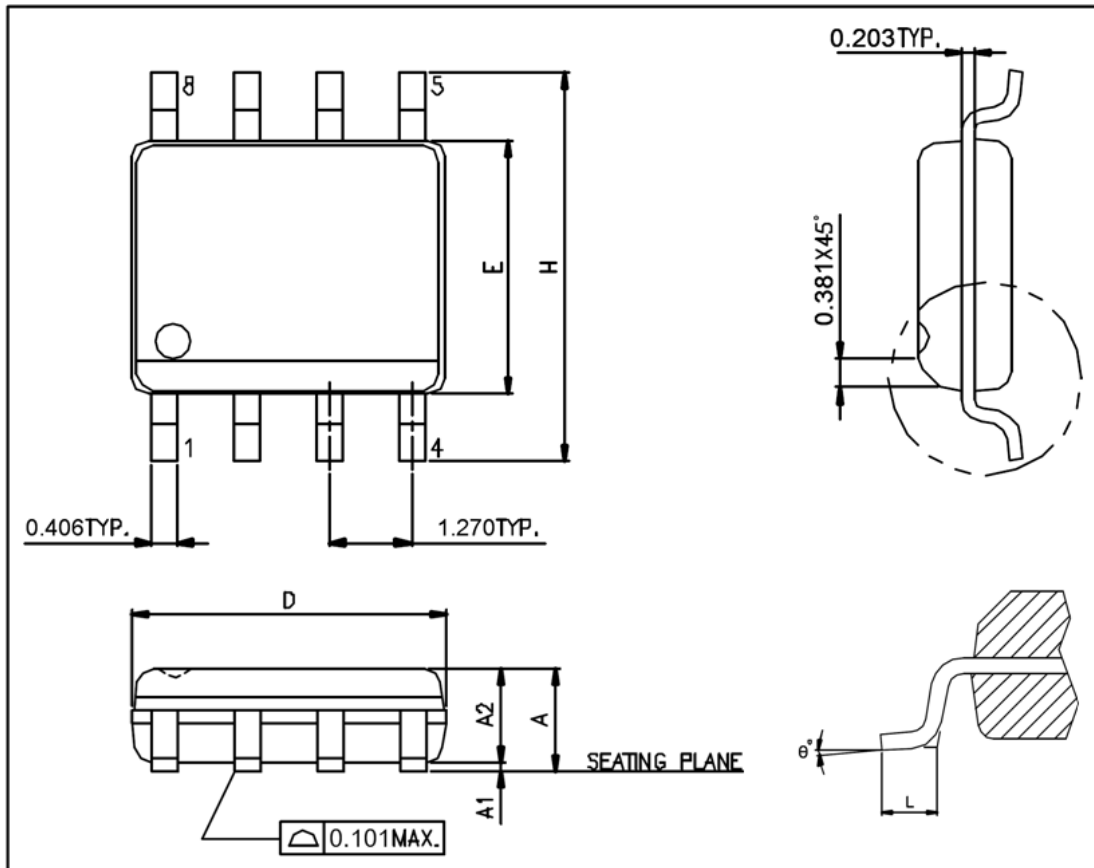
Suggested Layout

## Typical Application
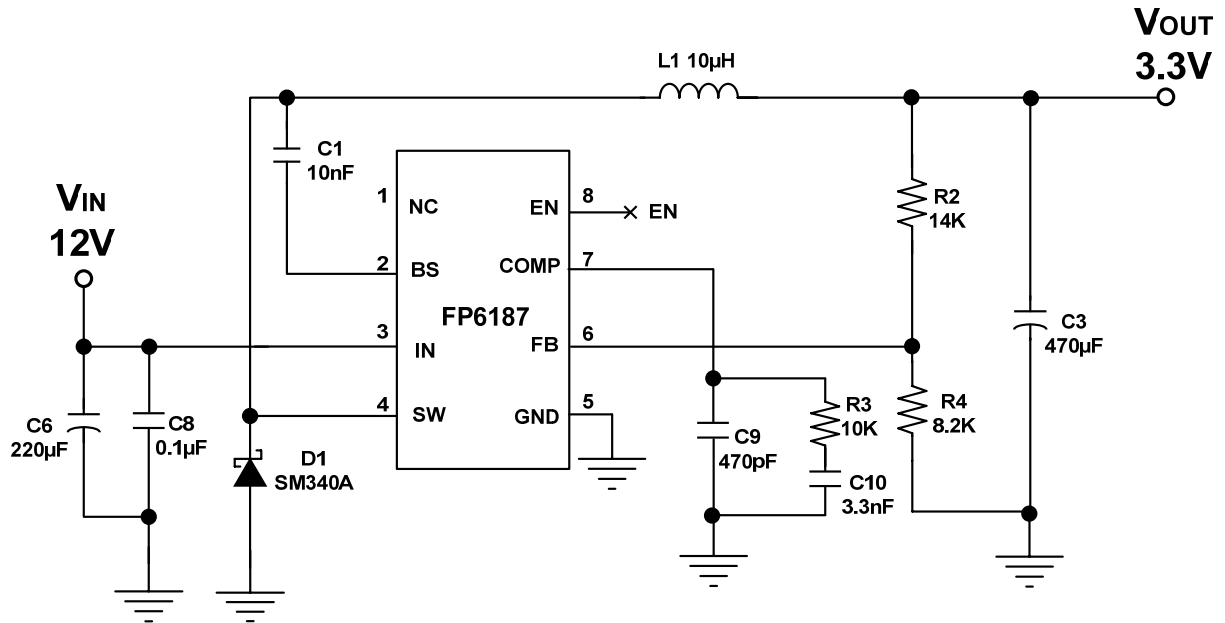
## Package Outline

**SOP-8L**



**UNIT: mm**

| Symbols | Min. (mm) | Max. (mm) |
|---------|-----------|-----------|
| A | 1.346 | 1.752 |
| A1 | 0.101 | 0.254 |
| A2 | 1.092 | 1.498 |
| D | 4.800 | 4.978 |
| E | 3.810 | 3.987 |
| H | 5.791 | 6.197 |
| L | 0.406 | 1.270 |
| θ° | 0° | 8° |

**Note:**

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.

2. Dimension "D" does not include molding flash, protrusions or gate burrs.

3. Dimension "E" does not include inter-lead flash or protrusions.

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