FP6606

USB Type-C Power Delivery and USB HVDCP Controller

Description

FP6606 is a USB PD PHY that enables a USB Type-C port with the Configuration Channel (CC) logic needed for USB Type-C ecosystems. It integrates the physical layer of the USB BMC power delivery (PD) protocol to allow up to 100W of power and support for alternate mode interfaces. An external microprocessor, containing USB Type-C Port Manager (TCPM), communicates with the FP6606 through an I2C interface.

Under control of the TCPM, FP6606 uses the CC pins to determine port attach/detach, cable orientation, role detection, and port control for USB Type-C current mode. The FP6606 can be configured as DFP, UFP, or DRP, depending on the application. The FP6606 implements VBUS detection and discharge for the implementation of a compliant USB Type-C port.

The FP6606 integrates 100mW switch to provide VCONN power for E-mark cable and provides VCONN discharge function. The FP6606 also supports USB Type-C optional features such as audio and debug accessory mode.

Additionally, the FP6606 integrates HiSilicon Fast Charging Protocol (FCP) and Qualcomm® Quick Charge™ 2.0/3.0 (QC 2.0/3.0) USB interface. The FP6606 monitors USB D+/D− data line and automatically adjusts the output voltage depending on different powered device. If the powered device doesn't support USB PD protocol, the FP6606 can support other protocol as mentioned above.

The FP6606 is available in TQFN-24 and TQFN-16 packages.

Features

USB Type-C:

- Supports USB Type-C™ 1.2 and TCPCI 1.2
  - 5V-24 V Power Sourcing and Sinking
  - 100mW VCONN Power (20mA)
- Optimized for Portable Applications with Autonomous Dual Role Port (DRP) Support
- TCPM Configures as :
  - Source, Sink and DRP mode
  - Attach/Detach of USB port
  - Cable Orientation Detection
  - Current Mode Advertisement and Detection
  - Debug and Audio Accessory Support
- Dead Battery Support (Optional)
- VBUS and VCONN Discharge Function
- Support Type-C DRP Try.SRC or Try.SNK

USB PD:

- USB Power Delivery 2.0/ 3.0 Specifications
- Fast Role Swap Support
- Data Chunked and PPS Support

D+/D− Data lines (Source Role Only) :

- Support Qualcomm® Quick Charge™ 2.0/3.0
  - Voltage Range from 3.6V to 12V for Class A and 20V for Class B
- Support HiSilicon Fast Charging Protocol (FCP) & Super Charge Protocol (SCP)
- Automatically Selects FCP and QC2.0/3.0 Protocols
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D− Line
- Supports USB DCP Shorting D+ Line to D− Line per USB Battery Charging Specification, Revision 1.2

Others:

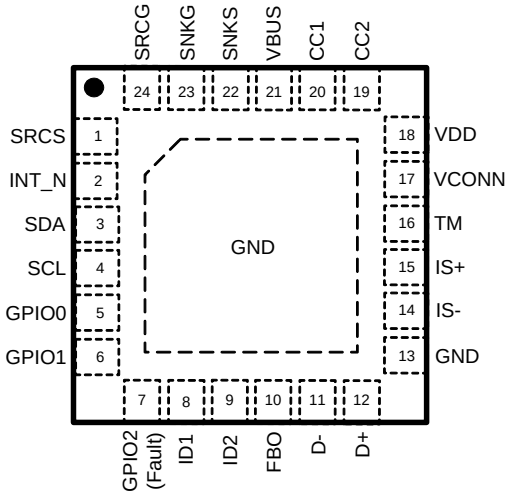
- Control of External N-CH MOSFETs for Source and Sink Power Path
- Fault pin Alarm for VBUS OVP, CC or D+/D− Short to VBUS
- User Defined I/O x 3 pins
- Low Current Consumption(< 30 uA)

Applications

- Adapter, Car Charger
- Wall Charger, Power Banks

Pin Assignments

W8 Package TQFN-24(Exposed Pad, 4mmx4mm)



W5 Package TQFN-16(Exposed Pad, 4mmx4mm)

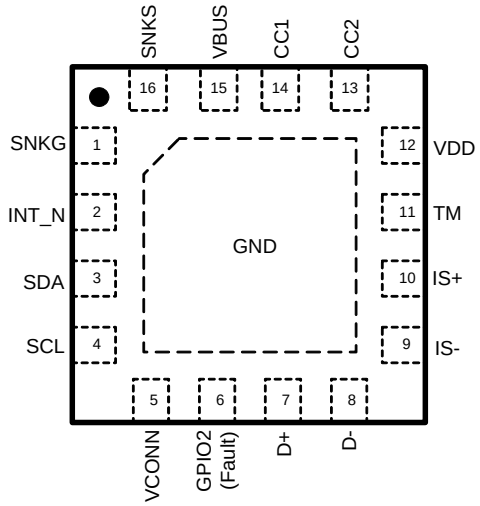


Figure 1. Pin Assignment of FP6606

Ordering Information

FP6606□□

- Package Type
  - W8: TQFN-24(Exposed Pad, 4mmx4mm)
  - W5: TQFN-16(Exposed Pad, 4mmx4mm)
- Dead Battery Function
  - A: Not Support
  - B: Support

Typical Application Circuit

1. Sink/Source – Boost Converter with FBO control

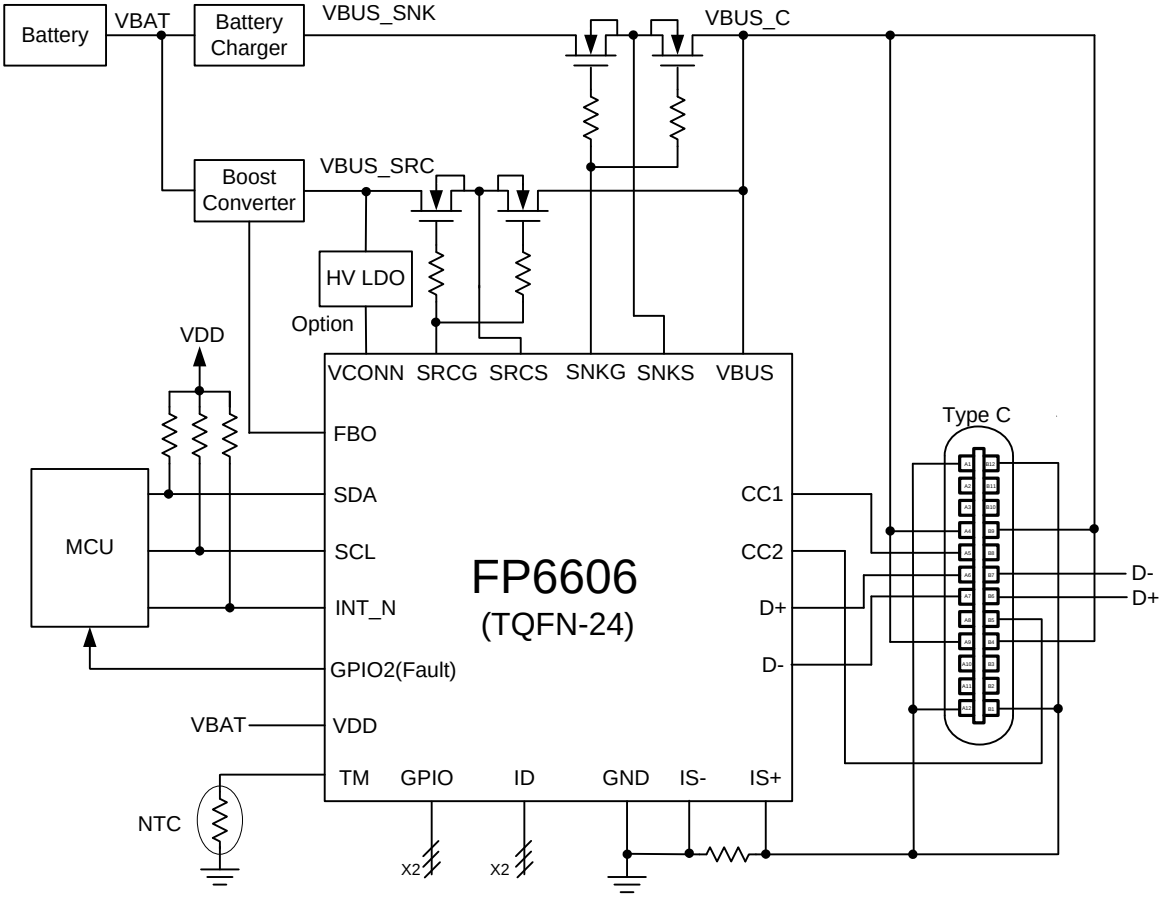


Figure 2. Boost Converter with FBO control circuit

Typical Application Circuit (Continued)

2. Sink/Source – Bi-directional Buck Charger with I2C control

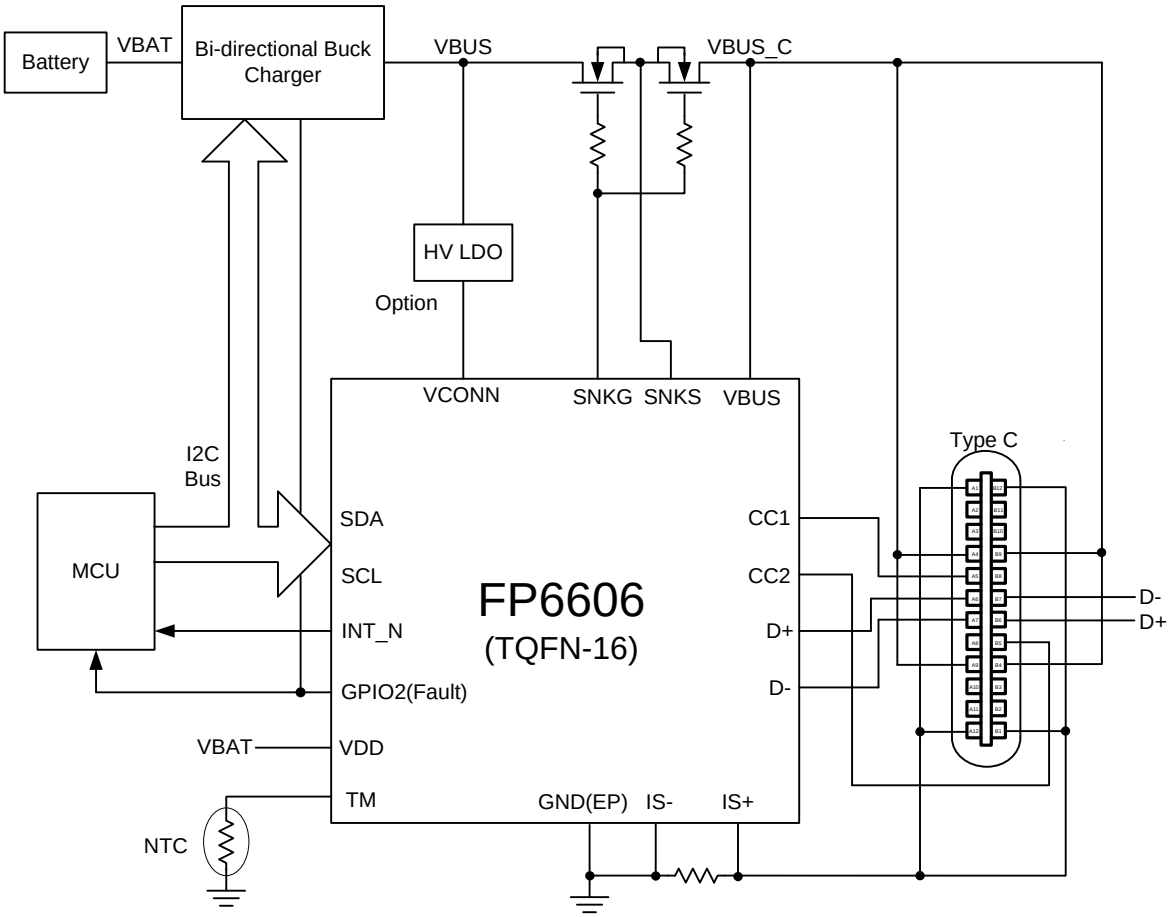


Figure 3. Bi-directional Buck Charger with I2C control circuit

Typical Application Circuit (Continued)

3. Source Only – HV Buck Converter with FBO control

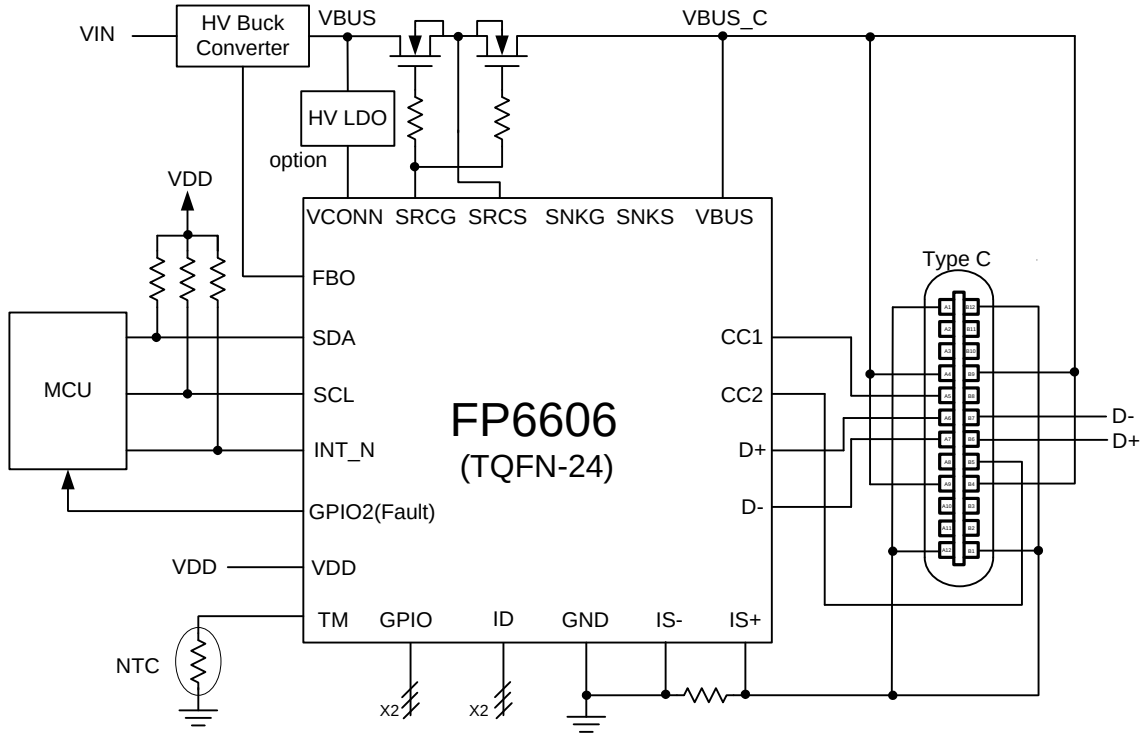


Figure 4. HV Buck Converter with FBO control Circuit

Typical Application Circuit (Continued)

4. Sink/Source – Bi-directional Buck Charger with I2C control - two Type-C ports

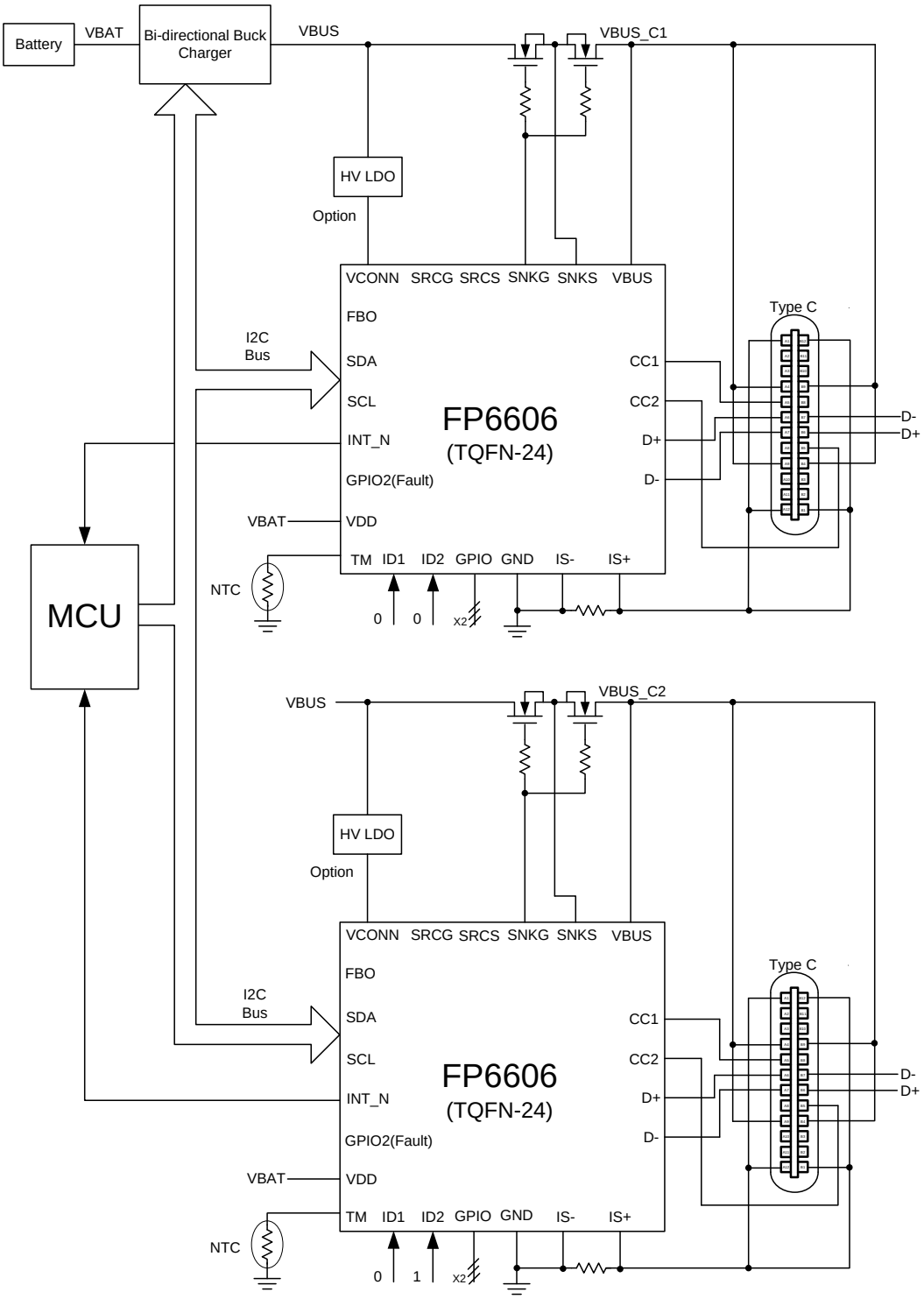


Figure 5. Bi-directional Buck Charger with I2C control - two Type-C ports Circuit

Functional Pin Description

Pin Name	Pin No. (TQFN-24)	Pin No. (TQFN-16)	Pin Function
SRCS	1	-	NMOS source note control(as source).
INT_N	2	2	Open drain output. Asserted low to indicate status change occurred. Requires an external pull-up resistor.
SDA	3	3	I^2C communication data signal. Requires an external pull-up resistor.
SCL	4	4	I^2C communication clock signal. Requires an external pull-up resistor.
GPIO 0~2	5,6,7	6	Programable digital input/ouput pin. The GPIO 2 also can be configued as fault pin.
ID1 & 2	8,9	-	The I^2C slave address selection pins.
FBO	10	-	Feedback output pin. Current sink/source FB node.
D−	11	8	USB D− data line for USB interface.
D+	12	7	USB D+ data line for USB interface.
GND	13	-	Ground.
IS−	14	9	Negative input of a current sense amplifier. Connect to the current sense resistor on the VBUS power path.
IS+	15	10	Positive input of a current sense amplifier. Connect to the current sense resistor on the VBUS power path. This pin could be opened or connected to ground if user want to neglect the current of VBUS power path.
TM	16	11	External thermal sensor connection node (NTC).
VCONN	17	5	4.75V to 5.5V VCONN. VCONN voltage should be at a valid stable value before TCPM turns on the VCONN switch.
VDD	18	12	2.7V to 5.5V positive supply voltage.
CC2	19	13	Type-C configuration channel signal 2.
CC1	20	14	Type-C configuration channel signal 1.
VBUS	21	15	VBUS voltage detection.
SNKS	22	16	NMOS source note control(as sink).
SNKG	23	1	NMOS gate note control(as sink).
SRCG	24	-	NMOS gate note control(as source).

Functional Block Diagram

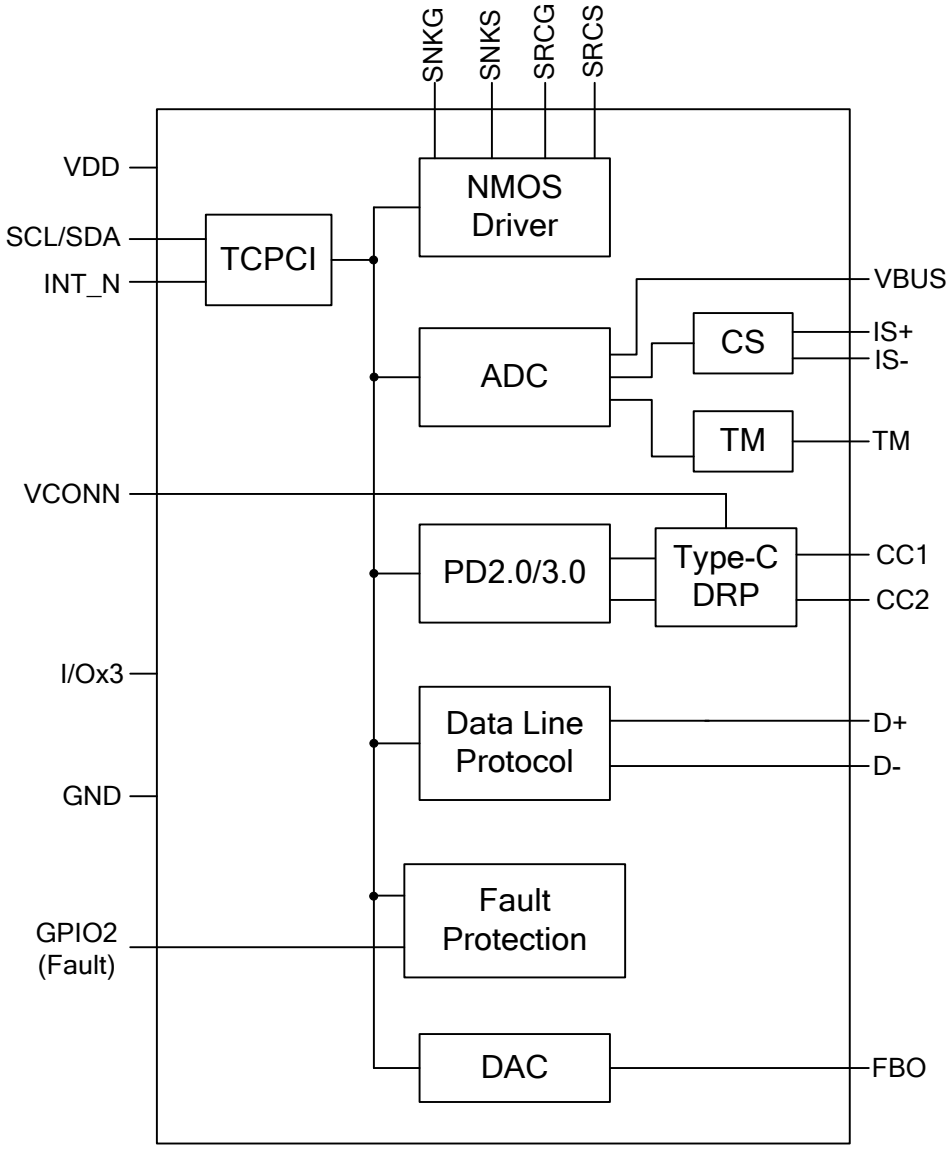


Figure 6. Block Diagram of FP6606

Function Description

Slave Address Selection

FP6606 supports four kinds of slave addresses, which is selected by TCPM. The default slave address of FP6606 is 0x60 and it could be changed by ID1 and ID2 pins through pull-high/low. Please refer to the table as blew.

Slave address	ID1	ID2
0x60	0	0
0x62	0	1
0x64	1	0
0x66	1	1

Dead Battery Function (FP6606B only)

FP6606 could be applied to the power bank system due to the input voltage of FP6606 ranges from 2.7V to 5.5V. Moreover, when the battery is dead, FP6606 will automatically change the supplied power from input pin to VBUS pin and enable the NMOS_SNK driver. Please refer to the register 0xAC for setting the dead battery function.

Overvoltage Protection

FP6606 supports overvoltage protection of VBUS, CC1, CC2, D+ and D− pin. The GPIO 2 (fault pin) will be pulled high when one of these pins is suffered from the high voltage. TCPM monitors the GPIO 2 (fault pin) and the abnormal information is therefore catched immetiatively. Additionally, the setting of OVP protection is assigned to the vendor define registers.

Temperature Measurement

FP6606 provides the TM pin connected to the NTC thermistor. The TM pin could source current and return the voltage on NTC thermistor to the register of FP6606. Therefore, TCPM could access the voltage on NTC thermistor from the register of FP6606 and the temperature could be obatained by simple calculation. Please refer to the register 0xC0[6:5] and 0xC4.

VBUS Control

The FP6606 is a controller so that it must be combined with power stage. The FBO pin of FP6606 must be connected to the feedback node of power stage. The VBUS control of FP6606 is implemented by sourcing/sinking current from FBO pin. Please refer to the register 0xD0~0xD2 for detail information.

Current Measurement

FP6606 could monitor the current flowing from IS+ pin to IS− pin. The current information is returned to register 0xC3. However, FP6606 do not support the over current protection. If the over current protection is needed, it must be implemented by power stage or other protection circuit.

VCONN Over Temperature Protection

VCONN switch is the only probably heating point in FP6606 due to the current limit of the VCONN switch is up to 40mA. When the temperature of the VCONN switch is higher than the 160°C the VCONN switch will be automatically turned off until the temperature decreases to 130°C.

Data Line Interface (D+/D−)

FP6606 supports QC 2.0/3.0/FCP and SCP protocol on the D+/D− data line. The related registers are assigned to the vendor define registers. These registers are public for user and could be managed by TCPM.

When the FP6606 is configured as QC 2.0/3.0/FCP mode, both D+ and D− pin are applied to 2.7V. If sink device has the function of QC 2.0/3.0/FCP, D+ pin will be forced between 0.325V and 2V. In the meanwhile, D+ pin will be automatically connected to D− pin by FP6606 and this process is called the short mode for USB BC1.2 specification. If D+ is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the FP6606 will enter QC 2.0/3.0/FCP operation mode. The QC 2.0/3.0 could be classed as the following table.

D+	D−	Output Voltage
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Continuous mode
0.6V	High-Z	5V (Default)

When the voltage of D+ pin and D− pin simultaneously satisfy these two inequalities VDAT(REF)< D+ <VSEL_REF and D− > VSEL_REF, the FP6606 would enter continuous mode.

In the continuous mode, each voltage pulse on D+ pin generated by sink device is between 1V and 3V. In the meanwhile, the high level of pulse should be keep at least 200us (default). If the specified conditions are satisfied, the FBO pin will sink 2uA (default) per pulse. The maximum sink current is 150uA for output voltage 20V.

In the continuous mode, each voltage pulse on D− pin generated by sink device is between 3V and 1V. At the same time, the low level of pulse should be keep at least 200us (default). If the specified conditions are satisfied, the FBO pin will source 2uA (default) per pulse. The maximum source current is 14uA for output voltage 3.6V.

If the sink device doesn't support QC 2.0/3.0, the FP6601Q will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of D+ pin is therefore lower than VDAT(REF) and the output default voltage 5V is also applied.

Function Description (Continued)

MTP Register table

MTP function in FP6606 indicates thirty-two registers. Each page consists of four registers. Then, each chip includes eight pages. The Reg.0x98~Reg.0x9A are used to operate the MTP registers. The definition of MTP register could be refer to following table. However, both page 0 and page 1 are reserved by vendor.

Chip	Page	Register Name	Register Address	MTP Address
0	0	Reserved	0xA0	0x00
		Reserved	0xA1	0x01
		Reserved	0xA2	0x02
		Reserved	0xA3	0x03
	1	QC_PROTOCOL_CONTROL_BYTE_0	0x9C	0x04
		QC_PROTOCOL_CONTROL_BYTE_1	0x9D	0x05
		Reserved	0x9E	0x06
		Reserved	0x9F	0x07
	2	Reserved	0xA4	0x08
		Reserved	0xA5	0x09
		Reserved	0xA6	0x0A
		Reserved	0xA7	0x0B
	3	Reserved	0xA8	0x0C
		Reserved	0xA9	0x0D
		Reserved	0xAA	0x0E
		Reserved	0xAB	0x0F
	4	DEAD_BATTERY_VOLTAGE_SELECTION	0xAC	0x10
		Reserved	0xAD	0x11
		Reserved	0xAE	0x12
		FACTORY_ID	0xAF	0x13
	5	VENDOR_ID_L	0x00	0x14
		VENDOR_ID_H	0x01	0x15
		USBTYPEC_REV_L	0x06	0x16
		USBTYPEC_REV_H	0x07	0x17
	6	DEVICE_ID_L	0x04	0x18
		DEVICE_ID_H	0x05	0x19
		DEVICE_CAPABILITIES_1_L	0x24	0x1A
		DEVICE_CAPABILITIES_1_H	0x25	0x1B
	7	DEVICE_CAPABILITIES_2_L	0x26	0x1C
		DEVICE_CAPABILITIES_2_H	0x27	0x1D
		STANDARD_INPUT_CAPABILITIES	0x28	0x1E
		STANDARD_OUTPUT_CAPABILITIES	0x29	0x1F

Absolute Maximum Ratings (Note 1)

- Supply voltage VDD ---------- -0.3V to +6.5V
- VCONN ---------- -0.3V to +6.5V
- INT_N, SDA, SCL ---------- -0.3V to +24V
- CC1, CC2, VBUS ---------- -0.3V to +24V
- VBUS ---------- -0.3V to +28V
- D+, D− ---------- -0.3V to +12V
- SRCS, SNKS, SRCG, SNKG ---------- -0.3V to +35V
- GPIO 0~4 ---------- -0.3V to +6.5V
- IS+, IS−, FBO, TM ---------- -0.3V to +6.5V
- Maximum junction temperature (T_J)---------- +150℃
- Storage temperature (T_{Stg}) ---------- -65℃ to +150℃
- Lead temperature (Soldering, 10sec.) ---------- +260°C
- Power dissipation @T_A=25℃, (P_D)
  - TQFN-16---------- 2 W
  - TQFN-24---------- 2 W
- Package thermal resistance, (θ_{JA}) (Note 2)
  - TQFN-16---------- 51 °C/W
  - TQFN-24---------- 50 °C/W
- Package thermal resistance, (θ_{JC})
  - TQFN-16---------- 25 °C/W
  - TQFN-24---------- 19 °C/W

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2: θ_{JA} is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7.

Recommended Operating Conditions

- Input supply voltage (VDD)---------- +2.7V to +5.5V
- VCONN voltage range ---------- +2.7V to +5.5V
- VBUS voltage ---------- 0V to +24V
- System I^2C voltage range that SDA and SCL are pulled up to ---------- +1.65V to +5.5V
- Operating temperature range (T_A)---------- -40°C to +85°C
- Junction temperature (T_J) ---------- -40°C to +125°C

Electrical Characteristics

General-Electrical Characteristics						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input Power						
VDD input voltage range	V_{VDD}		2.7		5.5	V
VDD voltage rising release voltage	$V_{BAT\_UVLOR\_LK(VTH)}$	DEAD_BAT_SEL, Reg.0xAC=0x01		2.9		V
VDD voltage falling lockout voltage	$V_{BAT\_UVLOF\_LK(VTH)}$	DEAD_BAT_SEL, Reg.0xAC=0x01		2.7		V
VDD voltage lockout hysteresis voltage	$V_{BAT\_UVLOF\_LK(HYS)}$			200		mV
In dead battery mode, VBUS turn on voltage	$V_{BUS\_NMOS\_ON}$		4		6.5	V
N Channel MOSFET Gate Driver						
Sourcing current of SNKG (Note 3)				TBD		µA
Sourcing voltage (ON) between SNKG and SNKS (Note 3)			5		15	V
Sourcing current of SRCG (Note 3)				TBD		µA
Sourcing voltage (ON) between SRCG and SRCS (Note 3)			5		15	V
Current Sense (IS+ and IS-)						
Current sense range			0		6.4	A
Resolution				TBD		
Accuracy				TBD		
GPIO0~GPIO2						
Logic-low threshold voltage for inputs	V_{IL_GPIO}				1.97	V
Logic-high threshold voltage for inputs	V_{IH_GPIO}		2.6			V
Logic-low threshold voltage for outputs	V_{OL_GPIO}					V
Logic-high threshold voltage for outputs	V_{OH_GPIO}					V
Power Consumption						
UFP current consumption in unattached.SNK	$I_{(UNATTACHED\_UFP)}$	VDD=3.7V		TBD		µA
DRP current consumption while toggling between unattached.SNK and unattached	$I_{(UNATTACHED\_DRP)}$	VDD=3.7V		TBD		µA
DFP current consumption in unattached	$I_{(UNATTACHED\_DFP)}$	VDD=3.7V		TBD		µA
UFP current consumption in attached.SNK active mode. PD disabled	$I_{(ACTIVE\_UFP)}$	VDD=3.7V		TBD		µA
UFP current consumption in attached.SNK with PD enabled and transmitting continuous BIST carrier mode 2	$I_{(ACTIVE\_UFP\_PD)}$	VDD = 3.7V; TX_CARRIER_MODE2_SEL = 1;		5.2		mA
Control Pins: INT_N						
INT_N leakage	$I_{(INTN\_LEAK)}$	VDD = 0V; 0 < INT_N < 3.3V	-1		1	µA
Low-level signal output voltage	V_{OL}	IOL = -2mA			0.4	V

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I2C (SDA and SCL). VDD must be above 3V to operate at 3.3V I2C levels						
High-level input signal voltage	$V_{IH(I2C)}$		1.2			V
Low-level input signal voltage	$V_{IL(I2C)}$				0.4	V
Low-level signal output voltage (open-drain)	$V_{OL(I2C)}$				0.4	V
Low level output current	$I_{OL(I2C)}$		6			mA
Leakage through SDA and SCL pins	$I_{(I2C\_LKG)}$	VDD = 0V; pin pulled up to 3.6V	-1		1	µA
Capacitance for SDA and SCL pins	$C_{(I2C)}$				10	pF
I2C bus capacitance for FM+ (1MHz)	$C_{(I2C\_FM+\_BUS)}$				150	pF
I2C bus capacitance for FM (400KHz)	$C_{(I2C\_FM\_BUS)}$				150	pF
External resistors on both SDA and SCL when operating at FM+ (1MHz)	$R_{(EXT\_I2C\_FM+)}$	C(I2C_FM+_BUS) = 150pF	620	820	910	Ω
External resistors on both SDA and SCL when operating at FM (400KHz)	$R_{(EXT\_I2C\_FM)}$	C(I2C_FM_BUS) = 150pF	620	1500	2200	Ω
VBUS						
Bleed discharge is a low current discharge to provide a minimum load current if needed	$R_{(Bleed)}$		8	10	12.5	kΩ
Force discharge resistance	$R_{(FA\_Discharge)}$			400		Ω
VBUS_voltage register measurement accuracy	$V_{(VBUS\_MEASURE\_ACC)}$		-2		2	%
OTSD						
TJ over temperature trip threshold resulting in VCONN turn off and flag set	$T_{(OTSD1)}$			150		°C
FBO Pin-QC mode						
Up/down current step (QC 2.0/3.0)	$I_{UP,\ IDOWN}$	IUP = 40µA (9V), 70µA (12V), IDOWN = 14µA (3.6V).		2		µA

Electrical Characteristics (Continued)

USB Power Delivery- Electrical Characteristics						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
CC Pins (CC1 and CC2)						
Voltage on both CC pins when in dead battery and the attached DFP is presenting default current advertisement	$V_{CC(USB\_DB)}$	VDD = 0V	0.25		1.5	V
Voltage on both CC pins when in dead battery and the attached DFP is presenting medium current (1.5A) advertisement	$V_{CC(MED\_DB)}$	VDD = 0V	0.45		1.5	V
Voltage on both CC pins when in dead battery and the attached DFP is presenting high current (3.0A) advertisement	$V_{CC(HIGH\_DB)}$	VDD = 0V	0.85		2.45	V
Pull-down resistor when in UFP or DRP mode	$R_{(CC\_RD)}$	VDD = 2.7V to 5.5V	4.59	5.1	5.61	kΩ
Pull-down resistor for active cable	$R_{(CC\_RA)}$	VDD = 2.7V to 5.5V	0.8	1	1.2	kΩ
Leakage current through CC pins	$I_{CC(LKG)}$	VDD = 0V; VCONN = 0V; CC pin = 5.5V			1.36	mA
Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising default current source capability	$V_{(UFP\_CC\_USB)}$		0.25		0.61	V
Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising medium (1.5A) current source capability	$V_{(UFP\_CC\_MED)}$		0.7		1.16	V
Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising high (3.0A) current source capability	$V_{(UFP\_CC\_HIGH)}$		1.31		2.04	V
Voltage threshold for detecting a UFP attach when FP6606 is advertising default current source capability	$V_{TH(DFP\_CC\_USB)}$		1.51	1.6	1.64	V
Voltage threshold for detecting a UFP attach when FP6606 is advertising medium current (1.5A) source capability	$V_{TH(DFP\_CC\_MED)}$		1.51	1.6	1.64	V
Voltage threshold for detecting a UFP attach when FP6606 is advertising high current (3.0A) source capability	$V_{TH(DFP\_CC\_HIGH)}$		2.46	2.6	2.74	V
Voltage threshold for detecting a active cable attach when advertising default current	$V_{TH(AC\_CC\_USB)}$		0.15	0.2	0.25	V
Voltage threshold for detecting a active cable attach when advertising medium current	$V_{TH(AC\_CC\_MED)}$		0.35	0.4	0.45	V
Voltage threshold for detecting a active cable attach when advertising high current	$V_{TH(AC\_CC\_HIGH)}$		0.76	0.8	0.84	V
Default mode pull-up current source when advertising default current	$I_{CC(DEFAULT\_P)}$		64	80	96	µA
Medium (1.5A) mode pull-up current source when advertising medium current	$I_{CC(MED\_P)}$		165.6	180	194.4	µA
High (3.0A) mode pull-up current source when advertising high current	$I_{CC(HIGH\_P)}$	VDD > 3.0V	303.6	330	356.4	µA

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output impedance of CC1/CC2 during TX when operating in PD mode and driving the CC line (Note 3)	$R_{TX(PD)}$	At 750KHz	33	48	75	Ω
Fast role swap request transmit driver resistance (excluding cable resistance)	$R_{TX(FRS\_PD)}$				5	Ω
Transmit high voltage when operating in PD mode	$V_{OH(PD)}$		1.05	1.125	1.2	V
Transmit low voltage when operating in PD mode	$V_{OL(PD)}$				0.07	V
Receiver input impedance. Does not include pull-up or pull-down resistance from cable detect	$R_{RX(PD)}$	TX is Hi-Z	1			MΩ
Fast role swap request voltage detection threshold	$V_{RX(FRS\_PD)}$		0.49	0.52	0.55	V
Input high voltage when sourcing power. Selected when POWER_ROLE = 1	$V_{IH(PD\_SRC)}$		0.8925		1.5325	V
Input high voltage when sinking power. Selected when POWER_ROLE = 0	$V_{IH(PD\_SNK)}$		0.6425		1.5325	V
Input low voltage when sourcing power. Selected when POWER_ROLE = 1	$V_{IL(PD\_SRC)}$		-0.3325		0.4825	V
Input low voltage when sinking power. Selected when POWER_ROLE = 0	$V_{IL(PD\_SNK)}$		-0.3325		0.2325	V
External shunt capacitance on both CC1 and CC2	$C_{RX(SHUNT)}$		200		450	pF
VCONN						
RON for VCONN power FET	$R_{DS(ON)}$			6	15	Ω
Voltage to pass through VCONN power FET	$V_{(PASS)}$			5		V
VCONN current limit; VCONN is connected above this voltage	$I_{(VCONN)}$		30	40	50	mA
Threshold for detecting VCONN present	$V_{(VCONN\_PRES)}$				2.4	V
Resistance to GND when VCONN discharge is enabled	$R_{(VCONN\_DIS)}$		4.59	5.1	5.61	kΩ
QC-EC						
High Voltage Dedicated Charging Port (HVDCP)						
Data detect voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output voltage selection reference	V_{SEL_REF}		1.8	2.0	2.2	V
D− pull-down resistance	$R_{D-(DWN)}$			20		kΩ
D+ leakage resistance	$R_{DAT-LKG}$	VDD =3.2-6.4V,VD+=0.6-3.6V Switch SW1=Off	300	500	800	kΩ
Switch SW1 on-resistance	$R_{DS\_ON\_N1}$	VDD =5V,SW1=200μA			40	Ω
Apple 2.4A Mode						
D+_2.7V/D−_2.7V line output voltage		VDD > 3V	2.57	2.7	2.84	V
D+_2.7V/D−_2.7V line output impedance		VDD > 3V		33.6		kΩ

Note 3: Not production tested.

Timing Requirements

General-Timing Requirements						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I2C(SDA and SCL)						
SCL clock frequency	F_{SCL}		0.001		1	MHz
Hold time (repeated) start condition	$t_{HD;STA}$		0.26			µs
Low period of SCL	t_{LOW}		0.5			µs
High period of SCL	t_{HIGH}		0.26			µs
Setup time for a repeated start condition	$t_{SU;STA}$		0.26			µs
Data hold time	$t_{HD;DAT}$		0			µs
Data setup time	$t_{SU;DAT}$		50			µs
Setup time for STOP condition	$t_{SU;STOP}$		0.26			µs
Bus free time between STOP and START condition	t_{BUF}		0.5			µs
Data valid time	$t_{VD;DAT}$				0.45	µs
Data valid acknowledge time	$t_{VD;ACK}$				0.45	µs
Rise time of both SDA and SCL	t_{R_I2C}	30% to 70%			120	Ns
Fall time of both SDA and SCL	t_{F_I2C}	70% to 30%	14		120	ns
Power-Up Requirements						
Time from VDD (min) to FP6606 asserts INT_N low	$t_{INT\_N\_LOW}$	Measured from VDD(min) to INT_N pin at VOL(min).			4	ms
VDD rise time	t_{VDD_RISE}	Measured from 0V to VDD(min)			40	ms
USB PD-Timing						
CC Pins (CC1 and CC2)						
Bit rate	F_{br_PD}		270	300	330	Kbps
Unit interval	t_{UI_PD}		3.03	3.3	3.7	µs
Rise time	t_{RISE_PD}	10% to 90%; CRX(SHUNT) = 200pF	300			ns
Fall time	t_{FALL_PD}	90% to 10%; CRX(SHUNT) = 200pF	300			ns
Rx Bandwidth limiting filter	$t_{RxFilter}$		100			ns
Time from the end of last bit of a frame until the state of the first bit of the next pre-amble	$t_{InterFrameCap}$		25		50	Ms
Time before the start of the first bit of the preamble when the transmitter shall start driving the line	$t_{StartDrive}$		-1		1	Ms
Time to cease driving the line after the end of the last bit of a frame	$t_{EndDriveBMC}$				23	Ms
Time to cease driving the line after the final high-to-low transition	$t_{HoldLowBMC}$		1		23	µs

Timing Requirements (Continued)

General-Timing Requirements						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Transitions for signal detect	$n_{TransitionCount}$	Number of transitions to be detected to declare bus non-idle	3			
Fast role swap request transmit duration	$t_{FRSWAPTX}$		60		120	μs
Fast role swap detection time	$t_{FRSWAPRX}$		30		50	μs
VCONN Fault						
Delay from VCONN fault detected to VCONN fault status flag set	$t_{VCONN\_FAULT\_DLY}$				20	μs
Delay from VCONN fault detected to VCONN switch opened	t_{VCONN_OPEN}				50	ns
Sampling Timings						
Delay from VCONN fault detected to VCONN fault status flag set	$t_{CC\_SAMPLE\_RATE}$	CC_SAMPLE_RATE = 2'b01		2		ms
The sampling interval of VBUS voltage	$t_{VBUSINRATE}$	CC_SAMPLE_RATE = 2'b01		2		ms

Qualcomm® Quick Charge-Timing Requirements						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
TCPC Timing Constraints						
Time between I2C STOP and first bit SOP	$t_{Buffer2Cc}$				195	μs
Time between last bit of EOP and Rx buffer ready	$t_{Cc2Buffer}$				50	μs
Time between status change occurs and status register(s) updated	t_{SetReg}				50	μs
Time between status change occurs and status register(s) updated	$t_{CcStatusDelay}$				200	μs
Time from last I2C transaction or ALERT# pin assertion to entering Error Recovery (Watchdog function)	$t_{HVWatchdog}$		650		5000	ms
High Voltage Dedicated Charging Port (HVDCP)						
D+ high glitch filter time	$T_{GLITCH(BC)-D+\_H}$		1000	1250	1500	ms
D- low glitch filter time	$T_{GLITCH(BC)-D-\_L}$			1		ms
Output voltage glitch filter time	$T_{GLITCH(V)\ CHANGE}$		20	40	60	ms
Continuous mode glitch filter time	$T_{GLITCH-CONT-CHANGE}$		100		200	μs

Register Maps

Address	Register Name	Reset	Definition
0x00	VENDOR_ID_L	0x5B	
0x01	VENDOR_ID_H	0x2E	
0x02	PRODUCT_ID_L	0x06	
0x03	PRODUCT_ID_H	0x66	
0x04	DEVICE_ID_L	0x00	
0x05	DEVICE_ID_H	0x00	
0x06	USBTYPEC_REV_L	0x00	
0x07	USBTYPEC_REV_H	0x00	
0x08	USBPD_REV_VER_L	0x11	
0x09	USBPD_REV_VER_H	0x30	
0x0A	PD_INTERFACE_REV_L	0x12	
0x0B	PD_INTERFACE_REV_H	0x10	
0x0C ~ 0x0F	Reserved	0x00	Reserved
0x10	ALERT_L	0x02	
0x11	ALERT_H	0x02	
0x12	ALERT_MASK_L	0xFF	
0x13	ALERT_MASK_H	0x0F	
0x14	POWER_STATUS_MASK	0xFF	
0x15	FAULT_STATUS_MASK	0xFF	
0x16 ~ 0x18	Reserved	0x00	Reserved
0x19	TCPC_CONTROL	0x00	
0x1A	ROLE_CONTROL	0x0A	
0x1B	FAULT_CONTROL	0x00	
0x1C	POWER_CONTROL	0x60	
0x1D	CC_STATUS	0x10	
0x1E	POWER_STATUS	0x00	
0x1F	FAULT_STATUS	0x80	
0x20 ~ 0x22	Reserved	0x00	Reserved
0x23	COMMAND	0x00	
0x24	DEVICE_CAPABILITIES_1_L	0xD8	
0x25	DEVICE_CAPABILITIES_1_H	0x1E	
0x26	DEVICE_CAPABILITIES_2_L	0xC1	
0x27	DEVICE_CAPABILITIES_2_H	0x01	
0x28	STANDARD_INPUT_CAPABILITIES	0x00	
0x29	STANDARD_OUTPUT_CAPABILITIES	0x00	
0x2A ~ 0x2D	Reserved	0x00	Reserved
0x2E	MESSAGE_HEADER_INFO	0x02	
0x2F	RECEIVE_DETECT	0x00	
0x30	RECEIVE_BYTE_COUNT	0x00	Number of Bytes in the RECEIVE_BUFFER that are not stale.
0x31	RX_BUF_FRAME_TYPE	0x00	Type of received frame (with a reference to a description of the register)
0x32	RX_BUF_HEADER_BYTE_0	0x00	Byte 0 (bits 7..0) of RX message header
0x33	RX_BUF_HEADER_BYTE_1	0x00	Byte 1 (bits 15..8) of RX message header
0x34	RX_BUF_OBJ1_BYTE_0	0x00	RX Byte 0 (bits 7..0) of 1st data object
0x35	RX_BUF_OBJ1_BYTE_1	0x00	RX Byte 1 (bits 15..8) of 1st data object
0x36	RX_BUF_OBJ1_BYTE_2	0x00	RX Byte 2 (bits 23..16) of 1st data object
0x37	RX_BUF_OBJ1_BYTE_3	0x00	RX Byte 3 (bits 31..24) of 1st data object
0x38	RX_BUF_OBJ2_BYTE_0	0x00	RX Byte 0 (bits 7..0) of 2nd data object
0x39	RX_BUF_OBJ2_BYTE_1	0x00	RX Byte 1 (bits 15..8) of 2nd data object
0x3A	RX_BUF_OBJ2_BYTE_2	0x00	RX Byte 2 (bits 23..16) of 2nd data object
0x3B	RX_BUF_OBJ2_BYTE_3	0x00	RX Byte 3 (bits 31..24) of 2nd data object
0x3C	RX_BUF_OBJ3_BYTE_0	0x00	RX Byte 0 (bits 7..0) of 3rd data object
0x3D	RX_BUF_OBJ3_BYTE_1	0x00	RX Byte 1 (bits 15..8) of 3rd data object
0x3E	RX_BUF_OBJ3_BYTE_2	0x00	RX Byte 2 (bits 23..16) of 3rd data object
0x3F	RX_BUF_OBJ3_BYTE_3	0x00	RX Byte 3 (bits 31..24) of 3rd data object

Register Maps (Continued)

Address	Register Name	Reset	Definition
0x40	RX_BUF_OBJ4_BYTE_0	0x00	RX Byte 0 (bits 7..0) of 4th data object
0x41	RX_BUF_OBJ4_BYTE_1	0x00	RX Byte 1 (bits 15..8) of 4th data object
0x42	RX_BUF_OBJ4_BYTE_2	0x00	RX Byte 2 (bits 23..16) of 4th data object
0x43	RX_BUF_OBJ4_BYTE_3	0x00	RX Byte 3 (bits 31..24) of 4th data object
0x44	RX_BUF_OBJ5_BYTE_0	0x00	RX Byte 0 (bits 7..0) of 5th data object
0x45	RX_BUF_OBJ5_BYTE_1	0x00	RX Byte 1 (bits 15..8) of 5th data object
0x46	RX_BUF_OBJ5_BYTE_2	0x00	RX Byte 2 (bits 23..16) of 5th data object
0x47	RX_BUF_OBJ5_BYTE_3	0x00	RX Byte 3 (bits 31..24) of 5th data object
0x48	RX_BUF_0BJ6_BYTE_0	0x00	RX Byte 0 (bits 7..0) of 6th data object
0x49	RX_BUF_OBJ6_BYTE_1	0x00	RX Byte 1 (bits 15..8) of 6th data object
0x4A	RX_BUF_OBJ6_BYTE_2	0x00	RX Byte 2 (bits 23..16) of 6th data object
0x4B	RX_BUF_OBJ6_BYTE_3	0x00	RX Byte 3 (bits 31..24) of 6th data object
0x4C	RX_BUF_OBJ7_BYTE_0	0x00	RX Byte 0 (bits 7..0) of 7th data object
0x4D	RX_BUF_OBJ7_BYTE_1	0x00	RX Byte 1 (bits 15..8) of 7th data object
0x4E	RX_BUF_OBJ7_BYTE_2	0x00	RX Byte 2 (bits 23..16) of 7th data object
0x4F	RX_BUF_OBJ7_BYTE_3	0x00	RX byte 3 (bits 31..24) of 7th data object
0x50	TRANSMIT	0x00	Retry count and SOP* TX type
0x51	TRANSMIT_BYTE_COUNT	0x00	The number of bytes the TCPM will write
0x52	TX_BUF_HEADER_BYTE_0	0x00	Byte 0 (bits 7..0) of TX message header
0x53	TX_BUF_HEADER_BYTE_1	0x00	Byte 1 (bits 15..8) of TX message header
0x54	TX_BUF_OBJ1_BYTE_0 / Extend header byte 0	0x00	TX Byte 0 (bits 7..0) of 1st data object
0x55	TX_BUF_OBJ1_BYTE_1 / Extend header byte 1	0x00	TX Byte 1 (bits 15..8) of 1st data object
0x56	TX_BUF_OBJ1_BYTE_2	0x00	TX Byte 2 (bits 23..16) of 1st data object
0x57	TX_BUF_OBJ1_BYTE_3	0x00	TX Byte 3 (bits 31..24) of 1st data object
0x58	TX_BUF_OBJ2_BYTE_0	0x00	TX Byte 0 (bits 7..0) of 2nd data object
0x59	TX_BUF_OBJ2_BYTE_1	0x00	TX Byte 1 (bits 15..8) of 2nd data object
0x5A	TX_BUF_OBJ2_BYTE_2	0x00	TX Byte 2 (bits 23..16) of 2nd data object
0x5B	TX_BUF_OBJ2_BYTE_3	0x00	TX Byte 3 (bits 31..24) of 2nd data object
0x5C	TX_BUF_OBJ3_BYTE_0	0x00	TX Byte 0 (bits 7..0) of 3rd data object
0x5D	TX_BUF_OBJ3_BYTE_1	0x00	TX Byte 1 (bits 15..8) of 3rd data object
0x5E	TX_BUF_OBJ3_BYTE_2	0x00	TX Byte 2 (bits 23..16) of 3rd data object
0x5F	TX_BUF_OBJ3_BYTE_3	0x00	TX Byte 3 (bits 31..24) of 3rd data object
0x60	TX_BUF_OBJ4_BYTE_0	0x00	TX Byte 0 (bits 7..0) of 4th data object
0x61	TX_BUF_OBJ4_BYTE_1	0x00	TX Byte 1 (bits 15..8) of 4th data object
0x62	TX_BUF_OBJ4_BYTE_2	0x00	TX Byte 2 (bits 23..16) of 4th data object
0x63	TX_BUF_OBJ4_BYTE_3	0x00	TX Byte 3 (bits 31..24) of 4th data object
0x64	TX_BUF_OBJ5_BYTE_0	0x00	TX Byte 0 (bits 7..0) of 5th data object
0x65	TX_BUF_OBJ5_BYTE_1	0x00	TX Byte 1 (bits 15..8) of 5th data object
0x66	TX_BUF_OBJ5_BYTE_2	0x00	TX Byte 2 (bits 23..16) of 5th data object
0x67	TX_BUF_OBJ5_BYTE_3	0x00	TX Byte 3 (bits 31..24) of 5th data object
0x68	TX_BUF_OBJ6_BYTE_0	0x00	TX Byte 0 (bits 7..0) of 6th data object
0x69	TX_BUF_OBJ6_BYTE_1	0x00	TX Byte 1 (bits 15..8) of 6th data object
0x6A	TX_BUF_OBJ6_BYTE_2	0x00	TX Byte 2 (bits 23..16) of 6th data object
0x6B	TX_BUF_OBJ6_BYTE_3	0x00	TX Byte 3 (bits 31..24) of 6th data object
0x6C	TX_BUF_OBJ7_BYTE_0	0x00	TX Byte 0 (bits 7..0) of 7th data object
0x6D	TX_BUF_OBJ7_BYTE_1	0x00	TX Byte 1 (bits 15..8) of 7th data object
0x6E	TX_BUF_OBJ7_BYTE_2	0x00	TX Byte 2 (bits 23..16) of 7th data object
0x6F	TX_BUF_OBJ7_BYTE_3	0x00	TX Byte 3 (bits 31..24) of 7th data object

Register Maps (Continued)

Address	Register Name	Reset	Definition
0x70	VBUS_VOLTAGE_L	0x00	LSB of VBUSIN measured voltage in 25mV steps.
0x71	VBUS_VOLTAGE_H	0x00	MSB of VBUSIN measured voltage in 25mV steps.
0x72	VBUS_SINK_DISCONNECT_THRESHOLD_L	0xC8	
0x73	VBUS_SINK_DISCONNECT_THRESHOLD_H	0x00	
0x74	VBUS_STOP_DISCHARGE_THRESHOLD_L	0x20	
0x75	VBUS_STOP_DISCHARGE_THRESHOLD_H	0x00	
0x76	VBUS_VOLTAGE_ALARM_HI_CFG_L	0x00	
0x77	VBUS_VOLTAGE_ALARM_HI_CFG_H	0x00	
0x78	VBUS_VOLTAGE_ALARM_LO_CFG_L	0x00	
0x79	VBUS_VOLTAGE_ALARM_LO_CFG_H	0x00	
0x7A ~ 0x7F	Reserved	0x00	Reserved
Vendor Defined Space (0x80 ~ 0xDF)			
0x80	SYSTEM_CONTROL_BYTE_0	0x10	
0x81	SYSTEM_CONTROL_BYTE_1	0x00	
0x82	Reserved	0x00	Reserved
0x83	MODE_STATUS_BYTE_0	0x01	
0x84	MODE_STATUS_BYTE_1	0x10	Reserved
0x85	EXTERNAL_NMOS_CONTROL	0x00	
0x86	SYSTEM_CONTROL_BYTE_2	0x00	
0x87 ~ 0x8F	Reserved	0x00	Reserved
0x90	VENDOR_INTERRUPTS_BYTE_0	0x00	
0x91	VENDOR_INTERRUPTS_BYTE_1	0x00	
0x92	VENDOR_INTERRUPTS_MASK_BYTE_0	0x00	
0x93	VENDOR_INTERRUPTS_MASK_BYTE_1	0x00	
0x94	CC_GENERAL_CONTROL	0x04	
0x95 ~ 0x97	Reserved	0x00	Reserved
0x98	MTP_CONTROL_BYTE_0	0x00	
0x99	MTP_CONTROL_BYTE_1	0x00	
0x9A	MTP_PASSWORD	0x00	
0x9B	Reserved	0x00	Reserved
0x9C	QC_PROTOCOL_CONTROL_BYTE_0	0x83	
0x9D	QC_PROTOCOL_CONTROL_BYTE_1	0x00	
0x9E ~ 0x9F	Reserved	0x00	Reserved
0xA0 ~ 0xAB	Reserved	0x00	Reserved
0xAC	DEAD_BATTERY_VOLTAGE_SELECTION	0x01	
0xAD ~ 0xAF	Reserved	0x30	Reserved
0xB0 ~ 0xBF	Reserved	0x00	Reserved
0xC0	ADC_CONTROL	0x81	
0xC1 ~ 0xC2	Reserved	0x00	Reserved
0xC3	ADC_IBUS_DATA	0x00	
0xC4	ADC_TEMPERATURE_DATA	0x00	
0xC5 ~ 0xC7	Reserved	0x00	Reserved
0xC8	GPIO_DIRECTION_CONTROL	0x00	
0xC9	GPIO_OUTPUT_DATA	0x00	
0xCA	GPIO_INPUT_DATA	0x00	
0xCB	DRP_POWER_SAVING	0x00	Reserved
0xCC	OVER_VOLTAGE_DETECT	0x00	
0xCD	OVER_VOLTAGE_STATUS	0x00	
0xCE ~ 0xCF	Reserved	0x00	Reserved
0xD0	VBUS CONTROL	0x00	
0xD1	VBUS_TARGET_CONTROL_BYTE_0	0xC8	
0xD2	VBUS_TARGET_CONTROL_BYTE_1	0x00	
0xD3 ~ 0xDC	Reserved	0xC8	Reserved
0xDD	FW_VERSION_HIGH_BYTE	0x00	
0xDE	FW_VERSION_LOW_BYTE	0x00	
0xDF	HW_VERSION	0x08	

Vendor ID Low Byte Register (address = 0x00) [reset = 0x5B]

Vendor ID Low Byte Register

7	6	5	4	3	2	1	0
VENDOR_ID_L							
R							

LEGEND: R/W = Read/Write; R = Read only

Vendor ID Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDOR_ID_L	R	0x5B	Low byte of a 16-bit USB-IF defined Fitipower vendor ID of 0x2E5B.

Vendor ID High Byte Register (address = 0x01) [reset = 0x2E]

Vendor ID High Byte Register

7	6	5	4	3	2	1	0
VENDOR_ID_H							
R							

LEGEND: R/W = Read/Write; R = Read only

Vendor ID High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VENDOR_ID_H	R	0x2E	High byte of a 16-bit USB-IF defined Fitipower vendor ID of 0x2E5B.

Product ID Low Byte Register (address = 0x02) [reset =0x06]

Product ID Low Byte Register

7	6	5	4	3	2	1	0
PRODUCT_ID_L							
R							

LEGEND: R/W = Read/Write; R = Read only

Product ID Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODUCT_ID_L	R	0x06	Low byte of a FP6606 16-bit Product ID of 0x6606.

Product ID High Byte Register (address = 0x03) [reset =0x66]

Product ID High Byte Register

7	6	5	4	3	2	1	0
PRODUCT_ID_H							
R							

LEGEND: R/W = Read/Write; R = Read only

Product ID High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODUCT_ID_H	R	0x66	High byte of a FP6606 16-bit Product ID of 0x6606.

Device ID Low Byte Register (address = 0x04) [reset =0x00]

Device ID Low Byte Register

7	6	5	4	3	2	1	0
DEVICE_ID_L							
R							

LEGEND: R/W = Read/Write; R = Read only

Device ID Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_L	R	0x00	Low byte of a 16-bit Device ID.

Device ID High Byte Register (address = 0x05) [reset =0x00]

Device ID High Byte Register

7	6	5	4	3	2	1	0
DEVICE_ID_H							
R							

LEGEND: R/W = Read/Write; R = Read only

Device ID High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID_H	R	0x00	High byte of a 16-bit Device ID.

USB Type-C Revision Low Byte Register (address = 0x06) [reset =0x00]

USB Type-C Revision Low Byte Register

7	6	5	4	3	2	1	0
USBTYPEC_REV_L							
R							

LEGEND: R/W = Read/Write; R = Read only

USB Type-C Revision Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USBTYPEC_REV_L	R	0x00	Low byte of a 16-bit USB Type-C Revision. Revision 1.1. The FP6606 also supports USB Type-C Revision 1.2.

USB Type-C Revision High Byte Register (address = 0x07) [reset =0x00]

USB Type-C Revision High Byte Register

7	6	5	4	3	2	1	0
USBTYPEC_REV_H							
R							

LEGEND: R/W = Read/Write; R = Read only

USB Type-C Revision High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USBTYPEC_REV_H	R	0x00	High byte of a 16-bit USB Type-C Revision.

USB PD Revision Version Low Byte Register (address = 0x08) [reset =0x11]

USB PD Revision Version Low Byte Register

7	6	5	4	3	2	1	0
USBPD_REV_VER_L							
R							

LEGEND: R/W = Read/Write; R = Read only

USB PD Revision Version Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USBPD_REV_VER_L	R	0x11	Low byte of a 16-bit USB PD version. Version 1.1.

USB PD Revision Version High Byte Register (address = 0x09) [reset =0x30]

USB PD Revision Version High Byte Register

7	6	5	4	3	2	1	0
USBPD_REV_VER_H							
R							

LEGEND: R/W = Read/Write; R = Read only

USB PD Revision Version High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USBPD_REV_VER_H	R	0x30	High byte of a 16-bit USB PD Revision. Revision 3.0.

PD Interface Revision Low Byte Register (address = 0x0A) [reset =0x12]

PD Interface Revision Low Byte Register

7	6	5	4	3	2	1	0
PD_INTERFACE_REV_L							
R							

LEGEND: R/W = Read/Write; R = Read only

PD Interface Revision Low Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PD_INTERFACE_REV_L	R	0x12	Low byte of a 16-bit PD Interface (TCPC) Version. Version 1.2

PD Interface Revision High Byte Register (address = 0x0B) [reset =0x10]

PD Interface Revision High Byte Register

7	6	5	4	3	2	1	0
PD_INTERFACE_REV_H							
R							

LEGEND: R/W = Read/Write; R = Read only

PD Interface Revision High Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PD_INTERFACE_REV_H	R	0x10	High byte of a 16-bit PD Interface (TCPC) Revision. Revision 1.0

Alert High Byte Register (address = 0x10) [reset =0x02]

If the FP6606 finishes the initiation, the PWR_STATUS bit will be set to high for informing the TCPM. When the FP6606 is powered on or reset, the default value of this register will be set to 0x02 caused by the PWR_STATUS bit.
This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the FP6606 will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.

Alert High Byte Register

7	6	5	4	3	2	1	0
VBUS_ALARM_HI	TX_SOP_SUCCESS	TX_SOP_DISCARD	TX_SOP_FAIL	RX_HARD_RESET	RX_SOP_STATUS	PWR_STATUS	CC_STATUS
RCU	RCU	RCU	RCU	RCU	RCU	RCU	RCU

LEGEND: R/W = Read/Write; R = Read only

Alert High Byte Register Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_ALARM_HI	RCU	0	VBUS Voltage Alarm High 0b: Cleared 1b: A high-voltage alarm has occurred. Please refer to Reg.0x78 and Reg. 0x79 for setting high-voltage alarm level.
6	TX_SOP_SUCCESS	RCU	0	Transmit SOP* Message Successful 0b: Cleared 1b: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
5	TX_SOP_DISCARD	RCU	0	Transmit SOP* Message Discarded 0b: Cleared 1b: Reset or SOP* message transmission not sent due to incoming receive message. Transmit SOP* message buffer registers are empty.
4	TX_SOP_FAIL	RCU	0	Transmit SOP* Message Failed 0b: Cleared 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
3	RX_HARD_RESET	RCU	0	Received Hard Reset 0b: Cleared. 1b: Received Hard Reset message
2	RX_SOP_STATUS	RCU	0	Receive SOP* Message Status 0b: Cleared. 1b: Receive buffer register changed. RECEIVE_BYTE_COUNT (Reg.0x30) being set to 0 does not set this bit.
1	PWR_STATUS	RCU	1	Power Status 0b: Cleared. 1b: Power Status Changed
0	CC_STATUS	RCU	0	CC Status 0b: Cleared 1b: CC status changed

Alert High Byte Register (address = 0x11) [reset =0x02]

If the FP6606 is powered on or reset, the Reg.0x1F [7] will be set to high and all registers set to default. The Reg.0x11 [1] FAULT bit is therefore set to high for informing TCPM. Consequently, the default value of this register is 0x02.
This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the FP6606 will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.

Alert Byte 1 Register

7	6	5	4	3	2	1	0
VENDOR_DEFINED_ALERT	Reserved			VBUS_SINK_DIS	RX_BUF_OVR	FAULT	VBUS_ALARM_LO
RCU	R			RCU	RCU	RCU	RCU

LEGEND: R/W = Read/Write; R = Read only

Alert Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7	VENDOR_DEFINED_ALERT	RCU	0	Vendor Defined Alert: This bit can be cleared, regardless of the current status of the alert source. 0b: Cleared 1b: A vendor defined alert has been detected. Refer to the vendor interrupt register (Reg.0x90&91).
6:4	Reserved	R	0x0	Reserved
3	VBUS_SINK_DIS	RCU	0	VBUS Sink Disconnect Detected: This bit only be asserted when POWER_CONTROL.AUTO_DISCHARGE_DISCONNECT (Reg.0x1C[4]) is set 0b: Cleared 1b: A VBUS Sink Disconnect Threshold crossing has been detected
2	RX_BUF_OVR	RCU	0	Rx Buffer Overflow: Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.ReceiveSOP*MessageStatus. 0b: FP6606 Rx buffer is functioning properly. 1b: FP6606 Rx buffer has overflowed. Future GoodCRC will not be sent.
1	FAULT	RCU	1	Fault 0b: No Fault 1b: A Fault has occurred. Read the FAULT_STATUS register (Reg.0x1F).
0	VBUS_ALARM_LO	RCU	0	VBUS Voltage Alarm Low 0b: Cleared 1b: A low-voltage alarm has occurred. Please refer to Reg.0x76 and Reg. 0x77 for setting low-voltage alarm level.

Alert Mask Byte 0 Register (address = 0x12) [reset =0xFF]

This register controls whether or not a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Alert Mask Byte 0 Register

7	6	5	4	3	2	1	0
VBUS_ALARM_HI_MASK	TX_SOP_SUCCESS_MASK	TX_SOP_DISCARD_MASK	TX_SOP_FAIL_MASK	RX_HARD_RESET_MASK	RX_SOP_STATUS_MASK	PWR_STATUS_MASK	CC_STATUS_MASK
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Alert Mask Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_ALARM_HI_MASK	RW	1	VBUS Voltage Alarm High Mask 0b: Interrupt masked 1b: Interrupt unmasked
6	TX_SOP_SUCCESS_MASK	RW	1	Transmit SOP* Message successful Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
5	TX_SOP_DISCARD_MASK	RW	1	Transmit SOP* Message discarded Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
4	TX_SOP_FAIL_MASK	RW	1	Transmit SOP* Message failed Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
3	RX_HARD_RESET_MASK	RW	1	Received Hard Reset Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
2	RX_SOP_STATUS_MASK	RW	1	Receive SOP* Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	PWR_STATUS_MASK	RW	1	Power Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	CC_STATUS_MASK	RW	1	CC Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked

Alert Mask Byte 1 Register (address = 0x13) [reset =0x0F]

This register controls whether or not a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Alert Mask Byte 1 Register

7	6	5	4	3	2	1	0
VENDOR_DEFINED_ALERT_MASK	Reserved			VBUS_SINK_DIS_MASK	RX_BUF_OVR_MASK	FAULT_MASK	VBUS_ALARM_LO_MASK
RW	RW			RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Alert Mask Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7	VENDOR_DEFINED_ALERT_MASK	RW	0	Vendor Defined Alert Mask 0b: Interrupt masked 1b: Interrupt unmasked
6:4	Reserved	RW	0x0	Reserved
3	VBUS_SINK_DIS_MASK	RW	1	VBUS Sink Disconnect Detected Mask 0b: Interrupt masked 1b: Interrupt unmasked
2	RX_BUF_OVR_MASK	RW	1	Rx Buffer Overflow Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	FAULT_MASK	RW	1	Fault Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	VBUS_ALARM_LO_MASK	RW	1	VBUS Voltage Alarm Low Mask 0b: Interrupt masked 1b: Interrupt unmasked

Power Status Mask Register (address = 0x14) [reset =0xFF]

This register controls whether or not a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Power Status Mask Register

7	6	5	4	3	2	1	0
DEBUG_ACCESSORY_MASK	TCPC_INIT_STATUS_MASK	SRC_HIGH_VBUS_STATUS_MASK	SRC_VBUS_STATUS_MASK	VBUS_PRES_DET_STATUS_MASK	VBUS_PRES_INT_MASK	VCONN_PRES_INT_MASK	SINK_VBUS_STATUS_INT_MASK
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Power Status Mask Register Descriptions

Bit	Field	Type	Reset	Description
7	DEBUG_ACCESSORY_MASK	RW	1	Debug Accessory Connected Mask 0b: Interrupt masked 1b: Interrupt unmasked
6	TCPC_INIT_STATUS_MASK	RW	1	TCPC Initialization Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
5	SRC_HIGH_VBUS_STATUS_MASK	RW	1	Sourcing High Voltage Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
4	SRC_VBUS_STATUS_MASK	RW	1	Sourcing VBUS Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
3	VBUS_PRES_DET_STATUS_MASK	RW	1	VBUS Present Detection Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
2	VBUS_PRES_INT_MASK	RW	1	VBUS Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	VCONN_PRES_INT_MASK	RW	1	VCONN Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	SINK_VBUS_STATUS_INT_MASK	RW	1	Sinking VBUS Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked

Fault Status Mask Register (address = 0x15) [reset =0xFF]

This register controls whether or not a status change event in Alert register will cause the INT_N to be asserted low. When a specific event is masked, its corresponding status change event will not cause INT_N to be asserted low.

Fault Status Mask Register

7	6	5	4	3	2	1	0
ALLREG_RESET_TO_DEFAULT_MASK	FORCE_VBUS_MASK	AUTO_DISC_FAIL_MASK	FORCE_DISC_FAIL_MASK	VBUS_OCP_FAIL_STATUS_MASK	VBUS_OVP_FAIL_STATUS_MASK	VCONN_OCP_FAULT_STATUS_MASK	I2C_INT_ERR_STATUS_I_MASK
R	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Fault Status Mask Register Descriptions

Bit	Field	Type	Reset	Description
7	ALLREG_RESET_TO_DEFAULT_MASK	RW	1	All Registers Reset to Default Mask 0b: Interrupt masked 1b: Interrupt unmasked
6	FORCE_VBUS_MASK	RW	1	Force Off VBUS Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
5	AUTO_DISC_FAIL_MASK	RW	1	Auto Discharge Failed Mask 0b: Interrupt masked 1b: Interrupt unmasked
4	FORCE_DISC_FAIL_MASK	RW	1	Force Discharge Failed Mask 0b: Interrupt masked 1b: Interrupt unmasked
3	VBUS_OCP_FAIL_STATUS_MASK	RW	1	Internal or External OCP VBUS Over Current Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
2	VBUS_OVP_FAIL_STATUS_MASK	RW	1	Internal or External OVP VBUS Over Voltage Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
1	VCONN_OCP_FAULT_STATUS_MASK	RW	1	VCONN Over Current Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked
0	I2C_INT_ERR_STATUS_I_MASK	RW	1	I2C Interface Error Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked

TCPC Control Register (address = 0x19) [reset =0x00]

The TCPM writes to the TCPC_ CONTROL register to set the Plug Orientation and enable/disable clock stretching.

TCPC Control Register

7	6	5	4	3	2	1	0
Reserved		EN_WATCHDOG_TIMER	DEBUG_ACC_CTL	I2C_CLOCK_STRETCHING_CTL		BIST_TEST_MODE	PLUG_ORIENTATION
RW		RW	RW	R		RW	RW

LEGEND: R/W = Read/Write; R = Read only

TCPC Control Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	RW	000	Reserved
5	EN_WATCHDOG_TIMER	RW	0	Enable Watchdog Timer Required if DEVICE_CAPABILITIES_2.Watch Dog Timer (Reg.0x27 [0]) = 1b 0b: Watchdog Monitoring is disabled (default) 1b: Watchdog Monitoring is enabled
4	DEBUG_ACC_CTL	RW	0	Debug Accessory Control 0b: Controlled by FP6606 (power on default) 1b: Controlled by TCPM. The TCPM writes 1b to this register to take over control of asserting the DebugAccessoryConnected#.
3:2	I2C_CLOCK_STRETCHING_CTL	RW	00	FP6606 does not support clock stretching.
1	BIST_TEST_MODE	RW	0	Built in Self-Test Mode: Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the FP6606. The TCPM should clear this bit when a detach is detected. 0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but will not be passed to the TCPM via Alert.
0	PLUG_ORIENTATION	RW	0	Plug Orientation 0b: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.

Role Control Register (address = 0x1A) [reset =0x0A]

The TCPM writes to this register to configure the CC pull up (Rp) or pull down (Rd) resistors.

Role Control Register

7	6	5	4	3	2	1	0
Reserved	DRP	RP_VALUE		CC2		CC1	
R	RW	RW		RW		RW	

LEGEND: R/W = Read/Write; R = Read only

Role Control Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Reserved
6	DRP	RW	0	Dual-Role Power: The TCPC toggles CC1 & CC2 after receiving COMMAND.Look4Connection and until a connection is detected. Upon connection, the TCPC shall resolve to either an Rp or Rd and report the CC1/CC2 State in the CC_STATUS register. 0b: No DRP. Bits B3..0 determine Rp/Rd/Ra or open settings 1b: DRP
5:4	RP_VALUE	RW	00	Pull up resistor 00b: Rp default current 01b: Rp 1.5 A 10b: Rp 3 A 11b: Reserved
3:2	CC2	RW	10	Configuration Channel 1 00b: Ra 01b: Rp 10b: Rd 11b: Open (Disconnect or don't care)
1:0	CC1	RW	10	Configuration Channel 2 00b: Ra 01b: Rp 10b: Rd 11b: Open (Disconnect or don't care)

Fault Control Register (address = 0x1B) [reset =0x00]

The TCPM writes to FAULT_CONTROL to enable/disable FAULT circuitry.

Fault Control Register

7	6	5	4	3	2	1	0
Reserved			FORCE_OFF_VBUS	VBUS_DIS_FAULT_DETECT_TIMER	VBUS_OCP_FAULT	VBUS_OVP_FAULT	VCONN_OC_FAULT
RW			RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Fault Control Register Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	RW	0	Reserved
4	FORCE_OFF_VBUS	RW	0	The FP6606 does not support the function.
3	VBUS_DIS_FAULT_DETECT_TIMER	RW	0	VBUS Discharge Fault Detection Timer: This enables or disables the timers for both FAULT_STATUTS.AutoDischargeFailed (Reg.0x1F [5]) and FAULT_STATUS.ForceDischargeFailed (Reg.0x1F [4]). 0b: VBUS Discharge Fault Detection Timer enabled 1b: VBUS Discharge Fault Detection Timer disabled
2	VBUS_OCP_FAULT	RW	0	The FP6606 does not support the function.
1	VBUS_OVP_FAULT	RW	0	The FP6606 does not support the function in this field. Please refer to the Reg. 0xCC. When the VBUS is higher than the specified voltage, the Reg. 0xCD [1] will be written with a 1b and the GPIO 2 (fault pin) will be pulled high.
0	VCONN_OC_FAULT	RW	0	VCONN Over Current Fault: Required if DEVICE_CAPABILITIES_2.VCONNOvercurrentFaultCapable (Reg.0x26 [0]) = 1b. 0b: Fault detection circuit enabled 1b: Fault detection circuit disabled

Power Control Register (address = 0x1C) [reset =0x60]

Power Control Register

7	6	5	4	3	2	1	0
Reserved	VBUS_VOLTAGE_MONITOR	DISABLE_VOTAGE_ALARMS	AUTO_DISCHARGE_DISCONNECT	EN_BLEED_DISCHARGE	FORCE_DISCHARGE	VCONN_PWR_SUPPORTED	ENABLE_VCONN
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Power Control Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Reserved
6	VBUS_VOLTAGE_MONITOR	RW	1	VBUS Voltage Monitor: Controls only VBUS VOLTAGE Monitoring. VBUS_VOLTAGE will report all zeroes if disabled. Required if DEVICE_CAPABILITIES_1.VBUS Measurement and Alarm Capable (Reg.0x25 [2]) = 1b. 0b: VBUS_VOLTAGE Monitoring is enabled. 1b: VBUS_VOLTAGE Monitoring is disabled (default).
5	DISABLE_VOTAGE_ALARMS	RW	1	Disable Voltage Alarms: Controls VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. Required if DEVICE_CAPABILITIES_1.VBUS Measurement and Alarm Capable (Reg.0x25 [2]) = 1b. 0b: Voltage Alarms Power status reporting is enabled. 1b: Voltage Alarms Power status reporting is disabled (default).
4	AUTO_DISCHARGE_DISCONNECT	RW	0	Auto Discharge Disconnect Setting this bit in a Source TCPC triggers the following actions upon disconnection detection: 1. Disable sourcing power over VBUS 2. VBUS discharge Sourcing power over VBUS shall be disabled before or at same time as starting VBUS discharge. Setting this bit in a Sink TCPC triggers the following action upon disconnection detection: 1. VBUS discharge The FP6606 will automatically disable discharge once the voltage on VBUS is below vSafe0V (max) or VBUS_STOP_DISCHARGE_THRESHOLD (Reg.0x74 & 0x75). 0b: The FP6606 shall not automatically discharge VBUS based on VBUS voltage. (Default) 1b: The FP6606 will automatically discharge
3	EN_BLEED_DISCHARGE	RW	0	Enable Bleed Discharge: Bleed Discharge is a low current discharge to provide a minimum load current. FP6606 will apply 10 Ohms on VBUS for bleed discharge. Required if DEVICE_CAPABILITIES_1.BleedDischarge (Reg.0x25 [4]) = 1b 0b: Disable bleed discharge (default). 1b: Enable bleed discharge of VBUS
2	FORCE_DISCHARGE	RW	0	Force Discharge: When this field is set, the FP6606 will discharge VBUS to Vsafe0V or threshold programmed in the VBUS_STOP_DISCHARGE_THRESHOLD register (Reg.0x74 & 0x75). Once VBUS is discharged to desired level, the FP6606 will disable the Force Discharge. Required if DEVICE_CAPABILITIES_1.ForceDischarge (Reg.0x25 [3])= 1b 0b: Disable forced discharge (default). 1b: Enable forced discharge of VBUS.
1	Reserved	RW	0	Reserved
0	ENABLE_VCONN	RW	0	Enable VCONN 0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC indicated by PLUG_ORIENTATION in TCPC Control register (Reg0x19 [0]).

CC Status Register (address = 0x1D) [reset =0x10]

The CC status register indicate the state of the FP6606. It is set by the FP6606 and read by the TCPM. The CC status register is not latched and is continually updated unless powered off.

CC Status Register

7	6	5	4	3	2	1	0
Reserved		LOOKING4CONNECTION	CONNECT_RESULT	CC2_STATE		CC1_STATE	
R		RU	RU	RU		RU	

LEGEND: R/W = Read/Write; R = Read only

CC Status Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	0	Reserved
5	LOOKING4CONNECTION	RU	0	Looking for Connection 0b: FP6606 is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found. 1b: FP6606 is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition)
4	CONNECT_RESULT	RU	1	Connect Result 0b: the FP6606 is presenting Rp 1b: the FP6606 is presenting Rd

3:2	CC2_STATE	RU	00	If (ROLE_CONTROL.CC2=Rp) or (CONNECT_RESULT=0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: reserved
				
				If (ROLE_CONTROL.CC2=Rd) or (CONNECT_RESULT=1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
				
				If ROLE_CONTROL.CC2=Ra, this field is set to 00b
				If ROLE_CONTROL.CC2=Open, this field is set to 00b
				
				This field always returns 00b if (Looking4Connection=1) or (POWER_CONTROL.ENABLE_VCONN=1 and TCPC_CONTROL.PLUG_ORIENTATION =0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

1:0	CC1_STATE	RU	00	If (ROLE_CONTROL.CC1 = Rp) or (CONNECT_RESULT=0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: reserved
				
				If (ROLE_CONTROL.CC1 = Rd) or (CONNECT_RESULT=1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp- 1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp- 3.0A
				
				If ROLE_CONTROL.CC1=Ra, this field is set to 00b
				If ROLE_CONTROL.CC1=Open, this field is set to 00b
				
				This field always returns 00b if (Looking4Connection=1) or (POWER_CONTROL.ENABLE_VCONN=1 and TCPC_CONTROL.PLUG_ORIENTATION =1). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

Power Status Register (address = 0x1E) [reset =0x00]

The power status register indicate the state of the FP6606. It is set by the FP6606 and read by the TCPM. The power status register is not latched and is continually updated unless powered off.

Power Status Register

7	6	5	4	3	2	1	0
DEBUG_ACC_CONNECTED	TCPC_INIT_STATUS	SOURCING_HIGH_VOLTAGE	SOURCING_VBUS	VBUS_PRES_DETECT_ENABLED	VBUS_PRESENT	VCONN_PRESENT	SINKING_VBUS
RU	RU	RU	RU	RU	RU	RU	RU

LEGEND: R/W = Read/Write; R = Read only

Power Status Register Descriptions

Bit	Field	Type	Reset	Description
7	DEBUG_ACC_CONNECTED	RU	0	Debug Accessory Connected: Reflects the state of the DebugAccessoryConnected# output if supported. 0b: No Debug Accessory connected (default) 1b: Debug Accessory connected
6	TCPC_INIT_STATUS	RU	0	TCPC Initialization Status 0b: The FP6606 has completed initialization and all registers are valid. 1b: The FP6606 is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh.
5	SOURCING_HIGH_VOLTAGE	RU	0	FP6606 does not support the function in this field. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2.
4	SOURCING_VBUS	RU	0	FP6606 does not support the function in this field. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2.
3	VBUS_PRES_DETECT_ENABLED	RU	0	VBUS Present Detection Enabled: Indicates if the FP6606 is monitoring for VBUS Present or if the circuit has been powered off. 0b: VBUS Present Detection Disabled (Default) 1b: VBUS Present Detection Enabled
2	VBUS_PRESENT	RU	0	VBUS present: The FP6606 shall report VBUS present when FP6606 detects VBUS rises above 4 V. The FP6606 shall report VBUS is not present when FP6606 detects VBUS falls below 3.5 V. The FP6606 may report VBUS is not present if VBUS is between 3.5 V and 4 V. 0b: VBUS Disconnected 1b: VBUS Connected
1	VCONN_PRESENT	RU	0	VCONN present: If POWER_CONTROL.EnableVCONN (Reg.0x1C [0]) is disabled VCONN Present should be set to 0b. 0b: VCONN is not present 1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4 V
0	SINKING_VBUS	RU	0	FP6606 does not support the function in this field. Please refer to the Reg.0x85 [1] NMOS_SNK_ON. It is used to control sinking power path.

Fault Status Register (address = 0x1F) [reset =0x80]

The fault status register indicate the state of the FP6606. It is set by the FP6606 and read by the TCPM. The fault status register is latched unless powered off.
The FP6606 indicates a fault status change has occurred by presenting a logical 1 in the corresponding bit position in this register, presenting a logical 1 to the ALERT.Fault bit (Reg.0x11 [1]), and asserting the INT_N pin if the corresponding fault bit in FAULT_STATUS_MASK (Reg.0x15) is 1 and ALERT_MASK.Fault (Reg.0x13 [1]) is 1. The TCPM clears the FAULT bit by writing a logical 1 to the respective FAULT bit position and then writing a logical 1 to the ALERT.Fault bit (Reg.0x11 [1]) after all bits in FAULT_STATUS (Reg.0x1F) have been cleared. The TCPM writing a logical 0 to any FAULT bit has no effect and therefore does not cause those FAULT bits to be set or cleared.

Fault Status Register

7	6	5	4	3	2	1	0
ALLREG_RESET_TO_DEFAULT	FORCE_OFF_VBUS_STATUS	AUTO_DIS_FAIL_STATUS	FORCE_DIS_FAIL_STATUS	VBUS_OCP_FAULT_STATUS	VBUS_OVP_FAULT_STATUS	VCONN_OCP_FAULT_STATUS	I2C_INT_ERROR_STATUS
R	RCU	RCU	RCU	RCU	RCU	RCU	RCU

LEGEND: R/W = Read/Write; R = Read only

Fault Status Register Descriptions

Bit	Field	Type	Reset	Description
7	ALLREG_RESET_TO_DEFAULT	RCU	1	All Registers Reset to Default: This bit is asserted when the FP6606 resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs. 0b: Cleared 1b: All registers had been reset to default value
6	FORCE_OFF_VBUS_STATUS	RCU	0	The FP6606 does not support this function.
5	AUTO_DIS_FAIL_STATUS	RCU	0	Auto Discharge Failed: If POWER_CONTROL.AutoDischargeDisconnect (Reg.0x1C [4]) is set, the FP6606 will report discharge fails if VBUS is not below vSafe0V within tSafe0V. 0b: No discharge failure 1b: Discharge commanded by the TCPM failed
4	FORCE_DIS_FAIL_STATUS	RCU	0	Force Discharge Failed: If POWER_CONTROL.ForceDischarge (Reg.0x1C [2]) is set, the FP6606 will report a discharge fails if VBUS is not below vSafe0V within tSafe0V. 0b: No discharge failure 1b: Discharge commanded by the TCPM failed
3	VBUS_OCP_FAULT_STATUS	RCU	0	The FP6606 does not support this function.
2	VBUS_OVP_FAULT_STATUS	RCU	0	The FP6606 does not support this function.
1	VCONN_OCP_FAULT_STATUS	RCU	0	VCONN Over Current Fault: Required if DEVICE_CAPABILITIES_2.VCONNOvercurrentFaultCapable (Reg.0x26 [0])= 1b 0b: No Fault detected 1b: Over current VCONN fault latched
0	I2C_INT_ERROR_STATUS	RCU	0	I2C Interface Error: A TRANSMIT has been sent with an empty TRANSMIT_BUFFER. May be asserted if a non-zero value has been written to a reserved bit in a register. 0b: No Error 1b: I2C error has occurred

Command Register (address = 0x23) [reset =0x00]

The Command is issued by the TCPM. The Command is cleared by the FP6606 after being acted upon.

Command Register

7	6	5	4	3	2	1	0
COMMAND							
RWU							

LEGEND: R/W = Read/Write; R = Read only

Command Register Descriptions

Bit	Field	Type	Reset	Description
7	COMMAND	RWU	0x00	1001 1001b: **Look4Connection** Start DRP Toggling if ROLE_CONTROL.DRP (Reg.0x1A [6]) =1b. If ROLE_CONTROL.CC1/CC2 (Reg.0x1A [1:0]/[3:2]) = 01b start with Rp, if ROLE_CONTROL.CC1/CC2 (Reg.0x1A [1:0]/[3:2]) =10b start with Rd. If ROLE_CONTROL.CC1/CC2 (Reg.0x1A [1:0]/[3:2]) are not both 01b or 10b, then do not start toggling. The TCPM shall issue COMMAND.Look4Connection to enable the FP6606 to restart Connection Detection in cases where the ROLE_CONTROL contents will not change. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case a Source Only or DRP should go back to its Unattached.Src state. This would result in ROLE_CONTROL staying the same. Besides command 0x99, The FP6606 will accept others command but will do nothing with it.

Device Capabilities 1 Byte 0 Register (address = 0x24) [reset =0xD8]

This register is in the nonvolatile memory of the FP6606. This register describes features supported by the FP6606.

Device Capabilities 1 Byte 0 Register

7	6	5	4	3	2	1	0
ROLES_SUPPORTED			SOP_DBG_SUPPORT	SRC_VCONN	SNK_VBUS	SRC_HIGH_VBUS	SRC_VBUS
R			R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only

Device Capabilities 1 Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:5	ROLES_SUPPORTED	R	110	Roles Supported. 000b: USB Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support 100b: DRP only 101b: Source, Sink, DRP, Adapter/Cable all supported 110b: Source, Sink, DRP 111b: Not valid
4	SOP_DBG_SUPPORT	R	1	SOP'_DBG/SOP"_DBG Support Configured in RECEIVE_DETECT (Reg.0x2F) and TRANSMIT (Reg.0x50) 0b: All SOP* except SOP'_DBG/SOP"_DBG 1b: All SOP* messages are supported
3	SRC_VCONN	R	1	Source VCONN Support for POWER_CONTROL.EnableVCONN (Reg.0x1C [0]) and POWER_STATUS.VCONNPresent (Reg.0x1E [1]) implemented. 0b: FP6606 is not capable of switching VCONN 1b: FP6606 is capable of switching VCONN
2	SNK_VBUS	R	0	This field does not affect FP6606. Please refer to the Reg.0x85 [1] NMOS_SNK_ON. It is used to control sinking power path.
1	SRC_ HIGH_VBUS	R	0	This field does not affect FP6606. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2.
0	SRC_VBUS	R	0	This field does not affect FP6606. Please refer to vendor defined register. The VBUS control function is assigned to the Reg.0xD0~0xD2.

Device Capabilities 1 Byte 1 Register (address = 0x25) [reset =0x1E]

This register is in the nonvolatile memory of the FP6606. This register describes features supported by the FP6606.

Device Capabilities 1 Byte 1 Register

7	6	5	4	3	2	1	0
Reserved	VBUS_OCP_REPORT	VBUS_OVP_REPORT	BLEED_DISCHARGE	FORCE_DISCHARGE	VBUS_MEASURE_ALARM_CAPABLE	SRC_RESISTOR_SUPPORT	
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only

Device Capabilities 1 Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6	VBUS_OCP_REPORT	R	0	VBUS OCP Reporting Support for both FAULT_STATUS.InternalorExternalOCP (Reg.0x1F [3]) and FAULT_CONTROL. InternalorExternalOCP (Reg.0x1B [2]) implemented. 0b: VBUS OCP is not reported by the FP6606 1b: VBUS OCP is reported by the FP6606
5	VBUS_OVP_REPORT	R	0	This field does not affect FP6606. Please refer to the Reg. 0xCC. When the VBUS is higher than the specified voltage, the Reg. 0xCD [1] will be written with a 1b and the GPIO 2 (fault pin) will be pull high.
4	BLEED_DISCHARGE	R	1	Bleed Discharge Support for POWER_CONTROL.EnableBleedDischarge (Reg.0x1C [3]) implemented. 0b: No Bleed Discharge implemented in the FP6606 1b: Bleed Discharge is implemented in the FP6606
3	FORCE_DISCHARGE	R	1	Force Discharge Support for POWER_CONTROL.ForceDischarge (Reg.0x1C [2]), FAULT_STATUS.ForceDischargeFailed (Reg.0x1F [4]), and VBUS_STOP_DISCHARGE_THRESHOLD (Reg.0x74&0x75) implemented. Support for VBUS_STOP_DISCHARGE_THRESHOLD (Reg.0x74&0x75) register implemented when act as Source. 0b: No Force Discharge implemented in the FP6606 1b: Force Discharge is implemented in the FP6606
2	VBUS_MEASURE_ALARM_CAPABLE	R	1	VBUS Measurement and Alarm Capable Support for VBUS_VOLTAGE, VBUS_VOLTAGE_ALARM_HI_CFG (Reg.0x76&0x77), VBUS_VOLTAGE_ALARM_LO_CFG (Reg.0x78&0x79) implemented. 0b: No VBUS voltage measurement or VBUS Alarms 1b: VBUS voltage measurement and VBUS Alarms
1:0	SRC_RESISTOR_SUPPORT	R	10	Source Resistor Supported Rp values which may be configured by the TCPM via the ROLE_CONTROL register (Reg.0x1A). 00b: Rp default only 01b: Rp 1.5 A and default 10b: Rp 3 A, 1.5 A, and default 11b: Reserved

Device Capabilities 2 Byte 0 Register (address = 0x26) [reset =0xC1]

This register is in the nonvolatile memory of the FP6606. This register describes features supported by the FP6606.

Device Capabilities 2 Byte 0 Register

7	6	5	4	3	2	1	0
SINK_DISCON NECT_DETECT	STOP_DISCHA RGE_THRESHOLD	VBUS_VOLTAGE_ALARM_LSB		VCONN_PWR_SUPPORT			VCONN_OC_FAULT_SUPPORT
R	R	R		R			R

LEGEND: R/W = Read/Write; R = Read only

Device Capabilities 2 Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	SINK_DISCON NECT_DETECT	R	1	Sink Disconnect Detection 0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (Use POWER_STATUS.VbusPresent (Reg.0x1E [2])=0b to indicate a Sink disconnect) 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented
6	STOP_DISCHA RGE_THRESHOLD	R	1	Stop Discharge Threshold 0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented
5:4	VBUS_VOLTAGE_ALARM_LSB	R	00	VBUS Voltage Alarm LSB 00b: FP6606 has 25mV LSB for its voltage alarm and uses all10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG 01b: FP6606 has 50mV LSB for its voltage alarm and uses only 9 bits VBUS_VOLTAGE_ALARM_HI_CFG [0] and VBUS_VOLTAGE_ALARM_LO_CFG [0] are ignored by FP6606 10b: FP6606 has 100mV LSB for its voltage alarm and uses only 8 bits VBUS_VOLTAGE_ALARM_HI_CFG [1:0] and VBUS_VOLTAGE_ALARM_LO_CFG [1:0] are ignored by FP6606 11b: Reserved Support for VBUS_VOLTAGE_ALARM_LO_CFG and VBUS_VOLTAGE_ALARM_HI implemented
3:1	VCONN_PWR_SUPPORT	R	000	VCONN Power Supported 000b: 100m W
0	VCONN_OC_FAULT_SUPPORT	R	1	VCONN Overcurrent Fault Capable Support for FAULT_STATUS.VCONNOverCurrentFault (Reg.0x1F [1]) and FAULT_CONTROL.VCONNOverCurrentFault (Reg.0x1B [0]) implemented 0b: FP6606 is not capable of detecting a VCONN fault 1b: FP6606 is capable of detecting a VCONN fault

Device Capabilities 2 Byte 1 Register (address = 0x27) [reset =0x01]

This register is in the nonvolatile memory of the FP6606. This register describes features supported by the FP6606.

Device Capabilities 2 Byte 1 Register

7	6	5	4	3	2	1	0
Reserved							WATCHDOG_TIMER
R							R

LEGEND: R/W = Read/Write; R = Read only

Device Capabilities 2 Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:1	Reserved	R	0x00	Reserved
0	WATCHDOG_TIMER	R	1	Watchdog Timer 0b: TCPC_CONTROL.Enable Watchdog Timer (Reg.0x19 [5]) not implemented 1b: TCPC_CONTROL.Enable Watchdog Timer (Reg.0x19 [5]) implemented

Standard Input Capabilities Register (address = 0x28) [reset =0x00]

This register is in the nonvolatile memory of the FP6606. This register describes the optional normative Standard Inputs and their capability.

Standard Input Capabilities Register

7	6	5	4	3	2	1	0
Reserved					EXT_VBUS_OVF_SUPPORT	EXT_VBUS_OCF_SUPPORT	EXT_FORCE_OFF_VBUS_SUPPORT
R					R	R	R

LEGEND: R/W = Read/Write; R = Read only

Standard Input Capabilities Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0	Reserved
2	EXT_VBUS_OVF_SUPPORT	R	0	VBUS External Over Voltage Fault 0b: Not present in FP6606 1b: Present in FP6606
1	EXT_VBUS_OCF_SUPPORT	R	0	VBUS External Over Current Fault 0b: Not present in FP6606 1b: Present in FP6606
0	EXT_FORCE_OFF_VBUS_SUPPORT	R	0	Force Off VBUS (Source or Sink) 0b: Not present in FP6606 1b: Present in FP6606

Standard Output Capabilities Register (address = 0x29) [reset =0x00]

This register is in the nonvolatile memory of the FP6606. This register describes the optional normative Standard Inputs and their capability.

Standard Output Capabilities Register

7	6	5	4	3	2	1	0
Reserved	DEBUG_ACC_INDICATOR	VBUS_PRESENT_MONITOR	AUDIO_ADAP_ACC_INDICATOR	ACTIVE_CABLE_ INDICATOR	MUX_CONFIG_CONTROL	CONNECT_PRESENT	CONNECTOR_ORIENT
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only

Standard Output Capabilities Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved
6	DEBUG_ACC_INDICATOR	R	0	Debug Accessory Indicator 0b: Not present in FP6606 1b: Present in FP6606
5	VBUS_PRESENT_MONITOR	R	0	VBUS Present Monitor 0b: Not present in FP6606 1b: Present in FP6606
4	AUDIO_ADAP_ACC_INDICATOR	R	0	Audio Adapter Accessory Indicator 0b: Not present in FP6606 1b: Present in FP6606
3	ACTIVE_CABLE_ INDICATOR	R	0	Active Cable Indicator 0b: Not present in FP6606 1b: Present in FP6606
2	MUX_CONFIG_CONTROL	R	0	MUX Configuration Control 0b: Not present in FP6606 1b: Present in FP6606
1	CONNECT_PRESENT	R	0	Connection Present 0b: Not present in FP6606 1b: Present in FP6606
0	CONNECTOR_ORIENT	R	0	Connector Orientation 0b: Not present in FP6606 1b: Present in FP6606

Message Header Info Register (address = 0x2E) [reset =0x02]

The FP6606 shall set this register at power on. The TCPM may overwrite this register after FP6606 initialization is complete.
On attach and after implementing the tCCDebounce, the TCPM shall update the MESSAGE_HEADER_INFO Register first before writing to the RECEIVE_DETECT (Reg.0x2F) register.
The FP6606 reads from this register to generate the Message header for the GoodCRC.

Message Header Info Register

7	6	5	4	3	2	1	0
Reserved			CABLE_PLUG	DATA_ROLE	USBPD_SPECREV		POWER_ROLE
RW			RW	RW	RW		RW

LEGEND: R/W = Read/Write; R = Read only

Message Header Info Register Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	000	Shall be set to zero by sender and ignored by receiver
4	CABLE_PLUG	RW	0	Cable Plug 0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug
3	DATA_ROLE	RW	0	Data Role 0b: UFP 1b: DFP
2:1	USBPD_SPECREV	RW	01	USB PD Specification Revision 00b: Revision 1.0 01b: Revision 2.0 10b: Revision 3.0 11b: Reserved
0	POWER_ROLE	RW	0	Power Role 0b: Sink 1b: Source

Receiver Detect Register (address = 0x2F) [reset =0x00]

The TCPM notifies the FP6606 of the message type and/or signaling types to be detected. The TCPM should not set any bits in this register until it is able to respond. The FP6606 responds to the enabled message type with a GoodCRC if it is a SOP* message, except in the case of a GoodCRC message.
On Hard Reset reception, the FP6606 shall set the RECEIVE_DETECT bits to zero to disable automatic transmission of GoodCRC. On detection of a Disconnect, the TCPC shall set the RECEIVE_DETECT bits all to zero to disable automatic transmission of GoodCRC. The FP6606 shall set the RECEIVE_DETECT bits to zero to disable automatic transmission of GoodCRC when RECEIVE_DETECT.CableReset is set and a Cable Reset is received.

Receiver Detect Register

7	6	5	4	3	2	1	0
Reserved	EN_CABLE_RESET	EN_HARD_RESET	EN_SOP_DBGPP	EN_SOP_DBGP	EN_SOPPP_MESSAGE	EN_SOPP_MESSAGE	EN_SOP_MESSAGE
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Receiver Detect Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Shall be set to zero by sender and ignored by receiver
6	EN_CABLE_RESET	RW	0	Enable Cable Reset 0b: FP6606 does not detect Cable Reset signaling (default) 1b: FP6606 detects Cable Reset signaling
5	EN_HARD_RESET	RW	0	Enable Hard Reset 0b: FP6606 does not detect Hard Reset signaling (default) 1b: FP6606 detects Hard Reset signaling
4	EN_SOP_DBGPP	RW	0	Enable SOP_DBG'' Message 0b: FP6606 does not detect SOP_DBG'' message (default) 1b: FP6606 detects SOP_DBG'' message
3	EN_SOP_DBGP	RW	0	Enable SOP_DBG' Message 0b: FP6606 does not detect SOP_DBG' message (default) 1b: FP6606 detects SOP_DBG' message
2	EN_SOPPP_MESSAGE	RW	0	Enable SOP'' Message 0b: FP6606 does not detect SOP'' message (default) 1b: FP6606 detects SOP'' message
1	EN_SOPP_MESSAGE	RW	0	Enable SOP' Message 0b: FP6606 does not detect SOP' message (default) 1b: FP6606 detects SOP' message
0	EN_SOP_MESSAGE	RW	0	Enable SOP Message 0b: FP6606 does not detect SOP message (default) 1b: FP6606 detects SOP message

Receive Byte Count Register (address = 0x30) [reset =0x00]

The TCPM reads the RECEIVE_BYTE_COUNT to determine the number of bytes in the RX_BUFFER_DATA_OBJECT (Reg.0x34~0x4F) and the RX_BUF_FRAME_TYPE (Reg.0x31) to determine the type of message.
The TCPM then reads the information in the RX_BUF_HEADER (Reg.0x32~33) and the RX_BUFFER_DATA_OBJECT. The FP6606 shall set the RECEIVE_BYTE_COUNT to 0 after the interrupt has been cleared.
Upon detection of a Disconnect, the FP6606 shall set the RECEIVE_BYTE_COUNT to zero.

Receive Byte Count Register

7	6	5	4	3	2	1	0
RECEIVE_BYTE_COUNT							
RU							

LEGEND: R/W = Read/Write; R = Read only

Receive Byte Count Register Descriptions

Bit	Field	Type	Reset	Description
7:0	RECEIVE_BYTE_COUNT	RU	0x00	Receive Byte Count Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register. This is the number of bytes in the RX_BUFFER_DATA_OBJECTS plus three (for the RX_BUF_FRAME_TYPE (Reg.0x31) and RX_BUF_HEADER (Reg.0x32~0x33)).

Receive Buffer Frame Type Register (address = 0x31) [reset =0x00]

Receive Buffer Frame Type Register

7	6	5	4	3	2	1	0
Reserved					RX_SOP_MESSAGE		
R					RU		

LEGEND: R/W = Read/Write; R = Read only

Receive Buffer Frame Type Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0x00	Shall be set to zero by sender and ignored by receiver
2:0	RX_SOP_MESSAGE	RU	0x0	Received SOP* Message 000b: Received SOP 001b: Received SOP' 010b: Received SOP'' 011b: Received SOP_DBG' 100b: Received SOP_DBG'' 110b: Received Cable Reset All others are reserved

Receive Buffer Header Byte 0 Register (address = 0x32) [reset =0x00]

Receive Buffer Header Byte 0 Register

7	6	5	4	3	2	1	0
RX_BUF_HDR_BYTE_0							
RU							

LEGEND: R/W = Read/Write; R = Read only

Receive Buffer Header Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	RX_BUF_HDR_BYTE_0	RU	0x00	Receive Buffer Header Byte 0 Byte 0 (bits 7:0) of USB PD message header.

Receive Buffer Header Byte 1 Register (address = 0x33) [reset =0x00]

Receive Buffer Header Byte 1 Register

7	6	5	4	3	2	1	0
RX_BUF_HDR_BYTE_1							
RU							

LEGEND: R/W = Read/Write; R = Read only

Receive Buffer Header Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	RX_BUF_HDR_BYTE_1	RU	0x00	Receive Buffer Header Byte 1 Byte 1 (bits 15:8) of USB PD message header.

Receive Buffer Data Object 1 Through 7 Register (address = 0x34 through 0x4F) [reset = 0x00]

Receive Buffer Data Object 1 Through 7 Register

7	6	5	4	3	2	1	0
RX_BUFF_OBJn_BYTE_m							
RU							

LEGEND: R/W = Read/Write; R = Read only

Receive Buffer Data Object 1 Through 7 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	RX_BUFF_OBJn_BYTE_m	RU	0x00	Receive Buffer Data Object n Byte m Ex: RX_BUFF_OBJ1_BYTE_0 = Byte 0 (bits 7..0) of 1st data object.

Transmit Register (address = 0x50) [reset = 0x00]

The TCPM writes to this register to transmit a SOP* message where the SOP* message payload is in 51h..6Fh registers. The entire register shall be written at once and then sent. The TCPC shall clear the TRANSMIT register (Reg.0x50) and TRANSMIT_BYTE_COUNT (Reg.0x51) after executing the transmission regardless of success or failure.

Transmit Register

7	6	5	4	3	2	1	0
Reserved		RETRY_COUNTER		Reserved	TX_SOP_MESSAGE		
RW		RWU		RW	RWU		

LEGEND: R/W = Read/Write; R = Read only

Transmit Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	RW	00	Shall be set to zero by sender and ignored by receiver
5:4	RETRY_COUNTER	RW	00	Retry Counter 00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
3	Reserved	RW	0	Shall be set to zero by sender, shall be ignored by receiver
2:0	TX_SOP_MESSAGE	RW	000	Transmit SOP* Message 000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP" 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2

Transmit Byte Count Register (address = 0x51) [reset = 0x00]

The TRANSMIT_BUFFER holds the TRANSMIT_BYTE_COUNT (Reg.0x51), the TX_BUF_HEADER (Reg.0x52~53), and the TX_BUFFER_DATA_OBJECTS (Reg.0x54~0x6F) (SOP* payload).

Transmit Byte Count Register

7	6	5	4	3	2	1	0
TX_BYTE_COUNT							
RWU							

LEGEND: R/W = Read/Write; R = Read only

Transmit Byte Count Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BYTE_COUNT	RWU	0x00	Transmit Byte Count The number of bytes the TCPM will write. This is the number of bytes in the TX_BUFFER_DATA_OBJECTS (Reg.0x54~6F) plus two (for the TX_BUF_HEADER (Reg.0x52~53)).

Transmit Buffer Header Byte 0 Register (address = 0x52) [reset = 0x00]

Transmit Buffer Header Byte 0 Register

7	6	5	4	3	2	1	0
TX_BUF_HDR_BYTE_0							
RW							

LEGEND: R/W = Read/Write; R = Read only

Transmit Buffer Header Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BUF_HDR_BYTE_0	RW	0x00	Transmit Buffer Header Byte 0 Byte 0 (bits 7:0) of USB PD message header.

Transmit Buffer Header Byte 1 Register (address = 0x53) [reset = 0x00]

Transmit Buffer Header Byte 1 Register

7	6	5	4	3	2	1	0
TX_BUF_HDR_BYTE_1							
RW							

LEGEND: R/W = Read/Write; R = Read only

Transmit Buffer Header Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BUF_HDR_BYTE_1	RW	0x00	Transmit Buffer Header Byte 1 Byte 1 (bits 15:8) of USB PD message header.

Transmit Buffer Data Object 1 Through 7 Register (address = 0x54 through 0x6F) [reset = 0x00]

Transmit Buffer Data Object 1 Through 7 Register

7	6	5	4	3	2	1	0
TX_BUFF_OBJn_BYTE_m							
R							

LEGEND: R/W = Read/Write; R = Read only

Transmit Buffer Data Object 1 Through 7 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	TX_BUFF_OBJn_BYTE_m	R	0	Transmit Buffer Object n Byte m Ex: TX_BUFF_OBJ1_BYTE_0 = Byte 0 (bits 7..0) of 1st data object.

VBUS Voltage Byte 0 Register (address = 0x70) [reset = 0x00]

The TCPM may read this register to determine the VBUS voltage measured on the Source or Sink at the USB Type-C Connector. The FP6606 shall maintain synchronization between the upper and lower 8 bits of the register.

VBUS Voltage Byte 0 Register

7	6	5	4	3	2	1	0
VBUS_MEASUREMENT[7:0]							
RU							

LEGEND: R/W = Read/Write; R = Read only

VBUS Voltage Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	VBUS_MEASUREMENT[7:0]	RU	0x00	VBUS Voltage Measurement [7:0] VBUS_MEASUREMENT[9:0] = VBUS_MEASUREMENT[9:8] + VBUS_MEASUREMENT[7:0]. The LSB is 25mV.

VBUS Voltage Byte 1 Register (address = 0x71) [reset = 0x00]

VBUS Voltage Byte 1 Register

7	6	5	4	3	2	1	0
Reserved						VBUS_MEASUREMENT[9:8]	
R						RU	

LEGEND: R/W = Read/Write; R = Read only

VBUS Voltage Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	0	Reserved
1:0	VBUS_MEASUREMENT[9:8]	RU	0	VBUS Voltage Measurement[9:8] VBUS_MEASUREMENT[9:0] = VBUS_MEASUREMENT[9:8] + VBUS_MEASUREMENT[7:0]. The LSB is 25mV.

VBUS Sink Disconnect Threshold Byte 0 Register (address = 0x72) [reset = 0x00]

This register is required by FP6606 which act as a Sink and are capable of receiving voltages greater than vSafe5V. Implementation of this register shall be defined in DEVICE_CAPABILITIES_2.SinkDisconnectDetection (Reg.0x26 [7]). This register has no action for a Source. The TCPM writes to this register to set the threshold at which a Sink will start the Auto Discharge if it is in the Attached.SNK state.

VBUS Sink Disconnect Threshold Byte 0 Register

7	6	5	4	3	2	1	0
VBUS_SNK_DISC_THRESHOLD[7:0]							
RW							

LEGEND: R/W = Read/Write; R = Read only

VBUS Sink Disconnect Threshold Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	VBUS_SNK_DISC_THRESHOLD[7:0]	RW	0x00	VBUS Sink Disconnect Threshold[7:0] 10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy. A value of bit 9..0 = 0x00 disables this threshold.

VBUS Sink Disconnect Threshold Byte 1 Register (address = 0x73) [reset = 0x00]

VBUS Sink Disconnect Threshold Byte 1 Register

7	6	5	4	3	2	1	0
Reserved						VBUS_SNK_DISC_THRESHOLD[9:8]	
R						RW	

LEGEND: R/W = Read/Write; R = Read only

VBUS Sink Disconnect Threshold Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	0x00	Reserved
1:0	VBUS_SNK_DISC_THRESHOLD[9:8]	RW	00	VBUS Sink Disconnect Threshold[9:8] 10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy. A value of bit 9..0 = 0x00 disables this threshold.

VBUS Stop Discharge Threshold Byte 0 Register (address = 0x74) [reset = 0x00]

This register is required by FP6606 which act as a Source and support POWER_CONTROL.ForceDischarge (Reg.0x1C [2]). The TCPM writes to this register to set the threshold at which a Source shall stop the forced discharge when POWER_CONTROL.ForceDischarge (Reg.0x1C [2]) = 1b. TCPC acting as a Source shall always discharge to vSafe0V upon disconnect, Hard Reset, or Power Role Swap.

VBUS Stop Discharge Threshold Byte 0 Register

7	6	5	4	3	2	1	0
VBUS_STOP_DISCHARGE_THRESHOLD[7:0]							
RW							

LEGEND: R/W = Read/Write; R = Read only

VBUS Stop Discharge Threshold Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	VBUS_STOP_DISCHARGE_THRESHOLD[7:0]	RW	0x00	VBUS Stop Discharge Threshold[7:0] 10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy.

VBUS Stop Discharge Threshold Byte 1 Register (address = 0x75) [reset = 0x00]

VBUS Stop Discharge Threshold Byte 1 Register

7	6	5	4	3	2	1	0
Reserved						VBUS_STOP_DISCHARGE_THRESHOLD[9:8]	
R						RW	

LEGEND: R/W = Read/Write; R = Read only

VBUS Stop Discharge Threshold Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	0x00	Reserved
1:0	VBUS_STOP_DISCHARGE_THRESHOLD[9:8]	RW	00	VBUS Stop Discharge Threshold[9:8] 10-bit for voltage threshold with 25 mV LSB. (Default vSafe5V) ±5% accuracy.

VBUS Voltage Alarm High Configure Byte 0 Register (address = 0x76) [reset = 0x00]

The TCPM writes to this registers to set the high voltage alarm level. The FP6606 sets ALERT. VBUS Voltage Alarm High (Reg.0x10 [7]) to 1 when VBUS exceeds the over voltage level. These registers are required if it is reported as supported in the one of the DEVICE_CAPABILITES registers (Reg.0x25 [2]).

VBUS Voltage Alarm High Configure Byte 0 Register

7	6	5	4	3	2	1	0
VBUS_ALARM_HIGH_THRESHOLD[7:0]							
RW							

LEGEND: R/W = Read/Write; R = Read only

VBUS Voltage Alarm High Configure Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	VBUS_ALARM_HIGH_THRESHOLD[7:0]	RW	0x00	VBUS Alarm High Threshold[7:0] 10-bit for voltage threshold with 25 mV LSB. ±5% accuracy.

VBUS Voltage Alarm High Configure Byte 1 Register (address = 0x77) [reset = 0x00]

VBUS Voltage Alarm High Configure Byte 1 Register

7	6	5	4	3	2	1	0
Reserved						VBUS_ALARM_HIGH_THRESHOLD[9:8]	
R						RW	

LEGEND: R/W = Read/Write; R = Read only

VBUS Voltage Alarm High Configure Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	0x00	Reserved
1:0	VBUS_ALARM_HIGH_THRESHOLD[9:8]	RW	0x00	VBUS Alarm High Threshold[9:8] 10-bit for voltage threshold with 25 mV LSB. ±5% accuracy.

VBUS Voltage Alarm Low Configure Byte 0 Register (address = 0x78) [reset = 0x00]

The TCPM writes to this registers to set the low voltage alarm level. The FP6606 sets ALERT. VBUS Voltage Alarm Low (Reg.0x11 [0]) to 1 when VBUS drops below the under voltage level. These registers are required if it is reported as supported in the one of the DEVICE_CAPABILITES registers (Reg.0x25 [2]).

VBUS Voltage Alarm Low Configure Byte 0 Register

7	6	5	4	3	2	1	0
VBUS_ALARM_LOW_THRESHOLD[7:0]							
RW							

LEGEND: R/W = Read/Write; R = Read only

VBUS Voltage Alarm Low Configure Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	VBUS_ALARM_LOW_THRESHOLD[7:0]	RW	0x00	VBUS Alarm Low Threshold[7:0] 10-bit for voltage threshold with 25 mV LSB. ±5% accuracy.

VBUS Voltage Alarm Low Configure Byte 1 Register (address = 0x79) [reset = 0x00]

VBUS Voltage Alarm Low Configure Byte 1 Register

7	6	5	4	3	2	1	0
Reserved						VBUS_ALARM_LOW_THRESHOLD[9:8]	
R						RW	

LEGEND: R/W = Read/Write; R = Read only

VBUS Voltage Alarm Low Configure Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	0x00	Reserved
1:0	VBUS_ALARM_LOW_THRESHOLD[9:8]	RW	0x00	VBUS Alarm Low Threshold[9:8] 10-bit for voltage threshold with 25 mV LSB. ±5% accuracy.

System Control Byte 0 (address = 0x80) [reset = 0x10]

System Control Byte 0 Register

7	6	5	4	3	2	1	0
Reserved					OTSD_EN	INT_VCONNDIS_DIS	INT_VBUSDIS_DIS
RW					RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

System Control Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	RW	00010	Reserved
2	OTSD_EN	RW	0	Enable Over Temperature Shutdown 1b : Enable on die thermal diode function 0b : Disable on die thermal diode function
1	INT_VCONNDIS_DIS	RW	0	Disable Internal VCONN Discharge 1b : Disable VCONN discharge function 0b : Set auto turn on VCONN discharge function
0	INT_VBUSDIS_DIS	RW	0	Disable Internal VBUS Discharge 1b : Disable VBUS discharge function 0b : Set auto turn on VBUS discharge function

System Control Byte 1 Register (address = 0x81) [reset = 0x00]

System Control Byte 1 Register

7	6	5	4	3	2	1	0
Reserved		VCONN_DET_EN	VBUS_DET_EN	Reserved	TX_CARRIER_MODE2_SEL	QC_SRC_RST	TX_FAST_ROLE_SWAP_ST
RW		RW	RW	RW	RW	W	RW

LEGEND: R/W = Read/Write; R = Read only

System Control Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	RW	00	Reserved
5	VCONN_DET_EN	RW	0	Enable VCONN Detection 1b : Enable VCONN detect (to AIP) 0b : Disable VCONN detect (to AIP)
4	VBUS_DET_EN	RW	0	Enable VBUS Detection 1b : Enable VBUS detect (to AIP) 0b : Disable VBUS detect (to AIP)
3	Reserved	RW	0	Reserved
2	TX_CARRIER_MODE2_SEL	RW	0	Transmit Carrier Mode 2 Selection 1b: FP6606 shall continuously send BIST carrier mode 2 data when the BIST carrier mode 2 is issued. 0b: FP6606 will stop to send BIST carrier mode 2 data at 45ms when BIST carrier mode 2 is issued.
1	QC_SRC_RST	W	0	Reset QC source and SCP Function This bit is written by TCPM and automatically cleared by FP6606. 0b: Maintain the original QC source status. 1b: Reset QC source & SCP
0	TX_FAST_ROLE_SWAP_ST	RW	0	Transmit Fast Role Swap Start This field is used to execute the fast role swap when the role of FP6606 is transmitter. 0b: Stop fast role swap 1b: Start fast role swap

Mode Status Byte 0 Register (address = 0x83) [reset = 0x01]

Mode Status Byte 0 Register

7	6	5	4	3	2	1	0
QC_MODE_STATUS				Reserved			
R				R			

LEGEND: R/W = Read/Write; R = Read only

Mode Status Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:4	QC_MODE_STATUS	R	0x0	QC Mode Status It is used to monitor the situation of QC source. 0000b: IDLE 0001b: Reserved 0010b: Reserved 0011b: DIV_MODE(Apple 2.4A Mode) 0100b: Reserved 0101b: DCP 0110b: Reserved 0111b: TRY_QC 1000b: DLY_40ms 1001b: QC_MODE_5V 1010b: QC_MODE_CONT 1011b: QC_MODE_9V 1100b: QC_MODE_12V 1101b: QC_MODE_20V 1110b: QC_MODE_UNDEF 1111b: QC_FCP_MODE
3:2	Reserved	R	0x0	Reserved

Mode Status Byte 1 Register (address = 0x84) [reset = 0x10]

Mode Status Byte 1 Register

7	6	5	4	3	2	1	0
Reserved	VCONN_OTSD_FLAG	Reserved					
R	R	R					

LEGEND: R/W = Read/Write; R = Read only

Mode Status Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0x0	Reserved
6	VCONN_OTSD_FLAG	R	0	VCONN Over Temperature Shutdown Flag This function is valid if VCONN is applied to CC pin. When the temperature of the VCONN switch is higher than the 160°C, the VCONN switch will be automatically turned off until the temperature decreases to 130°C. 0b: No VCONN over temperature. 1b: VCONN switch occurs over temperature.
5:0	Reserved	R	0x0	Reserved

External NMOS Control Register (address = 0x85) [reset = 0x00]

External NMOS Control Register

7	6	5	4	3	2	1	0
Reserved						NMOS_SNK_ON	NMOS_SRC_ON
R						RW	RW

LEGEND: R/W = Read/Write; R = Read only

External NMOS Control Register Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	0x00	Reserved
1	NMOS_SNK_ON	RW	0	Turn on Sink NMOS TCPM writes this bit to control the sink NMOS driver for turning on or turning off. 0b: Disable VBUS power on sinking connector port. 1b: Enable VBUS power on sinking connector port.
0	NMOS_SRC_ON	RW	0	Turn on Source NMOS TCPM writes this bit to control the source NMOS driver for turning on or turning off. 0b: Disable VBUS power on sourcing connector port. 1b: Enable VBUS power on sourcing connector port.

System Control Byte 2 Register (address = 0x86) [reset = 0x00]

System Control Byte 2 Register

7	6	5	4	3	2	1	0
Reserved		Reserved		FASTROLE_RX_EN	Reserved	Reserved	
RW		RW		RW	RW	RW	

LEGEND: R/W = Read/Write; R = Read only

System Control Byte 2 Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	RW	00	Reserved
5:4	Reserved	RW	00	Reserved
3	FASTROLE_RX_EN	RW	0	Enable Receive Fast Role Swap This field is used to enable receive fast role swap when the role of FP6606 is receiver (only sink device). 0b : Fast role swap detect disable 1b : Fast role swap detect enable
2	Reserved	RW	0	Reserved
1:0	Reserved	RW	00	Reserved

Vendor Interrupts Byte 0 Register (address = 0x90) [reset = 0x00]

This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the FP6606 will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.
For example, if Reg.0x13 [7] VENDOR_DEFINED_ALERT_MASK and the corresponding vendor interrupts mask (Reg.0x92 & 0x93) are written 1b for unmasking, the INT_N will assert low when FP6606 occurs vendor interrupt event. The TCPM should examine what the vendor interrupt event (Reg.0x91 & 0x92) occurs and deal with it.

Vendor Interrupts Byte 0 Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	I_ADC_VOLT_UPDATE	I_VCONN_OC	I_VCONN_OTSD_OCCUR	Reserved	I_FAST_ROLE_SWAP_OCCUR
RCU	RCU	RCU	RCU	RCU	RCU	RCU	RCU

LEGEND: R/W = Read/Write; R = Read only

Vendor Interrupts Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RCU	0	Reserved
6	Reserved	RCU	0	Reserved
5	Reserved	RCU	0	Reserved
4	I_ADC_VOLT_UPDATE	RCU	0	ADC Voltage Update Interrupt 0b: Cleared. 1b: FP6606 has finished the voltage ADC and the data of ADC has stored with corresponding register (Reg.0xC1~0xC2). If the data of ADC is different from previous one, this bit will be change to 1b. TCPM can access the data of ADC while this bit changes to 1b.
3	I_VCONN_OC	RCU	0	VCONN Over Current Interrupt 0b: No VCONN OC 1b : Over-current event occur on VCONN
2	I_VCONN_OTSD_OCCUR	RCU	0	VCONN Over Temperature Shutdown Occur 0b: No OTSD 1b : Over temperature event occurs in VCONN switch
1	Reserved	RCU	0	Reserved
0	I_FAST_ROLE_SWAP_OCCUR	RCU	0	Fast Role Swap Occur Interrupt 0b: Cleared 1b : Fast role swap request received

Vendor Interrupts Byte 1 Register (address = 0x91) [reset = 0x00]

This register is used to indicate a status change event. When a status change event occurs and its corresponding Alert mask is unmasked, the FP6606 will assert the INT_N low. The INT_N remains asserted until all events are cleared by write of 1'b1. Once all events are cleared or corresponding Alert mask is masked, the INT_N will be de-asserted high.
For example, if Reg.0x13 [7] VENDOR_DEFINED_ALERT_MASK and the corresponding vendor interrupts mask (Reg.0x92 & 0x93) are written 1b for unmasking, the INT_N will assert low when FP6606 occurs vendor interrupt event. The TCPM should examine what the vendor interrupt event (Reg.0x91 & 0x92) occurs and deal with it.

Vendor Interrupts Byte 1 Register

7	6	5	4	3	2	1	0
Reserved			I_OV_EVENT	Reserved	I_ADC_CUR_UPDATE	Reserved	I_QC_ST_CHG
R			RCU	RCU	RCU	RCU	RCU

LEGEND: R/W = Read/Write; R = Read only

Vendor Interrupts Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	RCU	000	Reserved
4	I_ OV_EVENT	RCU	0	Over Voltage Event Interrupt 0b: No over voltage on CC/D+/D−/VBUS pin. 1b: Over voltage event occur on CC/D+/D−/VBUS pin.
3	Reserved	RCU	0	Reserved
2	I_ADC_CUR_UPDATE	RCU	0	ADC Current Update Interrupt 0b: ADC is converting. 1b: FP6606 has finished the current ADC and the data of ADC has stored with corresponding register (Reg.0xC3~0xC4). If the data of ADC is different from previous one, this bit will be change to 1b. TCPM can access the data of ADC while this bit changes to 1b.
1	Reserved	RCU	0	Reserved
0	I_QC_ST_CHG	RCU	0	QC Mode Status Change Interrupt 0b: Cleared 1b: The QC mode status has been changed by FP6606. TCPM could check the value of Reg.0x83 [7:4].

Vendor Interrupts Mask Byte 0 Register (address = 0x92) [reset = 0x00]

Vendor Interrupts Mask Byte 0 Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	I_ADC_VOLT_UPDATE_MASK	I_VCONN_OC_MASK	I_VCONN_OTSD_MASK	Reserved	I_FAST_ROLE_SWAP_MASK
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Vendor Interrupts Mask Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Reserved
6	Reserved	RW	0	Reserved
5	Reserved	RW	0	Reserved
4	I_ADC_VOLT_UPDATE_MASK	RW	0	ADC Voltage Update Interrupt Mask 0b : Disable interrupt 1b : Enable interrupt
3	I_VCONN_OC_MASK	RW	0	VCONN Over Current Interrupt Mask 0b : Disable interrupt 1b : Enable interrupt
2	I_VCONN_OTSD_MASK	RW	0	Over Temperature Interrupt Mask 0b : Disable interrupt 1b : Enable interrupt
1	Reserved	RW	0	Reserved
0	I_FAST_ROLE_SWAP_MASK	RW	0	Fast Role Swap Interrupt Mask 0b : Disable interrupt 1b : Enable interrupt

Vendor Interrupts Mask Byte 1 Register (address = 0x93) [reset = 0x00]

Vendor Interrupts Mask Byte 1 Register

7	6	5	4	3	2	1	0
Reserved			I_CC_OV_MASK	Reserved	I_ADC_CUR_UPDATE_MASK	Reserved	I_QC_ST_CHG_MASK
RW			RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Vendor Interrupts Mask Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	RW	000	Reserved
4	I_CC_OV _MASK	RW	0	CC Over Voltage Interrupt Mask 0b : Disable interrupt 1b : Enable interrupt
3	Reserved	RW	0	Reserved
2	I_ADC_CUR_UPDATE_MASK	RW	0	ADC Current Update Interrupt Mask 0b : Disable interrupt 1b : Enable interrupt
1	Reserved	RW	0	Reserved
0	I_QC_ST_CHG_MASK	RW	0	QC Mode Status Change Mask 0b : Disable interrupt 1b : Enable interrupt

CC General Control Register (address = 0x94) [reset = 0x04]

CC General Control Register

7	6	5	4	3	2	1	0
Reserved	PD_TXRX_RESET	GLOBAL_SW_RESET	AUTO_DRP_SAMPLE_CTRL	CC_SAMPLE_RATE		DRP_DUTY_CYCLE	
RW	W	W	RW	RW		RW	

LEGEND: R/W = Read/Write; R = Read only

CC General Control Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Reserved
6	PD_TXRX_RESET	W	0	Reset PD Transmit and Receive: Both PD TX and RX state machines are reset when TCPM writes this field with a 1b. This bit is written by TCPM and automatically cleared by FP6606. 0b: No operation 1b: Reset PD engine
5	GLOBAL_FW_RESET	W	0	Global Reset: The FP6606 will be reset to power on default when TCPM writes this field with a 1b. This bit is written by TCPM and automatically cleared by FP6606. 0b: No operation 1b: Global reset
4	AUTO_DRP_SAMPLE_CTRL	RW	0	Auto DRP Sample Control: When FP6606 is enabled for autonomous DRP toggle, this field controls when CC pins are sampled while unattached. 0b: Continuously checks CC pins based on CC_SAMPLE_RATE field (Reg.0x97 [3:2]). 1b: Only checks CC pins just before Role toggle.
3:2	CC_SAMPLE_RATE	RW	01	CC Sample Rate: This field controls the FP6606 CC pins sample rate. 00b : 1ms 01b : 2ms 10b : 8ms 11b : 16ms
1:0	DRP_DUTY_CYCLE	RW	00	DRP Duty Cycle 00b : 30% , total scan time = 50 ms 01b : 50% , total scan time = 70 ms 10b : 56.25% , total scan time = 80 ms 11b : 65% , total scan time = 100 ms

MTP Control Byte 0 Register (address = 0x98) [reset = 0x00]

MTP Control Byte 0 Register

7	6	5	4	3	2	1	0
Reserved	Reserved		MTP_REG_WREN	Reserved	MTP_WRITE	MTP_ERASE	MTP_READ
RW	RW		RW	R	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

MTP Control Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Reserved
6:5	Reserved	RW	00	Reserved
4	MTP_REG_WREN	RW	0	MTP Register Write Enable The MTP registers are locked by this field. The MTP registers could be changed if TCPM writes this field with a 1b. 0b : Register write disable 1b : Register write enable
3	Reserved	R	0	Reserved
2	MTP_WRITE	RW	0	MTP Program Trigger TCPM writes the data to MTP register firstly and TCPM writes this field with a 1b. The MTP register is therefore changed. 0b : No operation 1b : Program MTP
1	MTP_ERASE	RW	0	MTP Erase Trigger TCPM selects MTP register that want to erase firstly and TCPM writes this field with a 1b. The MTP register is therefore erased. 0b :No operation 1b :Erase MTP
0	MTP_READ	RW	0	MTP Read Trigger TCPM writes this field with a 1b, then, the MTP registers could be read. 0b :No operation 1b :Read MTP

MTP Control Byte 1 Register (address = 0x99) [reset = 0x00]

MTP Control Byte 1 Register

7	6	5	4	3	2	1	0
MTP_ERASE_TYPE	MTP_ERASE_PAGE			MTP_WRITE_TYPE	MTP_WRITE_PAGE		
RW	RW			RW	RW		

LEGEND: R/W = Read/Write; R = Read only

MTP Control Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7	MTP_ERASE_TYPE	RW	0	MTP Erase Type: MTP Chip / Page Erase 0b: Chip Erase 1b: Page Erase
6:4	MTP_ERASE_PAGE	RW	00	MTP Page Erase: The MTP page erase function is locked by the password. The password must be filled in the MTP_PASSWORD [7:0] (Reg.0x9A). The page form 2 to 7 make public to the customers and the password is B7h. However, both page 0 and page 1 are reserved by vendor. 000b: Erase page 0 001b: Erase page 1 010b: Erase page 2 011b: Erase page 3 100b: Erase page 4 101b: Erase page 5 110b: Erase page 6 111b: Erase page 7
3	MTP_WRITE_TYPE	RW	0	MTP Write Type: MTP Chip / Page Program 0b: Chip Program 1b: Page Program
2:0	MTP_WRITE_PAGE	RW	00	MTP Page Program: The MTP page program function is locked by the password. The password must be filled in the MTP_PASSWORD [7:0] (Reg.0x9A). The page form 2 to 7 make public to the customers and the password is B7h. However, both page 0 and page 1 are reserved by vendor. 000b: Program page 0 001b: Program page 1 010b: Program page 2 011b: Program page 3 100b: Program page 4 101b: Program page 5 110b: Program page 6 111b: Program page 7

MTP Password Register (address = 0x9A) [reset = 0x00]

MTP Password Register

7	6	5	4	3	2	1	0
MTP_PASSWORD							
RW							

LEGEND: R/W = Read/Write; R = Read only

MTP Password Register Descriptions

Bit	Field	Type	Reset	Description
7:0	MTP_PASSWORD	RW	0x00	MTP Password The customer password is B7h for chip program / erase and page program / erase.

QC Protocol Control Byte 0 Register (address = 0x9C) [reset = 0xC0]

QC Protocol Control Byte 0 Register

7	6	5	4	3	2	1	0
QC_SRC_DIS	HVDCP_DIS	QC3.0_DIS	QC2.0_DIS	Reserved	SCP_FCP_DIS	QC_SNK_DIS	PD_DIS
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

QC Protocol Control Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7	QC_SRC_DIS	RW	1	Qualcomm Quick Charge Disable 0b :QC source enable 1b :QC source disable
6	HVDCP_DIS	RW	1	Qualcomm Quick Charge Disable 0b : with HVDCP function 1b : No HVDCP function (default 5V)
5	QC3.0_DIS	RW	0	Qualcomm Quick Charge 3.0 Disable (SRC only) 0b :QC 3.0 continuous mode enable 1b :QC 3.0 continuous mode disable
4	QC2.0_DIS	RW	0	Qualcomm Quick Charge 2.0 Disable (SRC only) 0b :QC 2.0 mode enable 1b :QC 2.0 mode disable
3	Reserved	RW	0	Reserved
2	SCP_FCP_DIS	RW	0	Huawei Super Charge/Fast Charge Protocol Disable (SRC only) 0b :SCP/FCP mode enable 1b :SCP/FCP mode disable
1	QC_SNK_DIS	RW	0	Qualcomm Quick Charge Disable (SNK only) 0b: QC sink enable 1b: QC sink disable
0	PD_DIS	RW	0	USB PD Disable (SRC/SNK) 0b: PD enable 1b: PD disable

QC Protocol Control Byte 1 Register (address = 0x9D) [reset = 0x00]

QC Protocol Control Byte 1 Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	FBO_CTRL	QC_CLASS_ CTRL	Reserved	Reserved	QC_H_VOLT _CTRL
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

QC Protocol Control Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0	Reserved
6	Reserved	RW	0	Reserved
5	Reserved	RW	0	Reserved
4	FBO_CTRL	RW	0	Feedback Output Node Control: FP6606 utilizes the feedback pin of the power stage to obtain the VBUS voltage control. 0b: Disable FBO pin to control the power stage 1b: Enable FBO pin to control the power stage
3	QC_CLASS_CTRL	RW	0	Qualcomm Quick Charge (SRC only) QC source class A enable 0b: Class B enable (QC 2.0 5V, 9V, 12V, 20V) 1b: Class A enable (QC 2.0 5V, 9V, 12V)
2	Reserved	RW	0	Reserved
1	Reserved	RW	0	Reserved
0	QC_H_VOLT_CTRL	RW	0	Qualcomm Quick Charge (SRC only) QC source 12V disable 0b : 12V enable (QC 2.0 5V, 9V, 12V, 20V) 1b : 12V disable (QC 2.0 5V, 9V)

Dead Battery Voltage Selection Register (address = 0xAC) [reset = 0x01]

Dead Battery Voltage Selection Register

7	6	5	4	3	2	1	0
Reserved					DEAD_BATTERY_SEL		
R					RW		

LEGEND: R/W = Read/Write; R = Read only

Dead Battery Voltage Selection Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0x00	Reserved
2:0	DEAD_BATTERY_SEL	RW	001	Dead Battery Voltage Selection: Suppose TCPM writes this field with a 000b. FP6606 is supplied by VDD and NMOS_SNK_ON (Reg.0x85 [1]) is automatically disabled by FP6606 when VDD is larger than 2.8V. However, FP6606 is supplied by VBUS and NMOS_SNK_ON (Reg.0x85 [1]) is enabled automatically by FP6606 when VDD is lower than 2.6V. In this manner, the dead battery function in FP6606 is therefore implemented. 000b: Dead Battery Voltage 2.6V. Rising 2.8V 001b: Dead Battery Voltage 2.7V. Rising 2.9V 010b: Dead Battery Voltage 2.8V. Rising 3.0V 011b: Dead Battery Voltage 2.9V. Rising 3.1V 100b: Dead Battery Voltage 3.0V. Rising 3.2V

ADC Control Register (address = 0xC0) [reset = 0x81]

ADC Control Register

7	6	5	4	3	2	1	0
Reserved	TM_DRIVE_SEL		ADC_DEBOUNCE_TIME		ADC_SCAN_TIME		
RW	RW		RW	RW	RW		

LEGEND: R/W = Read/Write; R = Read only

ADC Control Register Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	1	Reserved
6:5	TM_DRIVE_SEL	RW	00	TM Pin Drive current: The scale of current from TM pin could be selected by this field. The TM pin current is used to drive the connected thermal resistance. The voltage on the thermal resistance is therefore converted to temperature by ADC_TEMP_DATA (Reg.0xC4). 00b: 1.25uA 01b: 5uA 10b: 20uA 11b: 100uA
4:3	ADC_DEBOUNCE_TIME	RW	00	ADC Debounce Time: 00b: 0 time 01b: 1 time 10b: 2 times 11b: 3 times
2:0	ADC_SCAN_TIME	RW	01	ADC Scan Time: This field is used to decide how often to do an ADC conversion. 000b: 4ms 001b: 8ms 010b: 16ms 011b: 32ms 100b: 64ms 101b: 128ms

ADC IBUS Data Register (address = 0xC3) [reset = 0x00]

ADC IBUS Data Register

7	6	5	4	3	2	1	0
ADC_IBUS_DATA							
R							

LEGEND: R/W = Read/Write; R = Read only

ADC IBUS Data Register Descriptions

Bit	Field	Type	Reset	Description
7:0	ADC_IBUS_DATA	R	0x00	ADC IBUS Data: This field shows the current flowing from IS+ pin to IS− pin. The value of current measurement could be obtained by the following equation. IBUS = ADC_IBUS_DATA / (1992.1875*Rs) Where IBUS is the current flowing from IS+ pin to IS− pin. Rs is the resistance between IS+ pin and IS− pin. If Rs is equation to 10m Ohm, the equation is therefore rearranged as follow: IBUS = ADC_IBUS_DATA *50.19608mA

ADC Temperature Data Register (address = 0xC4) [reset = 0x00]

ADC Temperature Data Register

7	6	5	4	3	2	1	0
ADC_TEMP_DATA							
R							

LEGEND: R/W = Read/Write; R = Read only

ADC Temperature Data Register Descriptions

Bit	Field	Type	Reset	Description
7:0	ADC_TEMP_DATA	R	0x00	ADC Temperature Data: The value of voltage on TM pin measurement is presented in this field. The TM pin must be connected to the thermal resistor and the selected current of TM pin (Reg.0xC0 [6:5]) will flow to the thermal resistor. This field could represent analog voltage ranging from 0V to 2.4V. Each bit of this field can be calculated as 9.41176471mV. Additionally, the converted temperature is according to the different thermal resistor and TM_DRIVE_SEL (Reg.0xC0 [6:5]) selected by the customer.

GPIO Direction Control Register (address = 0xC8) [reset = 0x00]

GPIO Direction Control Register

7	6	5	4	3	2	1	0
Reserved					GPIO2_DIR_CTRL	GPIO1_DIR_CTRL	GPIO0_DIR_CTRL
R					RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

GPIO Direction Control Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0	Reserved
2	GPIO2_DIR_CTRL	RW	0	GPIO2 Direction Control 0b: Input 1b: Output
1	GPIO1_DIR_CTRL	RW	0	GPIO1 Direction Control 0b: Input 1b: Output
0	GPIO0_DIR_CTRL	RW	0	GPIO0 Direction Control 0b: Input 1b: Output

GPIO Output Data Register (address = 0xC9) [reset = 0x00]

GPIO Output Data Register

7	6	5	4	3	2	1	0
Reserved					GPIO2_OUTPUT_DATA	GPIO1_OUTPUT_DATA	GPIO0_OUTPUT_DATA
R					RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

GPIO Output Data Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0	Reserved
2	GPIO2_OUTPUT_DATA	RW	0	GPIO2 Output Data The direction of GPIO2 must be specified as output before setting this bit. (Reg.0xC8[2]=1) 0b: Low 1b: High
1	GPIO1_OUTPUT_DATA	RW	0	GPIO1 Output Data The direction of GPIO1 must be specified as output before setting this bit. (Reg.0xC8[1]=1) 0b: Low 1b: High
0	GPIO0_OUTPUT_DATA	RW	0	GPIO0 Output Data The direction of GPIO1 must be specified as output before setting this bit. (Reg.0xC8[0]=1) 0b: Low 1b: High

GPIO Input Data Register (address = 0xCA) [reset = 0x00]

GPIO Input Data Register

7	6	5	4	3	2	1	0
Reserved					GPIO2_INPUT_DATA	GPIO1_INPUT_DATA	GPIO0_INPUT_DATA
R					R	R	R

LEGEND: R/W = Read/Write; R = Read only

GPIO Input Data Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0	Reserved
2	GPIO2_INPUT_DATA	R	0	GPIO2 Input Data The direction of GPIO2 must be specified as input before reading this bit. (Reg.0xC8[2]=0) 0b: Low 1b: High
1	GPIO1_INPUT_DATA	R	0	GPIO1 Input Data The direction of GPIO1 must be specified as input before reading this bit. (Reg.0xC8[1]=0) 0b: Low 1b: High
0	GPIO0_INPUT_DATA	R	0	GPIO0 Input Data The direction of GPIO1 must be specified as input before reading this bit. (Reg.0xC8[1]=0) 0b: Low 1b: High

Role Judge Finish Register (address = 0xCB) [reset = 0x00]

Role Judge Finish Register

7	6	5	4	3	2	1	0
Reserved		ROLE_JUDGE_FINISH	Reserved	Reserved	Reserved	Reserved	Reserved
RW		RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only

Role Judge Finish Register Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	RW	00	Reserved
5	ROLE_JUDGE_FINISH	RW	0	Role Judge Finish: The purpose of this bit is power saving. TCPM should write this bit with a 1b if the role of FP6606 is finished connecting as source/sink. Then, the internal circuit of FP6606 will be activated from power saving mode. However, TCPM should write this bit with a 0b when there is no device connected with FP6606. 0b: The status of FP6606 is power saving mode. 1b: The status of FP6606 is activated from power saving mode.
4:0	Reserved	RW	0x0	Reserved

Over Voltage Detect Register (address = 0xCC) [reset = 0x00]

Over Voltage Detect Register

7	6	5	4	3	2	1	0
FAULT_PIN_EN	DP_DN_OV_SEL	DP_DN_OV_EN	VBUS_OV_EN	VBUS_OV_SEL			
RW	RW	RW	RW	RW			

LEGEND: R/W = Read/Write; R = Read only

Over Voltage Detect Register Descriptions

Bit	Field	Type	Reset	Description
7	FAULT_PIN_EN	RW	0	Fault Pin Enable: The fault pin is assigned to GPIO 2. If TCPM needs to sense the fault event (VBUS OV, DP_DN OV and CC OV), this field must be written with a 1b. In this manner, FP6606 will drive the fault to pin to high when the fault event occurring. 1b: Fault pin enable 0b: Fault pin disable
6	DP_DN_OV_SEL	RW	0	DP/DN Overvoltage Level Select: FP6606 support two DP/DN overvoltage level. In case DP/DN pin is suffered from abnormal high voltage, the fault pin (GPIO 2) will be drive to high for alerting the TCPM. 0b: 4V 1b: 4.5V
5	DP_DN_OV_EN	RW	0	DP/DN OV Check Enable 0b: No operation 1b: Start to check DP/DN overvoltage
4	VBUS_OV_EN	RW	0	VBUS OV Check Enable 0b: No operation 1b: Start to check VBUS overvoltage
3:0	VBUS_OV_SEL	RW	0x0	VBUS Overvoltage Select: The VBUS overvoltage can be selected based on the operated VBUS. TCPM could write this field with a 0000b if the VBUS of power stage is operated as 5V. In this manner, when the VBUS is larger than 6V, FP6606 will drive the fault pin (GPIO 2) to high and TCPM will be informed the abnormal situation. 0000b: Operated VBUS = 5V, VBUS OV = 6V 0001b: Operated VBUS = 6V, VBUS OV = 7.2V 0010b: Operated VBUS = 7V, VBUS OV = 8.4V 0011b: Operated VBUS = 8V, VBUS OV = 9.6V 0100b: Operated VBUS = 9V, VBUS OV = 10.8V 0101b: Operated VBUS = 10V, VBUS OV = 12V 0110b: Operated VBUS = 11V, VBUS OV = 13.2V 0111b: Operated VBUS = 12V, VBUS OV = 14.4V 1000b: Operated VBUS = 13V, VBUS OV = 15.6V 1001b: Operated VBUS = 14V, VBUS OV = 16.8V 1010b: Operated VBUS = 15V, VBUS OV = 18V 1011b: Operated VBUS = 16V, VBUS OV = 19.2V 1100b: Operated VBUS = 17V, VBUS OV = 20.4V 1101b: Operated VBUS = 18V, VBUS OV = 21.6V 1110b: Operated VBUS = 19V, VBUS OV = 22.8V 1111b: Operated VBUS = 20V, VBUS OV = 24V Note: VBUS OV is set by 1.2 times, compared to the operated VBUS.

Over Voltage Status Register (address = 0xCD) [reset = 0x00]

This register is related with Over Voltage Detection Register (Reg.0xCC). Each status bit is effect when Over Voltage Detection Register (Reg.0xCC) is properly set by TCPM.

Over Voltage Status Register

7	6	5	4	3	2	1	0
Reserved					DP_DN_OV_STATUS	VBUS_OV_STATUS	CC_OV_STATUS
R					RCU	RCU	RCU

LEGEND: R/W = Read/Write; R = Read only

Over Voltage Status Register Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0x00	Reserved
2	DP_DN_OV_STATUS	RCU	0	DP/DN Overvoltage Status: 0b: Cleared 1b: D+/D- pin overvoltage level depending on Reg.0xCC [6]
1	VBUS_OV_STATUS	RCU	0	VBUS Overvoltage Status: 0b: Cleared 1b: VBUS overvoltage level depending on Reg.0xCC [3:0]
0	CC_OV_STATUS	RCU	0	CC Overvoltage Status: The CC pin overvoltage level is fixed to 6.5V. It cannot be set by TCPM. 0b: Cleared 1b: CC pin overvoltage

VBUS Control Register (address = 0xD0) [reset = 0x00]

The FBO pin of FP6606 must be connected to the feedback node of power stage. The upper feedback resistance of power stage needs to select 100k Ohm and the VBUS of power stage also designs to default 5V. Consequently, the VBUS could be increased or decreased by sinking or sourcing current from FBO pin of the FP6606.
The scale of FBO pin sink/source current is set by 11-bit MCU IT counter (Reg.0xD2~D1). The VBUS is default 5V when MCU IT counter is default C8h (200 in decimal) and the FBO pin is no operation. If the value of MCU IT counter is set to lower than C8h, the FBO pin will source current and the VBUS will be decreased. The lowest VBUS is 3V when MCU IT counter is set to zero. However, in case the value of MCU IT counter is set to larger than C8h (200 in decimal), the FBO pin will sink current and the VBUS will be increased. The highest VBUS is 23.47V when MCU IT counter is full (7FFh).

VBUS Control Register

7	6	5	4	3	2	1	0
MCU_CTRL_VOLT_RST	Reserved						MCU_VOLT_EN_CTRL
W	R						RW

LEGEND: R/W = Read/Write; R = Read only

VBUS Control Register Descriptions

Bit	Field	Type	Reset	Description
7	MCU_CTRL_VOLT_RST	W	0	MCU Voltage Control Reset: TCPM reset MCU IT counter and FP6606 will clear this bit automatically. 0b: No operation 1b: Reset MCU IT counter. VBUS Target Control Register (Reg.0xD1~D2) reset to default value. The VBUS will be reset to 5V when TCPM writes this bit with a 1b
6:1	Reserved	R	0x00	Reserved
0	MCU_VOLT _EN_CTRL	RW	0	MCU Voltage Control Enable: 0b: MCU IT counter is controlled by FP6606 1b: MCU IT counter is controlled by TCPM through setting VBUS Target Control Register (Reg.0xD1~D2)

VBUS Target Control Byte 0 Register (address = 0xD1) [reset = 0xC8]

VBUS Target Control Byte 0 Register

7	6	5	4	3	2	1	0
MCU_IT_CNT_L							
RW							

LEGEND: R/W = Read/Write; R = Read only

VBUS Target Control Byte 0 Register Descriptions

Bit	Field	Type	Reset	Description
7:0	MCU_IT_CNT_L	RW	0xC8	MCU IT Counter Low: The MCU IT counter is validly set only by even number. Each bit of MCU IT counter represents 10mV of VBUS. The resolution of VBUS is 20mV because only even number can be set to MCU IT counter. The MCU IT counter is 11-bit, which is configured as follow equation: MCU_IT_CNT [10:0]= MCU_IT_CNT_H [10:8] + MCU_IT_CNT_L [7:0]

VBUS Target Control Byte 1 Register (address = 0xD2) [reset = 0x00]

VBUS Target Control Byte 1 Register

7	6	5	4	3	2	1	0
MCUL_VOLT _SET	Reserved	Reserved	Reserved		MCU_IT_CNT_H		
RW	RW	RW	R		RW		

LEGEND: R/W = Read/Write; R = Read only

VBUS Target Control Byte 1 Register Descriptions

Bit	Field	Type	Reset	Description
7	MCU _VOLT_SET	RW	0	MCU Voltage Set 0b: No operation 1b: The setting of MCU IT counter is taken effect
6	Reserved	RW	0	Reserved
5	Reserved	RW	0	Reserved
4:3	Reserved	R	00	Reserved
2:0	MCU_IT_CNT_H	RW	00	MCU IT Counter High: The MCU IT counter is validly set only by even number. Each bit of MCU IT counter represents 10mV of VBUS. The resolution of VBUS is 20mV because only even number can be set to MCU IT counter. The MCU IT counter is 11-bit, which is configured as follow equation: MCU_IT_CNT [10:0]= MCU_IT_CNT_H [10:8] + MCU_IT_CNT_L [7:0]

FW Version High Byte Register (address = 0xDD) [reset = 0x00]

FW Version High Byte Register

7	6	5	4	3	2	1	0
FW_VER_H							
RW							

LEGEND: R/W = Read/Write; R = Read only

FW Version High Byte Register Descriptions

Bit	Field	Type	Reset	Description
7:0	FW_VER_H	RW	0x00	Indicate FW version usage

FW Version Low Byte Register (address = 0xDE) [reset = 0x00]

FW Version Low Byte Register

7	6	5	4	3	2	1	0
FW_VER_L							
RW							

LEGEND: R/W = Read/Write; R = Read only

FW Version Low Byte Register Descriptions

Bit	Field	Type	Reset	Description
7:0	FW_VER_L	RW	0x00	Indicate FW version usage

HW Version Register (address = 0xDF) [reset = 0x08]

HW Version Register

7	6	5	4	3	2	1	0
HW_VER					Reserved		
R					RW		

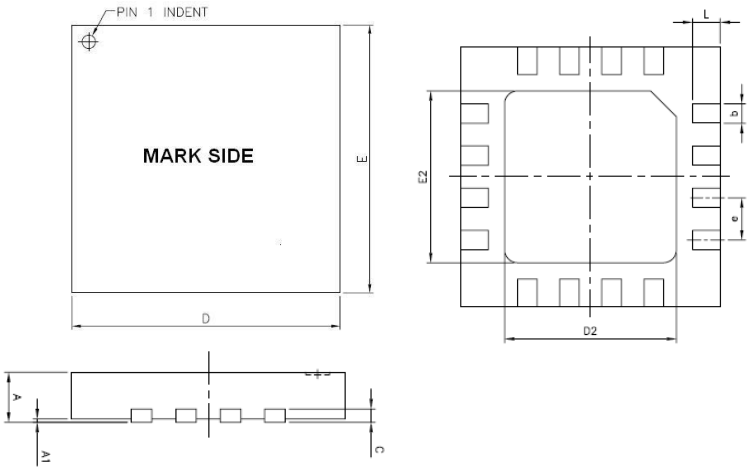
LEGEND: R/W = Read/Write; R = Read only

HW Version Register Descriptions

Bit	Field	Type	Reset	Description
7:3	HW_VER	R	00001	FP6606 HW Ver.
2:0	Reserved	RW	000	Reserved

Outline Information

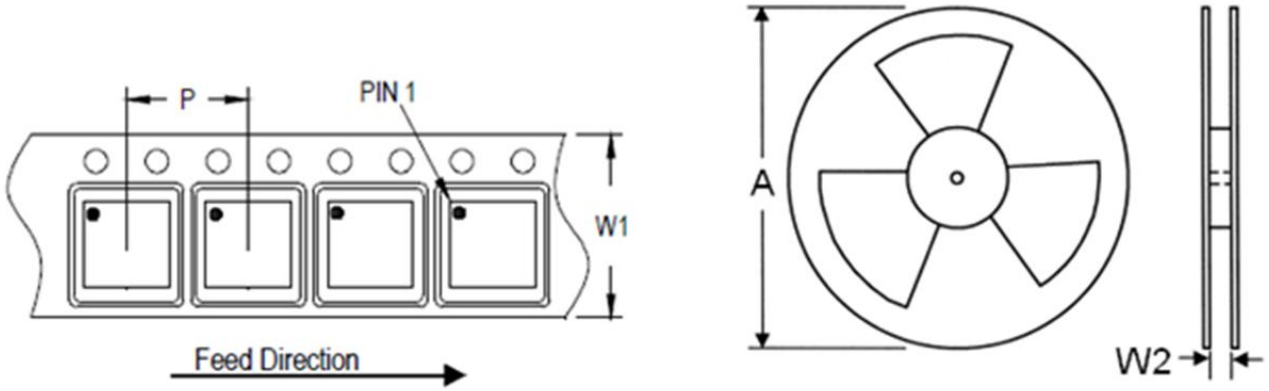
TQFN- 16 4mm×4mm (pitch 0.65mm) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
C	0.18	0.30
E	3.90	4.10
D	3.90	4.10
L	0.45	0.65
b	0.25	0.35
e	0.65 BSC	
E2	2.00	2.30
D2	2.00	2.30

Note: Followed From JEDEC MO-220

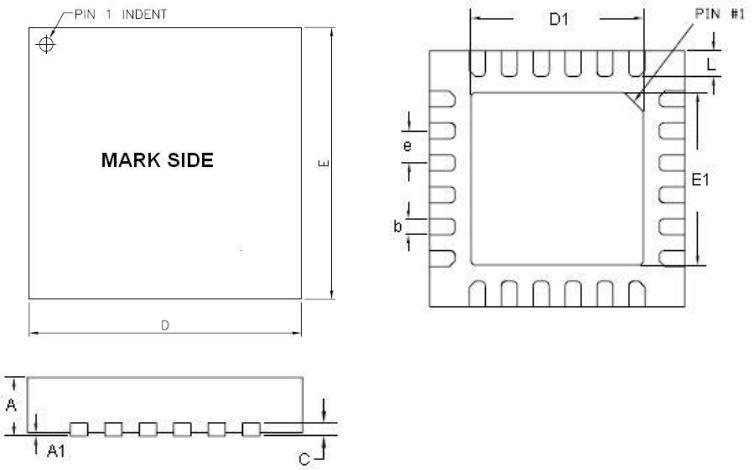
Carrier dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000

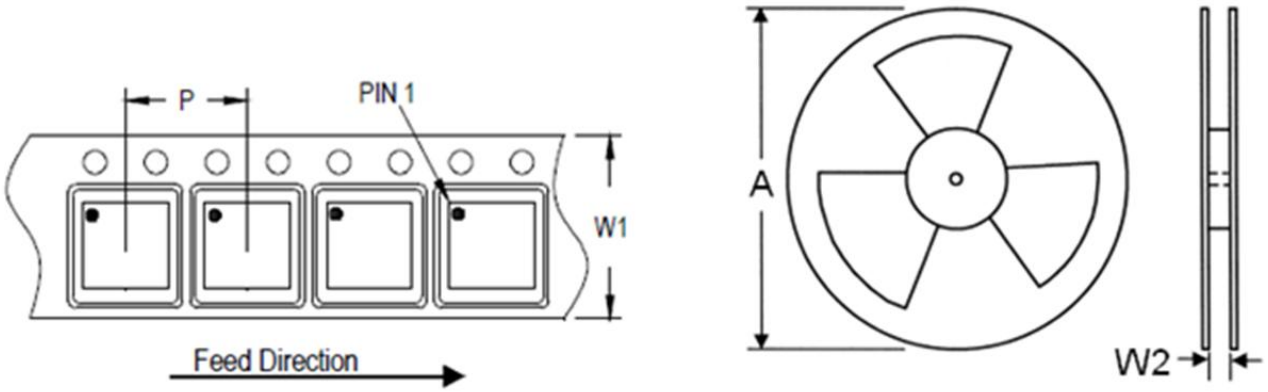
Outline Information (Continued)

TQFN- 24 4mm×4mm (pitch 0.5mm)Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
C	0.18	0.30
E	3.90	4.10
D	3.90	4.10
L	0.35	0.45
b	0.18	0.30
e	0.50 BSC	
E1	2.40	2.80
D1	2.40	2.80

Carrier dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000